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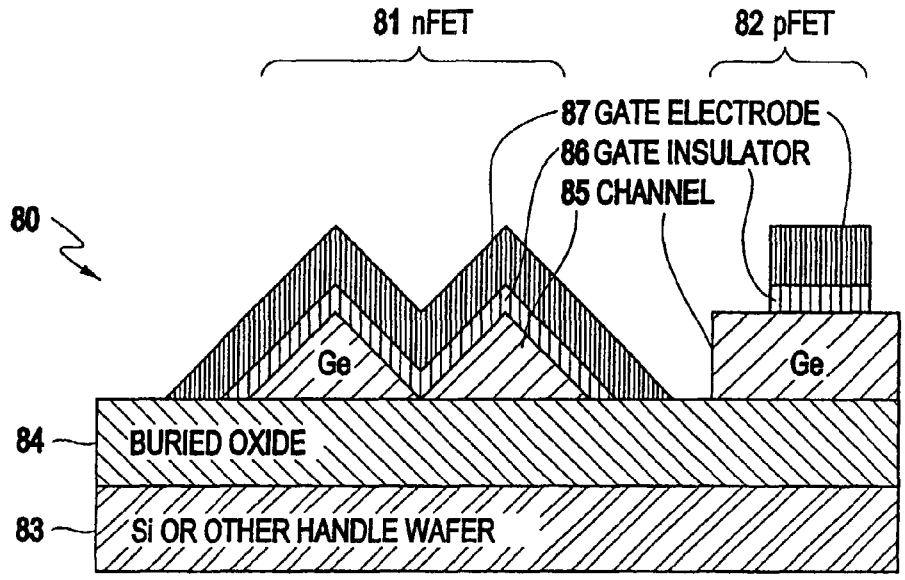
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(54) Title: N-FET AND P-FET FABRICATION ON THE SAME WAFER USING DIFFERENT CRYSTAL PLANES FOR THE OPTIMIZATION OF CARRIER TRANSPORT



(57) Abstract: A method (and structure) for an electronic chip having at least one layer of material for which a carrier mobility of a first carrier type is higher in a first crystal surface than in a second crystal surface and for which a carrier mobility of a second carrier type is higher in the second crystal surface than the first crystal surface includes a first device having at least one component fabricated on the first crystal surface of the material, wherein an activity of the component of the first device involves primarily the first carrier type, and a second device having at least one component fabricated on the second crystal surface of the material, wherein an activity of the component of the second device involves primarily the second carrier type.

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