

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN LOGICAL CIRCUITS

(71) We, HITACHI LIMITED, of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 The present invention relates to logic circuits utilizing metal insulated gate field-effect transistors (referred to hereafter as "Misfets"), and more particularly to Misfet logic circuits which employ depletion type load transistors.

15 Known Misfet logic circuits employ the system known as the EE system wherein the Misfets which operate as loads, and the Misfets which operate as drivers, are of the enhancement type. To reduce the power consumption of circuits constructed according to the above system, the circuit can be driven by means of a clock drive system wherein the load transistors are driven by clock pulse trains.

20 On the other hand, if the so-called ED system wherein a depletion type Misfet is employed as a load transistor is utilized, it proves difficult to adopt the clock drive system for the load transistors as mentioned above with reference to the EE system. However the ED system has some excellent features such as low power consumption, high speed and utilizing the ED system a high degree of circuit integration is possible as it is permissible to use a low supply voltage and take advantage of the constant current characteristic of the depletion type Misfet.

25 There is shown in Figure 5 of the accompanying drawings, the basic logic circuit according to the ED system.

30 Referring to the circuit of Figure 5, it can be seen that whenever a drive transistor such as Qd is conductive, current flows through a series circuit formed by the driving transistor Qd and a load transistor Qz.

35 It is an object of the present invention to reduce the average quantity of current which flows through the series circuit noted above,

50 to thereby further reduce the power consumption of a logic circuit constructed according to the ED system.

55 According to the present invention there is provided a logical circuit comprising a plurality of Misfet transistors (as hereinbefore defined), and wherein a Misfet acting as a load is of the depletion type, including the series connection of, firstly said depletion type Misfet, secondly a Misfet logic circuit block constructed so as to satisfy a required logical expression, and thirdly a further Misfet, the conduction of said further Misfet being controlled by a clock pulse train and said logic circuit block having first and second terminals serving to connect it respectively to the load Misfet and the further Misfet.

60 The present invention will now be described in greater detail by way of example with reference to the remaining Figures of the accompanying drawings, wherein:

65 Figure 1 shows the circuit diagram of a first embodiment of a logic circuit according to the present invention;

70 Figure 2 shows the circuit diagram of a second embodiment of a logic circuit according to the present invention;

75 Figure 3 shows the circuit diagram of a third embodiment of a logic circuit according to the present invention; and

80 Figure 4 shows the waveforms at various points in the circuit of Figure 3.

85 Referring to Figure 1 the first embodiment of a Misfet logic circuit according to the present invention includes a depletion type Misfet Qz1 wherein, even when no bias voltage is applied between the gate electrode and the source electrode thereof, current can flow between the source electrode and the drain electrode. The depletion type Misfet Qz1 is operated as a load transistor. The circuit further includes three enhancement type Misfets Qd1—Qd3 which conduct on application of a bias voltage, said voltage being applied between the gate electrode and the source electrode of the transistor and controlling current flow between the source electrode and the drain electrode of the tran-

sistor. The enhancement type Mifsets operate as drive transistors in the circuit.

In order to optimize the constant current characteristic of the Mifset Qz1, the gate electrode thereof is connected to the source electrode, which is also the output terminal of the logic circuit.

The Mifsets Qd1—Qd3 constitute a logic block designated LB the output of which can be expressed by the logic equation

$$V_{out} = (V_A + V_B) \cdot V_C,$$

(assuming P type Mifsets and a positive logic convention).

To the gate electrode of a Mifset Qd4 is applied as an input a clock pulse train ϕ which controls the conduction of the Mifset Qd4. The width of the pulses of the clock pulse train ϕ is made narrower than the width of the input pulse signals applied to the terminals VA—VC.

The Mifsets Qz1 and Qd4 and the logic block LB are connected in series. The output signal Vout is derived from the junction between the logic block LB and the load Mifset Qz1.

In a Mifset logic circuit constructed as described above current flow can only be through the closed series circuit consisting of the Mifsets Qz1 and Qd4 and the logic block LB when the Mifset Qd4 is rendered conductive by a pulse of the clock pulse train ϕ . Hence it is possible to reduce the power consumption of the circuit. The level of the output signal Vout is determined by the levels of the input signals VA to VC during the conduction period. That is, the logical relation

$$V_{out} = (V_A + V_B) \cdot V_C$$

is valid during the conduction period.

In a circuit according to the present invention, the number of transistors connected in series between the output terminal and the earth terminal is increased by one in comparison with the number of said transistors in a similar circuit constructed according to the EE system. However, the area occupied by the circuit elements of the present invention does not increase, and is reduced under some conditions.

The above-mentioned economy of circuit area is achieved because the EE system, a maximum of two transistors can be connected in series from the output terminal, whereas with the ED system, about four transistors can be connected in series from the output terminal, whilst still maintaining the same output level at the same operating speed. This advantage of the ED system operation can be explained quantitatively although such an explanation is not given herein.

Thus utilizing the ED system the current limiting Mifset can be connected in series with the logic block LB.

A second embodiment of the present invention is shown in Figure 2, this circuit being that of an AND—OR logic gate of a type often required for digital control circuits.

Referring to the Figure, the circuit includes six enhancement type Mifsets Qd5 to Qd10, two of said transistors comprising each of three logic blocks LB1 to LB3. Three depletion type Mifsets Qz2 to Qz4 are connected as the load elements of the respective logic blocks. Each of the logic blocks LB1 to LB3 is arranged to function as a two-input NAND circuit. Output signals derived from the logic blocks LB1 and LB2 are applied as inputs to the logic block LB3. Hence the output signal at the terminal Vout can be expressed by the logical expression:

$$V_{out} = (V_D \cdot V_E) \cdot (V_F \cdot V_G) = V_D \cdot V_E + V_F \cdot V_G.$$

The notable feature of the AND—OR circuit of Figure 2 is that a single Mifset Qd11 is connected commonly in series to all three logic blocks and thus the currents which flow through all three logic blocks are limited by the one transistor. Using this arrangement, the actual logical operations performed by the circuit conform to the above equation within a period equal to the width of a pulse of the clock pulse train ϕ which is applied to the transistor Qd11.

Thus, according to the embodiment of Figure 2, a single Mifset may be used to control conduction of a plurality of logic blocks. Hence the power consumption is reduced and the degree of integration of the circuit is increased. Said single Mifset must be capable of conducting a current which is the sum of the currents flowing through the logic blocks of the logic circuit to which the Mifset is connected. Consequently, said single Mifset must be made larger (i.e. lower in resistance) than the transistors constituting the logic blocks or alternatively instead of using a large single Mifset for current limiting a plurality of smaller Mifsets connected in parallel may be employed.

The circuit of a third embodiment according to the present invention is shown in Figure 3, this circuit being that of a two-phase two bit dynamic shift register.

Referring to Figure 3, four enhancement type Mifsets Qd12 to Qd15 are connected to four depletion type Mifsets Qz5 to Qz8, respectively operating as loads. An enhancement type Mifset Qd16 operating as a current limiter is connected in series with both the Mifsets Qd12 and Qd14, the gate electrode of the Mifset Qd16 being driven by the clock pulse train ϕ_1 as shown in Figure 4. A Mifset Qd17 is connected in series

with both the Misfets Qd13 and Qd15, the gate electrode of the Misfet Qd17 being driven by the clock pulse train $\phi 2$ (see Figure 4) which differs in phase from the clock pulse train $\phi 1$.

The Misfets Qz5, Qd12 and Qd16 constitute an inverter circuit. Similarly, the other Misfets of the circuit of Figure 3 (including Qd16) constitute three further inverter circuits. The four inverter circuits are connected serially via three enhancement type Misfets Qt1—Qt3 which operate as transfer gates. An output signal is derived from the final stage inverter circuit via a Misfet Qt4. To the gate electrodes of the Misfets Qt1 and Qt3 is applied the clock pulse train $\phi 1$, whilst to the gate electrodes of the Misfets Qt2 and Qt4 is applied the clock pulse train $\phi 2$. To the gate electrode of the Misfet Qd12 is applied an input signal V_{in} (see Figure 4) which is synchronized with the clock pulse train $\phi 2$.

The operation of the shift register constructed as described above and illustrated in Figure 3 will now be explained with reference to the waveform diagram of Figure 4. In Figure 4, the upper level of the signals is the logical "1" level (earth potential), and the lower level represents logical "0" (a negative potential).

When a pulse of the clock train $\phi 1$ goes to the logical "0" level thus rendering the Misfet Qd16 conductive, the signal output by the first inverter circuit which is the source potential V_1 of the Misfet Qz5 takes a level which corresponds to the input signal inverted,

i.e. V_{in} . Since the transfer Misfet Qt1 is simultaneously conductive the output signal V_1 is fed via the Misfet Qt1 to the Misfet Qd13, and is stored by the gate electrode capacitance of the Misfet Qd13. Similarly, when the clock pulse train $\phi 2$ goes to the logical "0" level thus rendering the Misfets Qd17 and Qt2 conductive, the complement of the signal stored in the Misfet Qd13 is written into the gate electrode capacitance of the Misfet Qd14. Thus, the gate electrode potential V_2 of the Misfet Qd13 corresponds to a signal being the complement of the input signal V_{in} delayed by the phase difference between the clock pulse trains $\phi 1$ and $\phi 2$, because the gate electrode potential V_2 is synchronized with the clock pulse train $\phi 1$ and the input signal V_{in} is synchronized with the clock pulse train $\phi 2$. Since the periods of the clock pulses $\phi 1$ and $\phi 2$ are equal, the gate electrode potential V_4 of the Misfet Qd14 ultimately becomes equal to a signal corresponding to the input signal V_{in} delayed by one period (one bit) of the clock pulse trains $\phi 1$ or $\phi 2$. This can be seen from the waveform diagrams in Figure 4.

As illustrated in Figure 4, the output potential V_1 of the first inverter is driven to the

logical "0" level irrespective of the input signal applied to the circuit when a pulse of the clock pulse train $\phi 1$ is held at the logical "1" level. Only when such a clock pulse falls to the logical "0" level is the output potential V_1 transferred via the Misfet Qt1 to the Misfet Qd13 and written into the gate capacitance thereof. The gate potential V_2 is therefore maintained at the correct level corresponding to the value of the output potential V_1 until a pulse of the clock pulse train $\phi 1$ subsequently goes to the logical "0" level. For a similar reason, the period during which the output potential V_1 is at the correct level is equal to the pulse width of the clock pulse train $\phi 1$, and is shorter than the period of the input signal V_{in} . However, this is not disadvantageous since the period during which the gate electrode potential V_2 is at the correct level becomes equal to the period of the clock pulse train $\phi 1$.

In the above described manner, the period during which the output signal derived from each logic block of the circuit of Figure 3 is at the correct logical level is reduced to correspond to the pulse width of a clock pulse. If it is necessary to correct the pulse width of a signal the logic circuit of Figure 1, for example may be used and the signal is fed from the logic block LB of Figure 1 to the next stage of the logical circuit via a transfer Misfet which is triggered by the clock pulse train ϕ .

The shift register described above has the following advantages.

1. The power consumption is low.
2. The number of transistors employed to lower the power consumption can be made fewer than the number of logic blocks of the logical element.

WHAT WE CLAIM IS:—

1. A logical circuit comprising a plurality of Misfet transistors (as hereinbefore defined) and wherein a Misfet acting as a load is of the depletion type, including the series connection of, firstly said depletion type Misfet, secondly a Misfet logic circuit block constructed so as to satisfy a required logical expression, and thirdly a further Misfet, the conduction of said further Misfet being controlled by a clock pulse train and said logic circuit block having first and second terminals serving to connect it respectively to the load Misfet and the further Misfet.
2. A logical circuit according to Claim 1, wherein the drain electrode of said depletion type Misfet is connected to a first terminal of a power supply, the source and gate electrodes thereof being commonly connected to an output terminal of the circuit and to the first terminal of said logic circuit block.
3. A logical circuit according to Claim 2, whereof the source electrode of said further Misfet, the conduction of which is controlled



with both the Misfets Qd13 and Qd15, the gate electrode of the Misfet Qd17 being driven by the clock pulse train ϕ_2 (see Figure 4) which differs in phase from the clock pulse train ϕ_1 .

The Misfets Qz5, Qd12 and Qd16 constitute an inverter circuit. Similarly, the other Misfets of the circuit of Figure 3 (including Qd16) constitute three further inverter circuits. The four inverter circuits are connected serially via three enhancement type Misfets Qt1—Qt3 which operate as transfer gates. An output signal is derived from the final stage inverter circuit via a Misfet Qt4. To the gate electrodes of the Misfets Qt1 and Qt3 is applied the clock pulse train ϕ_1 , whilst to the gate electrodes of the Misfets Qt2 and Qt4 is applied the clock pulse train ϕ_2 . To the gate electrode of the Misfet Qd12 is applied an input signal Vin (see Figure 4) which is synchronized with the clock pulse train ϕ_2 .

The operation of the shift register constructed as described above and illustrated in Figure 3 will now be explained with reference to the waveform diagram of Figure 4. In Figure 4, the upper level of the signals is the logical "1" level (earth potential), and the lower level represents logical "0" (a negative potential).

When a pulse of the clock train ϕ_1 goes to the logical "0" level thus rendering the Misfet Qd16 conductive, the signal output by the first inverter circuit which is the source potential V1 of the Misfet Qz5 takes a level which corresponds to the input signal inverted,

i.e. Vin. Since the transfer Misfet Qt1 is simultaneously conductive the output signal V1 is fed via the Misfet Qt1 to the Misfet Qd13, and is stored by the gate electrode capacitance of the Misfet Qd13. Similarly, when the clock pulse train ϕ_2 goes to the logical "0" level thus rendering the Misfets Qd17 and Qt2 conductive, the complement of the signal stored in the Misfet Qd13 is written into the gate electrode capacitance of the Misfet Qd14. Thus, the gate electrode potential V2 of the Misfet Qd13 corresponds to a signal being the complement of the input signal Vin delayed by the phase difference between the clock pulse trains ϕ_1 and ϕ_2 , because the gate electrode potential V2 is synchronized with the clock pulse train ϕ_1 and the input signal Vin is synchronized with the clock pulse train ϕ_2 . Since the periods of the clock pulses ϕ_1 and ϕ_2 are equal, the gate electrode potential V4 of the Misfet Qd14 ultimately becomes equal to a signal corresponding to the input signal Vin delayed by one period (one bit) of the clock pulse trains ϕ_1 or ϕ_2 . This can be seen from the waveform diagrams in Figure 4.

As illustrated in Figure 4, the output potential V1 of the first inverter is driven to the

logical "0" level irrespective of the input signal applied to the circuit when a pulse of the clock pulse train ϕ_1 is held at the logical "1" level. Only when such a clock pulse falls to the logical "0" level is the output potential V1 transferred via the Misfet Qt1 to the Misfet Qd13 and written into the gate capacitance thereof. The gate potential V2 is therefore maintained at the correct level corresponding to the value of the output potential V1 until a pulse of the clock pulse train ϕ_1 subsequently goes to the logical "0" level. For a similar reason, the period during which the output potential V1 is at the correct level is equal to the pulse width of the clock pulse train ϕ_1 , and is shorter than the period of the input signal Vin. However, this is not disadvantageous since the period during which the gate electrode potential V2 is at the correct level becomes equal to the period of the clock pulse train ϕ_1 .

In the above described manner, the period during which the output signal derived from each logic block of the circuit of Figure 3 is at the correct logical level is reduced to correspond to the pulse width of a clock pulse. If it is necessary to correct the pulse width of a signal the logic circuit of Figure 1, for example may be used and the signal is fed from the logic block LB of Figure 1 to the next stage of the logical circuit via a transfer Misfet which is triggered by the clock pulse train ϕ .

The shift register described above has the following advantages.

1. The power consumption is low.
2. The number of transistors employed to lower the power consumption can be made fewer than the number of logic blocks of the logical element.

WHAT WE CLAIM IS:—

1. A logical circuit comprising a plurality of Misfet transistors (as hereinbefore defined) and wherein a Misfet acting as a load is of the depletion type, including the series connection of, firstly said depletion type Misfet, secondly a Misfet logic circuit block constructed so as to satisfy a required logical expression, and thirdly a further Misfet, the conduction of said further Misfet being controlled by a clock pulse train and said logic circuit block having first and second terminals serving to connect it respectively to the load Misfet and the further Misfet.

2. A logical circuit according to Claim 1, wherein the drain electrode of said depletion type Misfet is connected to a first terminal of a power supply, the source and gate electrodes thereof being commonly connected to an output terminal of the circuit and to the first terminal of said logic circuit block.

3. A logical circuit according to Claim 2, whereof the source electrode of said further Misfet, the conduction of which is controlled

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by a clock pulse train, is connected to a second terminal of said power supply, the drain electrode thereof is connected to the second terminal of said logic circuit block and the gate electrode thereof is connected to the clock pulse train source.

4. A logical circuit according to any one of the preceding Claims, wherein said logic circuit block includes three Misfet transistors, the source electrodes of the first and second of said transistors being commonly connected to one terminal of said logic circuit block, the source electrode of the third of said transistors being connected to the drain electrode of the first of said transistors, and the drain electrodes of said second and third transistors are commonly connected to the other terminal of said logic circuit block.

5. A logical circuit according to any one of the preceding Claims 1 to 3, including in addition to and connected in parallel with said logic circuit block and depletion type Misfet one or more further circuits, each circuit being the series combination of a depletion type Misfet and a logic circuit block.

6. A logical circuit according to Claim 5, wherein there are included two of said further circuits, and wherein three logic circuit blocks of the resulting logical circuit are each comprised by two Misfets connected in parallel at their source and drain electrodes between the terminals of said logic circuit blocks respectively and arranged to receive input signals applied to their gates.

7. A logical circuit according to Claim 6, wherein the three logic circuit blocks are inter-connected, the output of the first logic circuit block being connected to a first input of the third logic circuit block and the output of the second logic circuit block being connected to a second input of the third logic circuit block.

8. A logical circuit according to any one of Claims 1 to 3, wherein said logic circuit block is a Misfet, the gate electrode of which is arranged to receive an input, the drain electrode of which is connected to one terminal of said logic circuit block, and the source electrode of which is connected to the other terminal of said logic circuit block.

9. A logical circuit including two logic circuit blocks according to Claim 8, the first

of said logic circuit blocks being controlled by said first clock pulse train and the second of said logic circuit blocks being controlled by a second clock pulse train phase shifted from said first clock pulse train.

10. A logical circuit according to Claim 9, further including, in each of said two logic circuit blocks, and connected in parallel with the series connection of said logic circuit block and said depletion type load Misfet one more additional series circuit comprising a logic circuit block and a depletion type load resistance.

11. A logical circuit according to Claim 10, wherein the output of a first one of said logic circuit blocks, said circuit block being controlled by said first clock pulse train, is applied as an input to a second of said logic circuit blocks which are controlled by the second said clock pulse train via a first gate Misfet, conduction of which is controlled by said first clock pulse train, the output of said second logic circuit block being applied as an input to a third logic circuit block controlled by said first clock pulse train via a second gate Misfet, conduction of which is controlled by said second clock pulse train, the output of said third logic circuit block controlled by said first clock pulse train being applied as an input to a fourth logic circuit block which is controlled by said second clock pulse train via a third gate Misfet, conduction of which is controlled by said first clock pulse train, the output of said fourth logic circuit block controlled by said second clock pulse train being controlled by a fourth gate Misfet, conduction of which is controlled by said second clock pulse train.

12. A logical circuit constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figure 1, or Figure 2, or Figure 3 of the accompanying drawings.

MEWBURN ELLIS & CO.,
Chartered Patent Agents,
70—72 Chancery Lane,
London, W.C.2.
Agents for the Applicants.

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