(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 July 2004 (29.07.2004)

PCT

(10) International Publication Number
WO 2004/063916 A3

(51) International Patent Classification[7]: G06F 1/32, 1/32, G11C 11/406

(21) International Application Number: PCT/US2004/000092

(22) International Filing Date: 2 January 2004 (02.01.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/340,020 9 January 2003 (09.01.2003) US

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: **SAMSON, Eric**; P.O. Box 963, Folsom, CA 95763 (US). **NAVALE, Aditya**; 4215 Flushing Place, El Dorado Hills, CA 95762 (US). **JENSEN, Sam**; 8842 Winding Way, #634, Fair Oaks, CA 95628 (US). **SRITAN-YARATANA, Siripong**; 3280 Santa Sophia Court, Union City, CA 94587 (US). **CHENG, Win**; 21567 Rosario Avenue, Cupertino, CA 95014 (US).

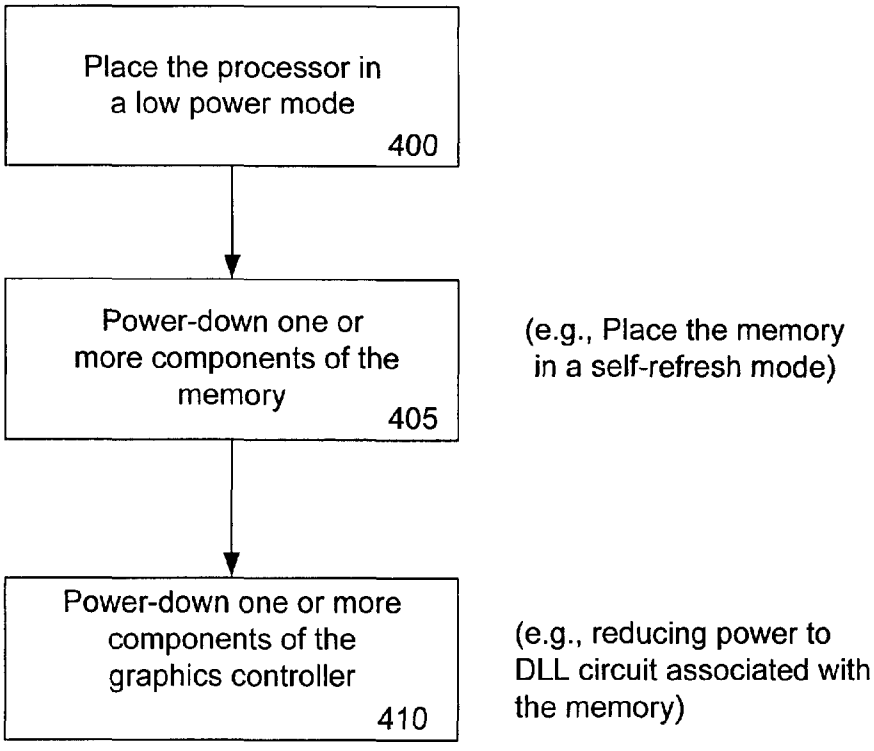
(74) Agents: **MALLIE, Michael, J.** et al.; Blakely, Sokoloff, Taylor & Zafman, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR,

[Continued on next page]

(54) Title: MEMORY CONTROLLER CONSIDERING PROCESSOR POWER STATES



(57) Abstract: When a processor in a computer system is placed in a low power mode, power consumption of the computer system may be further reduced by reducing power consumption of one or more components of a memory coupled to the processor and by reducing power consumption of one or more components of a controller device coupled to the memory. The processor and the controller device may share the memory.

WO 2004/063916 A3

GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

(88) Date of publication of the international search report:
14 April 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.