ABSTRACT

SELECTIVE CVD TiSi2 DEPOSITION WITH TiSi2 LINER

A method for improving the quality and uniformity of a silicide film in the fabrication of a silicided polysilicon gate and source/drain regions in an integrated circuit device is described. A polysilicon gate electrode is provided on the surface of a semiconductor substrate. Source and drain regions are formed within the semiconductor substrate adjacent to the gate electrode. A layer of titanium is deposited over the surfaces of the substrate. The substrate is annealed whereby the titanium layer is transformed into a first titanium silicide layer except where the titanium layer overlies the spacers. The titanium layer overlying the spacers is stripped to leave the first titanium silicide layer only on the top surface of the gate electrode and on the top surface of the semiconductor substrate overlying the source and drain regions. A second titanium silicide layer is selectively deposited on the first titanium silicide layer to complete formation of the silicided gate electrode and source and drain regions in the fabrication of an integrated circuit device. The first titanium silicide layer reduces or eliminates the effect of the polysilicon and silicon surface effects allowing for a higher quality and more uniform second titanium silicide layer.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)