

ABSTRACT

LAYERED CAPACITOR DEVICE

5 A layered capacitor device with high capacitance per unit area is realised
by alternating in the vertical direction first layers (FL1, FL2, FL3, FL4, FL5) and
second layers (SL1, SL2, SL3, SL4). A first layer (FL2) consists of horizontally
alternating electrically conducting tracks (T2,2; T2,3) and electrically insulating
tracks, whereas a second layer consists of electrically insulating material, e.g. an
10 oxide. In this way top-bottom capacitors (C_{TB}) and side-wall capacitors (C_{SW}) are
constituted that are parallel coupled to form the layered capacitor device. In a
preferred embodiment of the invention, this parallel coupling is realised by
conductively interconnecting diagonally neighbouring electrically conducting
tracks (T1,2; T2,3).

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