

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
17 March 2022 (17.03.2022)



(10) International Publication Number
WO 2022/055860 A1

(51) International Patent Classification:
G05F 1/56 (2006.01) *H02M 7/02* (2006.01)
C25D 21/12 (2006.01)

(21) International Application Number:
PCT/US2021/049252

(22) International Filing Date:
07 September 2021 (07.09.2021)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
17/015,612 09 September 2020 (09.09.2020) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventor: **BORJESSON, Mikael R.**; 3050 Bowers Avenue, Santa Clara, California 95054 (US).

(74) Agent: **BERGSTROM, James T.** et al.; 1100 Peachtree Street NE, Suite 2800, Mailstop: IP Docketing - 22, Atlanta, California 30309 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) Title: ELECTROPLATING CONTROLLER WITH POWER BASED HEAD-ROOM CONTROL

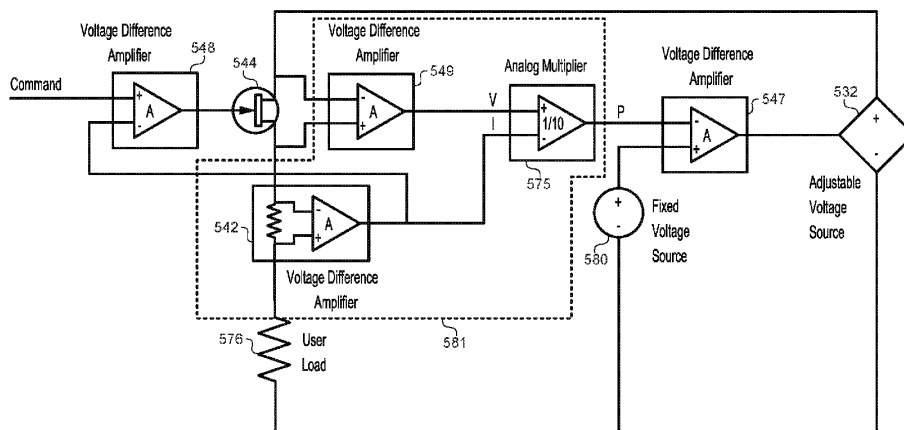


FIG. 5

(57) Abstract: A method of controlling a headroom voltage of a transistor stage of an electroplating system to maintain a target power dissipation across the transistor stage may include maintaining a headroom voltage in the transistor stage for a load in the electroplating system. The method may also include measuring an instantaneous power dissipation in the transistor stage and generating a difference output representing a difference between the instantaneous power dissipation in the transistor stage and the target power dissipation in the transistor stage. A voltage across the transistor stage and the load may then be adjusted using the difference output such that the headroom voltage in the transistor stage is adjusted to maintain the target power dissipation in the transistor stage.

[Continued on next page]

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to the identity of the inventor (Rule 4.17(i))*
- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*