What is claimed is:

1. A semiconductor device comprising:

an active pattern which includes:

a lower pattern extending in a first direction, and

a plurality of sheet patterns spaced apart from the lower pattern in a third direction perpendicular to an upper surface of the lower pattern, each of the plurality of sheet patterns including an upper surface and a lower surface opposite to each other in the third direction;

a gate structure which extends in a second direction and is disposed on the lower pattern and includes a gate electrode and a gate insulating film, the gate electrode and the gate insulating film surrounding each of the plurality of sheet patterns; and

a source/drain pattern which is disposed on at least one side of the gate structure,

wherein the gate structure includes a plurality of inter-gate structures,

wherein a lowermost inter-gate structure of the plurality of inter-gate structures is disposed between the lower pattern and a lowermost sheet pattern of the plurality of sheet patterns,

wherein each of other inter-gate structures of the plurality of inter-gate structures is between two sheet patterns, adjacent to each other in the third direction, of the plurality of sheet patterns,

wherein the gate structure contacts the source/drain pattern,

wherein the gate insulating film includes:

a horizontal portion extending along an upper surface of each sheet pattern of the plurality of sheet patterns and a lower surface of each sheet pattern of the plurality of sheet patterns, and

a first vertical portion extending along the source/drain pattern, and

wherein a thickness, in the third direction, of the horizontal portion of the gate insulating film is smaller than a thickness, in the first direction, of the first vertical portion of the gate insulating film.

2. The semiconductor device of claim 1,

wherein the gate insulating film includes an interfacial insulating film and a high-dielectric constant insulating film,

wherein the high-dielectric constant insulating film is disposed between the interfacial insulating film and the gate electrode, and

wherein a thickness, in the third direction, of the interfacial insulating film in the horizontal portion of the gate insulating film is different from a thickness, in the first direction, of the interfacial insulating film in the first vertical portion of the gate insulating film.

3. The semiconductor device of claim 2,

wherein the thickness, in the third direction, of the interfacial insulating film in the horizontal portion of the gate insulating film is smaller than the thickness, in the first direction, of the interfacial insulating film in the first vertical portion of the gate insulating film.

4. The semiconductor device of claim 1,

wherein each of the plurality of sheet patterns includes side walls,

wherein in each of the plurality of sheet patterns, the side walls connect the upper surface to the lower surface,

wherein the gate insulating film includes a second vertical portion extending along the side walls of each of the plurality of sheet patterns, and

wherein the thickness, in the third direction, of the horizontal portion of the gate insulating film is smaller than a thickness, in the second direction, of the second vertical portion of the gate insulating film.

5. The semiconductor device of claim 4,

wherein the gate insulating film includes an interfacial insulating film and a high-dielectric constant insulating film,

wherein the high-dielectric constant insulating film is disposed between the interfacial insulating film and the gate electrode, and

wherein a thickness, in the third direction, of the interfacial insulating film in the horizontal portion of the gate insulating film is smaller than a thickness, in the second direction, of the interfacial insulating film in the second vertical portion of the gate insulating film.

6. The semiconductor device of any one of claims 1 to 3,

wherein each of the plurality of sheet patterns includes side walls,

wherein in each of the plurality of sheet patterns, the side walls connect the upper surface to the lower surface,

wherein the gate insulating film includes a second vertical portion extending along the side walls of each of the plurality of sheet patterns, and

wherein the thickness, in the third direction, of the horizontal portion of the gate insulating film is equal to a thickness, in the second direction, of the second vertical portion of the gate insulating film.

7. The semiconductor device of any one of claims 1 to 6,

wherein the source/drain pattern includes a plurality of width expansion regions that are spaced apart from each other in the third direction,

wherein each of the plurality of width expansion regions has curved sidewalls, and

wherein a width of each of the plurality of width expansion regions, in the first direction, between the curved sidewalls varies when the width is measured along a straight line extending in the third direction away from the upper surface of the lower pattern.

8. The semiconductor device of claim 7,

wherein the plurality of width expansion regions have maximum widths at regions between the lower pattern and the lowermost sheet pattern of the plurality of sheet patterns, and between two adjacent sheet patterns, in the third direction, of the plurality of sheet patterns.

9. The semiconductor device of any one of claims 1 to 7,

wherein the plurality of inter-gate structures include a first inter-gate structure and a second inter-gate structure,

wherein the plurality of sheet patterns include a first sheet pattern disposed between the first inter-gate structure and the second inter-gate structure,

wherein the first sheet pattern includes a boundary surface that is in contact with the source/drain pattern, and

wherein a part of the first inter-gate structure and a part of the second inter-gate structure protrude toward the source/drain pattern from the boundary surface of the first sheet pattern.

10. The semiconductor device of any one of claims 1 to 8,

wherein the plurality of inter-gate structures include a first inter-gate structure and a second inter-gate structure disposed between adjacent sheet patterns, and

wherein a width, in the first direction, of the first inter-gate structure is equal to a width, in the first direction, of the second inter-gate structure.

11. The semiconductor device of any one of claims 1 to 8,

wherein the plurality of inter-gate structures include first to third inter-gate structures sequentially disposed on the lower pattern,

wherein a width of the second inter-gate structure in the first direction is smaller than a width of the first inter-gate structure in the first direction, and

wherein the width of the second inter-gate structure in the first direction is smaller than a width of the third inter-gate structure in the first direction.

12. A semiconductor device comprising:

an active pattern which includes:

a lower pattern extending in a first direction, and

a plurality of sheet patterns spaced apart from the lower pattern in a third direction perpendicular to an upper surface of the lower pattern, each of the plurality of sheet patterns including an upper surface and a lower surface opposite to each other in the third direction;

a gate structure which extends in a second direction and is disposed on the lower pattern and includes a gate electrode and a gate insulating film, the gate electrode and the gate insulating film surrounding each of the plurality of sheet patterns; and

a source/drain pattern which is disposed on at least one side of the gate structure,

wherein the gate structure includes a plurality of inter-gate structures,

wherein a lowermost inter-gate structure of the plurality of inter-gate structures is disposed between the lower pattern and a lowermost sheet pattern of the plurality of sheet patterns,

wherein each of other inter-gate structures of the plurality of inter-gate structures is disposed between corresponding two sheet patterns, adjacent to each other in the third direction, of the plurality of sheet patterns,

wherein the gate insulating film includes:

an interfacial insulating film, and

a high-dielectric constant insulating film disposed between the interfacial insulating film and the gate electrode,

wherein the interfacial insulating film includes:

a horizontal portion extending along an upper surface of each of the plurality of sheet patterns and a lower surface thereof, and

a first vertical portion extending along the source/drain pattern, and

wherein a thickness, in the third direction, of the horizontal portion of the interfacial insulating film is different from a thickness, in the first direction, of the first vertical portion of the interfacial insulating film.

13. The semiconductor device of claim 12,

wherein the thickness, in the third direction, of the horizontal portion of the interfacial insulating film is smaller than the thickness, in the first direction, of the first vertical portion of the interfacial insulating film.

14. The semiconductor device of claim 12 or claim 13,

wherein the interfacial insulating film contacts the source/drain pattern.

15. The semiconductor device of any one of claims 12 to 14,

wherein the first vertical portion of the interfacial insulating film includes:

a first region contacting the source/drain pattern, and

a second region disposed on the first region of the first vertical portion of the interfacial insulating film,

wherein the source/drain pattern is doped with a first element other than silicon, and

wherein a concentration of the first element in the first region of the first vertical portion of the interfacial insulating film is higher than a concentration of the first element in the second region of the first vertical portion of the interfacial insulating film.

16. The semiconductor device of any one of claims 12 to 15,

wherein each of the plurality of sheet patterns includes side walls,

wherein in each of the plurality of sheet patterns, the side walls connect the upper surface to the lower surface,

wherein the interfacial insulating film includes a second vertical portion extending along the side walls of each of the plurality of sheet patterns, and

wherein the thickness, in the third direction, of the horizontal portion of the interfacial insulating film is smaller than a thickness, in the second direction, of the second vertical portion of the interfacial insulating film.

17. A semiconductor device comprising:

an active pattern which includes:

a lower pattern extending in a first direction, and

a plurality of sheet patterns spaced apart from the lower pattern in a third direction

perpendicular to an upper surface of the lower pattern, each of the plurality of sheet patterns including an upper surface and a lower surface opposite to each other in the third direction;

a gate structure which extends in a second direction and is disposed on the lower pattern and includes a gate electrode and a gate insulating film, the gate electrode and the gate insulating film surrounding each of the plurality of sheet patterns;

a gate spacer disposed on opposite side walls of the gate structure; and

a source/drain pattern which is disposed on at least one side of the gate structure,

wherein the gate insulating film includes:

an interfacial insulating film, and

a high-dielectric constant insulating film disposed between the interfacial insulating film and the gate electrode,

wherein the interfacial insulating film does not extend along side walls of the gate spacer,

wherein the high-dielectric constant insulating film extends along the side walls of the gate spacer,

wherein the interfacial insulating film includes:

a horizontal portion extending along an upper surface of each of the plurality of sheet patterns and a lower surface thereof, and

a first vertical portion extending along the source/drain pattern and contacting the source/drain pattern, and

wherein a thickness, in the third direction, of the horizontal portion of the interfacial insulating film is different from a thickness, in the first direction, of the first vertical portion of the interfacial insulating film.

18. The semiconductor device of claim 17,

wherein each of the plurality of sheet patterns includes side walls,

wherein in each of the plurality of sheet patterns, the side walls connect the upper surface to the lower surface,

wherein the interfacial insulating film includes a second vertical portion extending along the side walls of each of the plurality of sheet patterns, and

wherein the thickness, in the third direction, of the horizontal portion of the interfacial insulating film is smaller than a thickness, in the second direction, of the second vertical portion of the interfacial insulating film.

19. The semiconductor device of claim 17,

wherein each of the plurality of sheet patterns includes side walls,

wherein in each of the plurality of sheet patterns, the side walls connect the upper surface to the lower surface,

wherein the interfacial insulating film includes a second vertical portion extending along the side walls of each of the plurality of sheet patterns, and

wherein the thickness, in the third direction, of the horizontal portion of the interfacial insulating film is equal to a thickness, in the second direction, of the second vertical portion of the interfacial insulating film.