

A FINITE ELEMENT SIMULATION METHOD TO PREDICT THE FILM THICKNESS
PROFILE FROM ZONAL SHOPED

CROSS-REFERENCES

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] Semiconductor manufacturing typically involves one or more processes to deposit and pattern a structure on a wafer. As the complexity and/or non-uniformity of the structure and/or materials on or across the wafer increase, stress applied to the wafer can cause wafer deformation (e.g., bowing, twisting, etc.) impacting various aspects from structure formation to product yield. For example, in three-dimensional NOT-AND logic gate (3D-NAND) structure fabrication, multi-stacked films with thick, high stress carbon-based hard masks, metallization patterns, and substrate trenches can cause significant wafer warpage, leading to issues such as frontside lithographic overlay mismatches, wafer bow beyond chucking limits of an electrostatic chuck, etc.

[0003] The background provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent that it is described in this background, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the disclosure.

SUMMARY

[0004] Disclosed herein are methods and systems of modelling deposition profiles of films. In one aspect of the embodiments herein, a computer program product is provided, the computer program product including a non-transitory computer readable medium having computer-executable instructions for: (a) receiving parameter values for a plurality of parameters of a semiconductor device fabrication process to deposit a non-uniform profile film on a substrate, wherein the semiconductor device fabrication process is performed by a process chamber having a showerhead with a plurality of zones; (b) performing a simulation of the semiconductor device fabrication process based on the parameter values; and (c) determining a deposition profile of the non-uniform profile film based on the simulation. In some embodiments, the plurality of parameters includes a showerhead design. In some embodiments, the simulation is performed using a model for curved-bar profile films. In some embodiments, the simulation is performed using a model for curved-channel profile films. In some embodiments, the simulation is performed

using a model for silicon nitride films. In some embodiments, the simulation is performed using a model for silicon oxide films. In some embodiments, including additional computer-executable instructions for determining a concentration field of precursor radicals and an electron density field at the substrate surface during the semiconductor device fabrication process, wherein the deposition profile is based on the concentration field of precursor radicals and the electron density field at the substrate surface. In some embodiments, the electron density field represents hot electrons. In some embodiments, the plurality of parameters includes RF power. In some embodiments, the plurality of parameters includes RF power. In some embodiments, the plurality of parameters includes pressure. In some embodiments, a first parameter value for a first parameter for a first zone of the plurality of zones is different from a second parameter value for the first parameter for a second zone of the plurality of zones. In some embodiments, the first parameter is a flow rate. In some embodiments, the first parameter is a concentration of precursor species. In some embodiments, the non-uniform profile film includes silicon oxide or silicon nitride.

[0005] In another aspect of the embodiments herein, a method is provide, including: (a) receiving parameter values for a plurality of parameters of a semiconductor device fabrication process to deposit a non-uniform profile film on a substrate, wherein the semiconductor device fabrication process is performed by a process chamber having a showerhead with a plurality of zones; (b) performing a simulation of the semiconductor device fabrication process based on the parameter values; and (c) determining a deposition profile of the non-uniform profile film based on the simulation.

[0006] These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0007] Figures 1A and 1B show examples of unbowed and bowed semiconductor wafers on an electrostatic chuck.

[0008] Figure 2 shows an example isometric view of anisotropic wafer bow.

[0009] Figure 3A illustrates exemplary zones for depositing films having a curved bar profile and a curved channel profile on a backside of a wafer according to various embodiments herein.

[0010] Figures 3B and 3C illustrate a side view and exploded side view of a wafer having backside layers having a curved bar profile and a curved channel profile according to various embodiments herein.

[0011] Figures 3D-3G illustrate side views of a wafer having alternating stack of backside layers having a curved bar profile and a curved channel profile according to various embodiments herein.

[0012] Figure 4A-B present isometric and overhead views of a showerhead pedestal according to various embodiments herein.

[0013] Figure 5 is a process flow diagram illustrating certain operation in semiconductor wafer processing.

5 [0014] Figures 6A and 6B show a block diagram of an example substrate processing system.

[0015] Figure 7A shows an example cross section of an edge of a shower-pedestal.

[0016] Figure 7B shows a top view of an example carrier ring.

[0017] Figure 8 shows a schematic of an example process system that may be used to perform the methods described herein.

10 [0018] Figure 9 presents example data illustrating the effects of high-frequency (HF) power on deposition profiles.

DETAILED DESCRIPTION

Terminology

[0019] The following terms are used throughout the instant specification:

15 [0020] The terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate” and “partially fabricated integrated circuit” may be used interchangeably. Those of ordinary skill in the art understand that the term “partially fabricated integrated circuit” can refer to a semiconductor wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm.

20 Examples of wafer materials include silicon (Si), gallium arsenide (GaAs), and silicon germanium (SiGe). Besides semiconductor wafers, other workpieces that may take advantage of the disclosed embodiments include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, display devices or components such as backplanes for pixelated display devices, flat panel displays, micro-mechanical devices and the

25 like. The workpiece may be of various shapes, sizes, and materials.

[0021] A “semiconductor device fabrication operation” as used herein is an operation performed during fabrication of semiconductor devices. Typically, the overall fabrication process includes multiple semiconductor device fabrication operations, each performed in its own semiconductor fabrication tool such as a plasma reactor, an electroplating cell, a chemical mechanical

30 planarization tool, a wet etch tool, and the like. Categories of semiconductor device fabrication operations include subtractive processes, such as etch processes and planarization processes, and material additive processes, such as deposition processes (e.g., physical vapor deposition,

chemical vapor deposition, atomic layer deposition, electrochemical deposition, electroless deposition). In the context of etch processes, a substrate etch process includes processes that etch a mask layer or, more generally, processes that etch any layer of material previously deposited on and/or otherwise residing on a substrate surface. Such an etch process may etch a stack of layers in the substrate.

[0022] “Manufacturing equipment” refers to equipment in which a manufacturing process takes place. Manufacturing equipment often has a process chamber in which the workpiece resides during processing. Typically, when in use, manufacturing equipment performs one or more semiconductor device fabrication operations. Examples of manufacturing equipment for semiconductor device fabrication include deposition reactors such as electroplating cells, physical vapor deposition reactors, chemical vapor deposition reactors, and atomic layer deposition reactors, and subtractive process reactors such as dry etch reactors (e.g., chemical and/or physical etch reactors), wet etch reactors, and ashers.

[0023] “Wafer bow” as used herein may refer to a deformation of a wafer. The deformation may have radial and/or azimuthal components. Examples of types of wafer bow include dome shapes, bowl shapes, and saddle shapes. Wafer bow may occur during fabrication, for example, as a result of stress to the wafer during deposition of materials on an active surface of a wafer. Wafer bow may occur during various types of fabrication, such as when large stacks of materials are deposited. Wafer bow may cause complications in subsequent processing steps. For example, the wafer may fail to chuck correctly if an amount of bowing is too large, which may subject the wafer to nonuniform heating and/or other process conditions. Moreover, some processing steps (e.g., photolithography) may produce poor results if performed on a wafer that is excessively bowed.

[0024] In some embodiments, wafer bow may be measured as a deviation of the mean or median distance of the surface of the wafer to a reference plane. In some embodiments, the point of the median surface of the wafer may be the center point (e.g., in the case of concave or domed bowing), or an edge point of the wafer and/or an average edge point of the wafer (e.g., in the case of warping or convex bowing). In some embodiments wafer bow may be measured from a reference plane such that when an edge point of the wafer is below the reference plane the edge point is considered to have a negative bow, and when the edge point of the wafer is above the reference plane the edge point is considered to have a positive bow. In some embodiments, positive or negative bow may be measured along a z axis perpendicular to the reference plane.

[0025] In some embodiments, wafer bow may vary between the two principal planar directions of a substrate, which are referred to as the x and y directions. For example, wafer bow along the

x direction may be in a positive z direction while wafer bow along the y direction may be in a negative z direction (the z axis being perpendicular to a plane formed by the planar x and y directions). When bowing is positive along the x and y directions, a bowl shape is formed, while when bowing is negative in the x and y directions, an umbrella or dome shape is formed. Other shapes include a “half pipe” or “taco” shape when there is substantially no wafer bow in one direction while a positive or negative bow in the planar perpendicular direction. When wafer bow is positive in one direction and negative in another direction, a “saddle” or “potato chip” shape is formed.

[0026] Wafer bowing may be characterized by x-bow and y-bow values. A positive x-bow value corresponds to bowing of the wafer in a positive z-direction at a coordinate of the wafer having a large x-value and a small or zero y-value, e.g., an x-value greater than about 100 mm or of about 150 mm (for a 300 mm wafer) and a y-value of about 0 mm (where the reference point is at a center of the wafer). A negative x-bow value similarly corresponds to bowing of the wafer in a negative z-direction at a coordinate of the wafer having a large x-value and a small or zero y-value. Conversely, a positive y-bow and negative y-bow correspond to bowing of the wafer in positive or negative z-directions, respectively, at a coordinate of the wafer having a large y-value and a small or zero x-value.

[0027] In some embodiments, wafer bow may be characterized by a single value. In some embodiments, wafer bow may be described as a “delta bow.” When referring to wafer bow of saddle-shaped wafers, the wafer delta bow may be expressed in terms of a difference between the negative-bow in one direction (such as along the x-axis) and positive-bow in another direction (such as along the y-axis). For example, a wafer bow of 200 μm may result from an x-bow of -25 μm and a y-bow of +175 μm . For wafers having a taco, bowl, or dome-shaped wafer bow, wafer bow may refer to a difference between the maximum bow and a reference plane as described above.

[0028] A “curved bar profile” is characterized by a two-dimensional shape that has a varying thickness along one of the two principal planar dimensions of a substrate, which are referred to as the x and y directions. While the thickness varies in one of these two directions, it does not substantially vary in the other direction. Further, the curved bar profile means that the thickness of the layer is generally thicker toward the center of the substrate than the edges of the substrate. Hence the structure appears like a bar or “speed bump” on the backside of the substrate. In some cases, the curved bar profile varies in the direction away from the plane of the substrate (the z-direction) as a function of x-axis position, but without significantly varying in the y-axis position. In other cases, the curved bar profile varies in the z direction as a function of y-axis position, but

without significantly varying in the x-axis position. In certain embodiments, a curved bar is disposed along a principal axis of the substrate such that a centerline of the bar passes through the origin (center point) of the substrate. Thus, the curved bar profile may be characterized by a film having greater thickness in the center of the substrate than the edge of the substrate. The curved shape may be generally rounded such a circular, parabolic, gaussian, etc. In some embodiments the shape may be characterized by a parabolic or polynomial function.

[0029] A “curved channel profile” is characterized by a two-dimensional shape that has a varying thickness along one of the x and y directions of the substrate, which are referred to as the x and y directions. While the thickness varies in one of these two directions, it does not substantially vary in the other direction. Further, the curved bar profile means that the thickness of the layer is generally thicker toward the edges of the substrate than the center of the substrate. Hence the structure appears like a channel or indentation on the backside of the substrate. In some cases, the curved channel profile varies in the direction away from the plane of the substrate (the z-direction) as a function of x-axis position, but without significantly varying in the y-axis position. In other cases, the curved channel profile varies in the z direction as a function of y-axis position, but without significantly varying in the x-axis position. In certain embodiments, a curved channel is disposed along a principal axis of the substrate such that a centerline of the channel passes through the origin (center point) of the substrate. Thus, the curved channel profile may be characterized by a film having greater thickness at the edges of the substrate than the center of the substrate. The curved shape may be generally rounded such as a circular, parabolic, gaussian, etc. In some embodiments the shape may be characterized by a parabolic or polynomial function.

[0030] Generally, the curved bar and curved channel profiles refer to geometries of the films’ varying properties. Frequently, the film property is film thickness, but other properties can similarly assume the profiles. Such properties may include film density, film composition, film internal stress, etc. Examples of a curved bar profile and a curved channel profile are illustrated in Figures 3B and 3C. Film 308 is an example of a curved bar profile, while film 307 is an example of a curved channel profile. A curved bar profile film and a curved channel profile film may also be referred to as non-uniform thickness profile films. A non-uniform thickness profile film may refer to either of a curved bar profile film or a curved channel profile film.

[0031] A “uniform thickness profile” is characterized by a two-dimension shape that has a substantially non-varying thickness along any planar directions of a substrate, e.g., an x and y direction. In some embodiments, the combination of a curved channel profile film and a curved bar profile film may be a uniform thickness film. In some embodiments, a curved channel profile film and a curved bar profile film have complementary shapes that together may form a

substantially uniform thickness profile bilayer film. In some embodiments, the combination of a curved bar profile film and a curved channel profile film may be referred to as a stack of complementary profile films. In some embodiments, a non-uniform thickness profile may refer to either or both of a curved channel profile and a curved bar profile. In some embodiments, a stacked
5 film formed from combination of layers having a curved channel profile and layers of having a curved bar profile may be substantially flat, e.g., having a flatness similar to a single uniform thickness profile film deposited to a similar thickness as the combined non-uniform thickness profile films.

Bowed Wafers

10 [0032] Semiconductor device fabrication often involves deposition of a stack of layers or films on a wafer. Typically, most deposition and other processing to form the devices occurs on one side of the wafer, often referred to as the front face or frontside of a wafer. As the deposited layers build up, they can introduce stress in the wafer. A large net tensile or compressive stress can cause the wafer to bow (and potentially crack in case of excessive tensile stress), which is undesirable.

15 [0033] Bowing is especially likely to occur where large stacks of materials are deposited, for example, in the context of 3D-NAND devices, or where a thick frontside layer is deposited. Where bowing is significant, it can deleteriously affect subsequent processing steps. For instance, the wafer may fail to chuck correctly if the bowing is too great. Figures 1A and 1B show a wafer on an electrostatic chuck, which typically have a flat surface. Figure 1A shows a wafer 102 on an
20 electrostatic chuck 110. When the wafer 102 is substantially flat for purposes of a particular process operation, e.g., having a bow of about 100 μm or less, the wafer may be properly clamped, securing the wafer for subsequent processing steps. Figure 1B shows a bowed wafer 104 on the electrostatic chuck 110. Wafer 104 is illustrated as having a negative wafer bow (i.e., a dome shape where the center point of the wafer is above the edge of the wafer). This may result from frontside
25 layers having a compressive internal stress. Frontside layers having a tensile internal stress may cause a wafer to bow in the opposite manner, having a bowl shape.

[0034] When the bow is significant, various manufacturing problems may arise. In some instances, the wafer may fail to secure properly on the electrostatic chuck. This may cause various nonuniformity issues—for example, the wafer may not be heated uniformly, the process gases
30 may not be applied to the wafer uniformly across the wafer, and/or the distance between the wafer and the showerhead and/or showerhead pedestal may not be maintained evenly in parallel (i.e., parallelism may be disrupted). Wafer bow may cause other problems. For example, certain processing steps (e.g., photolithography) are very precise and produce poor results if the wafer is not substantially flat. The problem may be manifest as lithography defocus. Cracking may also

occur, which can introduce additional defects, reducing yield.

[0035] One example stack that may cause these problems is a stack having alternating layers of oxide and nitride (e.g., silicon oxide/silicon nitride/silicon oxide/silicon nitride, etc.). Another example of a type of stack likely to cause bowing includes alternating layers of oxide and polysilicon (e.g., silicon oxide/polysilicon/silicon oxide/polysilicon, etc.). Other examples of stack materials that may be problematic include, but are not limited to, tungsten and titanium nitride.

[0036] The materials in the stacks may be deposited through chemical vapor deposition (CVD) techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), or plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Certain disclosed embodiments may be useful whenever wafer stress and/or bowing are induced due to material present on the frontside of the wafer.

[0037] The frontside stacks may be deposited to any number of layers and thicknesses. In an example, the stack may include about 20 or more layers, and have a total thickness of about 2 μm to about 4 μm . In some cases, multiple-layer stacks may include about one hundred or more layers. In some embodiments, multiple-layer stacks may have about five hundred or more layers. In some embodiments, the multiple-layer stacks may have about one thousand or more layers. Such stacks may have a thickness of about 4 μm to 12 μm , for example.

[0038] The stress induced in the wafer by the stack or other frontside deposition may be about -500 MPa to about +500 MPa. In some embodiments, the resulting bow is about 150 μm or greater, e.g., about 300 μm and above, about 400 μm and above, or about 200 μm to about 400 μm (for a 300 mm wafer).

[0039] Another cause of wafer bow may be frontside processing which uses thick hardmasks with limited etch selectivity. In these embodiments, at least one of the one or more frontside layers is a hardmask. The thick hardmasks may have an internal stress similar to those described above, e.g., have a magnitude of 0 MPa to about 500 MPa. The stress caused by the hardmask may be tensile stress or compressive stress. The thick hardmasks may cause wafers to have a significant wafer bow, e.g., about 150 μm or more.

[0040] Various techniques have been devised for combatting bowing. When bowing is severe, deposition processes may be tuned to reduce or counteract internal stresses in deposited layers. However, any such tuning should not interfere with process requirements for fabricating devices.

One commonly used technique to counteract bowing deposits layers on the backside of the wafer.

[0041] Backside deposition may form a high-stress film on the backside of the wafer intentionally to control overall stress and bowing of the wafer. If the backside layer has the same type of internal stress (tensile or compressive) and of comparable magnitude to the internal stress
5 created on the frontside of the wafer, the backside film effectively counteracts and reduces the bow of the wafer.

[0042] Examples of backside films used to counteract bow include the following: amorphous silicon, silicon oxide, silicon nitride, and silicon oxynitride. Variations of these films may be used, such as doped amorphous silicon, doped silicon oxide, doped silicon nitride, and doped silicon
10 oxynitride; and these films may be formed under different deposition conditions to tune and optimize their material properties. Also, other types of films that may be introduced during the semiconductor process may be used in conjunction with, and/or instead of, these exemplary films. Current backside films have high internal stress and can mitigate the stresses imparted on the wafer from the frontside layers to reduce or eliminate the wafer bow. Although not required, generally,
15 backside layers are made of films with high stress when deposited on the silicon wafer. High-stress films may be preferred because a high-stress films may compensate the wafer bow more efficiently.

[0043] In some embodiments, backside film thicknesses are relatively uniform because the bow caused by depositing material on the frontside is relatively symmetrical, forming a bowl or dome
20 shape based on an isotropic internal stress. Thus, depositing a uniform thickness profile film, either with tensile or compressive internal stress, could mitigate the stress imparted on a wafer from the frontside layers as the backside film would impart an opposite wafer bow that is similarly symmetrical. However, certain frontside deposition techniques may cause anisotropic stress, such that the internal stress on the frontside of the wafer, and hence the resultant bowing, varies in one
25 principal planar direction compared to another principal planar direction, e.g., x and y directions. In such embodiments a wafer may have x-bow and y-bow that are different in magnitude as well as direction (or sign). A uniform backside layer may insufficiently address such saddle-shaped wafer bow.

[0044] Figure 2 presents a perspective view of a bowed wafer exhibiting asymmetrical bowing.
30 Substrate 201 is shown relative to a three-dimensional coordinate system having reference plane 203 parallel to a plane defined by the x-axis direction and the y-axis direction. In this manner, an extent of deformation (e.g., warpage) of substrate 201 from reference plane 203 is indicated along the u axis-direction. Accordingly, substrate 201 is shown as being asymmetrically bowed. In other words, an extent of the bowing of substrate 201 along the x-axis direction is different than

an extent of the bowing of substrate 201 along the y-axis direction. For instance, bow in the x-axis direction has a positive value and bow in the y-axis direction has a negative value. Such deformation of substrate 201 may be referred to as “saddle-shaped” bowing of substrate 201. As used herein, warpage refers to any deviation of a median surface of substrate 201 from a reference plane 203, and, thereby, from planarity.

[0045] One technique to address saddle-shaped wafer bow is to deposit films on the backside of the wafer that cause anisotropic stress across the wafer from the backside such that the overall wafer bow may be controlled. Such films, when viewed along an x-direction, may have an internal compressive stress near the center of the wafer while having an internal tensile stress near the edge of the wafer, or vice versa. Such films, when viewed along a y-direction, may have an internal compressive stress from center-to-edge or an internal tensile stress from center-to-edge. When deposited on the backside of a wafer such films may reduce wafer bow that is unequal along x and y directions. While such techniques are obviously applicable to wafers having a positive y-bow and negative x-bow, or vice versa, techniques disclosed herein may be applied to various wafer bow shapes that have a different magnitude or sign of bowing in one principal direction than the other principal direction, or wafers having no bow. For example, the techniques disclosed herein may be applied to the wafer having a certain shape of bow caused by the frontside deposition. For another example, the backside of the bare wafer having no frontside deposited layers or the wafer having no or minimal bow may be processed with the techniques disclosed herein preemptively before bow is generated due to the frontside deposition.

[0046] Anisotropic internal stress may be accomplished by depositing curved bar profile and curved channel profile films on a wafer. A curved bar profile film and a curved channel profile film may have different internal stresses, resulting in a stacked film that has an anisotropic internal stress, i.e., the internal stress changes based upon the direction. As an example, Figures 3A-C illustrate curved bar and curved channel profile films. Figure 3A is a bottom-side view of a wafer 306 having a center zone 304 and edge zones 302. Figure 3B and 3C present a side view and exploded side view, respectively, along the x direction of the wafer 306 having a curved bar profile film 308 and a curved channel profile film 307. A frontside layer 305 may be deposited on the frontside (or top) of wafer 306, causing a wafer bow that is compensated by films 307 and 308 deposited on a backside (or bottom) of the wafer 306. A film may be deposited on the backside of the wafer such that the film is substantially deposited in either center zone 304 or edge zones 302. This may be accomplished by a showerhead that is configured to substantially deposit in center zone 304 or edge zones 302. In some embodiments, a showerhead pedestal (or shopped) may be used for such deposition. In some embodiments, a shopped may be configured to deposit in such

zones by, e.g., control of reactant gas flow in zones of the shopped that correspond to the zones of Figure 3A. Such zones are schematically illustrated in Figure 3A for illustration purposes only; a shopped or wafer may be considered having any different numbers, shapes, and configurations of zones.

5 [0047] Referring back to Figures 3B and 3C, a film deposited substantially in center zone 304 may have curved bar profile 308, while a film deposited substantially in edge zones 302 may have curved channel profile 307. That is, for example, a compressive stress film (307) may be deposited more in edge zones 302 (e.g., is thicker) compared to in center zone 304, while a tensile stress film (308) may be deposited more in the center zone 304 (e.g., is thicker) compared to in edge zones
10 302. While films may be deposited substantially in either center zone 304 or edge zones 302, it should be understood that some deposition may occur across the wafer and in the other zone. Furthermore, the shapes of the curved bar profile and curved channel profile are mere examples and variations in profile shape may occur. In some embodiments, center zone 304 may also be referred to as a curved bar profile deposition zone. In some embodiments, edge zones 302 may
15 also be referred to as a curved channel profile deposition zone. In some other embodiments, center zone 304 may be referred to as a curved bar profile deposition zone, and edge zones 302 may be referred to as a curved channel profile deposition zone.

[0048] The curved bar profile film 308 has a decreasing thickness along an x direction from center to edge of wafer 306 and a uniform, or substantially uniform, thickness along a y direction
20 of the wafer. Conversely, the curved channel profile film 307 has an increasing thickness along the x direction from center to edge of wafer 306 and a uniform, or substantially uniform, thickness along a y direction of the wafer. Together, curved bar profile film 308 and curved channel profile film 307 may form a uniform thickness profile film.

[0049] As film 307 and film 308 are deposited independently, each film may be deposited under
25 conditions to have a different internal stress. For example, curved bar profile film 308 may have a compressive internal stress, while curved channel profile film 307 may have a tensile internal stress, or vice versa. As film stresses may be superimposed, the stacked film may have a compressive internal stress in areas of the film having a small x/large y coordinate, i.e., corresponding to center zone 304, while the stacked film also has a tensile internal stress in areas
30 of the film having a large x/small y coordinate, i.e., coordinating to edge zones 302, or vice versa. As noted above, the center of the wafer may be considered the origin, e.g., $x=0$ and $y=0$.

[0050] Deposition of a curved bar profile film and a curved channel profile film may be done using a gas distributor (also called a showerhead or shopped) that allows for zonal control of deposition. According to various embodiments, a gas distributor is used to distribute one or more

gases, such as one or more process (or reactant) gases and/or one or more dilution gases, in an area adjacent to (e.g., over or under) a substrate in a process chamber. Generally, a gas distributor may have a first surface and a second surface, each of which includes ports (or holes) that are fluidically interposed between an interior and an exterior of a main body of the gas distributor. The first surface defines a portion of the main body that, during a semiconductor process, faces towards a location in the process chamber where a wafer may be positioned during processing operations. The first surface includes a plurality of gas distribution ports, which are openings or apertures that permit gas to be delivered from within the gas distributor towards the substrate. The second surface defines a portion of the main body that faces away from the location in the process chamber where a wafer may be positioned during processing operations. In a plan view, each of the first and second surfaces may have a circular (or substantially circular) shape, but embodiments are not limited thereto. At least one third surface may extend between the first and second surfaces to enclose one or more volumes within the gas distributor. These one or more volumes may define portions of one or more gas distribution flow paths interior to the gas distributor and may be defined by one or more through-holes (or passages), cavities, recessed portions, and/or elongated holes in an interior of the gas distributor. One or more gas inlets may interface with the second surface to deliver one or more gases for distribution. In some embodiments, the one or more gas inlets are provided in a stem connected to the second surface. Gas within the one or more volumes exits the gas distributor by flowing out of the plurality of gas distribution ports. As previously mentioned, a showerhead pedestal is a showerhead configured to deliver gas(es) to a backside of a substrate.

[0051] Figure 4A and 4B schematically illustrate perspective views of a gas distributor according to various embodiments. A showerhead pedestal 400 includes main body 401, outer wall 403, and stem 405. Main body 401 has first surface 401a that is perpendicular to a central axis 417 of showerhead pedestal 400 in a first direction. First surface 401a includes a plurality of gas distribution ports 407, which may be divided into a plurality of zones (or groups), such as zones 411, 413, and 415. Zones 411, 413, and 415 may be adjacent to one another along a second direction (e.g., a direction extending parallel to the x-axis direction). Further, zones 411, 413, and 415 may longitudinally extend in a third direction (e.g., a direction extending parallel to the y-axis direction). In some embodiments, the longitudinal extension of zone 413 may separate zone 411 from zone 415. In some embodiments the first, second, and third directions are substantially perpendicular to each other. Although three zones are depicted, embodiments are not limited thereto. For example, the gas distribution ports 407 may be divided into two zones or divided into four or more zones. Zones 411, 413, and 415 may correspond to center zone 304 and edge zones 302 of Figure 3.

[0052] In addition, one or more of the zones of gas distribution ports 407 may include at least one sub-zone of gas distribution ports. For instance, zones 411, 413, and 415 may include sub-zones. In some embodiments, each of the zones of gas distribution ports may have a same pattern (or spatial arrangement) of gas distribution ports, except the gas distribution ports
5 disposed in a sub-zone may have a different pattern, e.g., denser or less dense pattern. Embodiments, however, are not limited thereto.

[0053] According to one embodiment, central axis 417 of showerhead pedestal 400 extends through a center of zone 413 along with transverse axes 419 and 421 of first surface 401a. Transverse axis 419 may extend through the respective centers of zones 411 and 415. In various
10 implementations, the shape of zone 413 may exhibit symmetry about each of transverse axes 419 and 421. The shapes of zones 411 and 415 may exhibit symmetry about transverse axis 419. The shape of zone 411 may have mirror symmetry with the shape of zone 415 about transverse axis 421. Similarly, a pattern of gas distribution ports in zone 413 may have symmetry about each of
15 transverse axes 419 and 421. In one or more embodiments, at least some of the gas distribution ports in zones 411, 413, and 415 may be distributed (or arranged) across a circular area. It is also noted that the combined patterns of gas distribution ports in zone 411 and the combined patterns of gas distribution ports in zone 415 may exhibit mirror symmetry about a transverse axis (e.g., transverse axis 421), but not exhibit 3-fold or higher radial symmetry.

[0054] Although certain shapes, relative dimensions, and symmetries for the zones, sub-zones,
20 and sub-portions of sub-zones have been described, embodiments are not limited thereto. For instance, the zones, sub-zones, and sub-portions of gas distribution ports 407 may have any suitable shape, relative dimensions, symmetries, and/or asymmetries that may enable a uniform (or substantially uniform) amount of gas flow within zone 413 and a changing amount of gas flow in zones 411 and 415 as a distance from central axis 417 increases. Further, although
25 certain patterns, pitches, diameters, offsets, symmetries, and/or asymmetries for the gas distribution ports in the zones, sub-zones, and sub-portions have been described, embodiments are not limited thereto. For example, the gas distribution ports in the zones, sub-zones, and sub-portions may have any suitable pattern, pitch, diameter, offset, symmetry, and/or asymmetry that may enable a uniform (or substantially uniform) amount of gas flow within (or across) zone 413
30 and an increasing amount of gas flow within (or across) zones 411 and 415 as a distance from central axis 417 increases. To this end, the gas distribution ports in a sub-zone or sub-portion of a sub-zone may have any suitable pattern, pitch, diameter, symmetry, and/or asymmetry that may enable a changing amount of gas flow in (or across) zones 411 and 415 as a distance from central axis 417 increases. Further, the gas distribution ports in a sub-portion may have any

suitable offset from an outermost gas distribution port of a corresponding zone including the sub-portion to enable gas flow at (or near) an edge portion of zones 411 and 415 to match (or substantially match) an intended gas flow profile across zones 411 and 415. Thus, the various gas flow profiles serve as a stand-in for all of the various structural ways the gas distribution ports 407 may be configured to arrive at an intended result.

[0055] According to various embodiments, gas distribution ports 407 may distribute one or more gases, such as one or more process (or reactant) gases and/or one or more dilution gases, in an area adjacent to a backside of a substrate in a process chamber. For instance, one or more first gases may be flowed from the gas distribution ports of zone 413 and one or more second gases may not only be flowed from the gas distribution ports of zones 411 and 415. As such, showerhead pedestal 400 may modulate a concentration of precursor gas delivered across a backside of a substrate by flowing one or more dilution gases in one of zone 413 or zones 411 and 415 and flowing one or more precursor gases in the other of zone 413 or zones 411 and 415. In this manner, a flow of inert gas in certain zones or regions adjacent to the substrate will dilute or otherwise limit a concentration of precursor gas in the regions adjacent to the substrate that is flowed from certain other zones or regions adjacent to the substrate. Example inert gases include, but are not limited to nitrogen (N₂), helium (He), argon (Ar), neon (Ne), or xenon (Xe). Example process (or precursor) gases include, but are not limited to, silicon-containing gases, oxygen-containing gases, and nitrogen-containing gases (although generally not pure N₂).

[0056] In some implementations, during operation an inert gas is flowed through main body 401 to mix with precursor gas in an environment adjacent to the substrate. According to some embodiments, the inert gas is flowed through main body 401 to mix with precursor gas in an environment adjacent to the substrate, but without mixing within main body 401 of showerhead pedestal 400. As such, main body 401 may include one or more first gas distribution flow paths to distribute one or more first gases to the gas distribution ports of zone 413 and may include one or more second gas distribution flow paths to distribute one or more second gases to gas distribution ports of zones 411 and 415.

[0057] A non-uniform profile film may be defined by a deposition profile. In some embodiments, a deposition profile may be a thickness profile measured in an x-direction at y=0. In some embodiments, a deposition profile may represent a surface reaction flux, which indicates a reaction rate along an x-direction. In some embodiments, a surface reaction flux may directly correlate with a growth rate of a layer, and thus may also directly correlate with a thickness profile. The deposition profile of a non-uniform profile film may depend on various process conditions, including gas flow, RF power, pressure, temperature, etc., as well as the shaped

design. For example, increasing or decreasing RF power may change the profile of a curved bar profile film to have a steeper or less steep profile. Figure 9 presents a chart indicating film thickness as a function of radial distance along an x-axis for different amounts of high-frequency (HF) power. Increasing the HF power changes the deposition profile to have a greater proportion of deposition near the center of the wafer than the edge of the wafer.

[0058] In some embodiments, it is desirable to simulate the deposition profile as a function of various inputs, including various parameters that may be set in a recipe and the shaped design, to better understand the resulting profile of a non-uniform profile film. This may improve recipe development by understanding the deposition profile of a non-uniform profile film based on various process conditions. For example, a model may be used to predict the deposition profile based in part on HF power, similar to the empirical data shown in Figure 9.

[0059] A model may also be useful in the design of shapeds. As noted above in reference to Figures 4A–B, process gases may be flowed from gas distribution ports 407, which may be divided into various zones. When depositing a uniform profile film, a uniform distribution of gas distribution ports may be desirable to deposit a film having a uniform thickness. However, when depositing non-uniform profile films, it may be desirable for the shaped to have a different configuration of gas distribution ports. Simulating a non-uniform film profile based in part on a shaped design may improve the design process as different hardware configurations may be simulated without needing to construct and test each shaped design. For example, different shaped designs may be simulated to determine a shaped design that permits a process window having desired deposition profiles for non-uniform profile films. In some embodiments, desirable deposition profiles for non-uniform profile films may include deposition profiles that are substantially complementary, i.e., a curved bar profile film and a curved channel profile film that together form a substantially flat stacked film. It may also be desirable to control the relative proportions of a curved bar profile film and a curved channel profile film so that the resulting stacked film has a greater compensation of y-bow or x-bow. For example, a relatively larger curved bar profile film may compensate additional y-bow compared to a smaller curved bar profile film. Manufacturing various shaped designs is extremely costly and time-consuming. Thus, simulating the deposition profiles based on shaped designs may reduce costs and improve iteration speed.

[0060] Described herein is a transport-reaction model to predict deposition profiles for non-uniform profile films. Models disclosed herein may include an advection-diffusion transport scheme that may consider multiple species as well as bulk electron generation and consumption resulting from a plasma ignited during deposition.

[0061] In some embodiments, different models may be trained for different non-uniform profile films, e.g., a first model may be trained for simulating the deposition profile of a curved bar profile film, and a second model may be trained for simulating the deposition profile of a curved channel profile film. In some embodiments, different models may be trained depending on the material to be deposited. For example, a SiN film may be deposited using silicon-containing reactants and nitrogen-containing reactants, while a SiO₂ film may be deposited using silicon-containing reactants and oxygen-containing reactants. In some embodiments, a SiN film deposition process may have a lower surface reaction rate than a SiO₂ film deposition process. Thus, a SiN film deposition process may be more surface reaction limited than a SiO₂ deposition process, while a SiO₂ deposition process may be more mass transport limited. Developing a different model for each non-uniform profile film and each film material may more accurately model the respective deposition profiles.

[0062] The diffusion-advection equation with reacting species for a backside film deposition may be defined as:

$$-R + \nabla \cdot (-D_i \nabla c_i) + \nabla \cdot (\mathbf{u} c_i) = 0 \quad \text{EQ. 1}$$

[0063] Where R is the reaction rate for a particular species i, $\nabla \cdot (-D_i \nabla c_i)$ represents diffusion, and $\nabla \cdot (\mathbf{u} c_i)$ represents convection, with D_i being the diffusion coefficient for a species and c_i being the concentration of the species. $\mathbf{u}$ represents the velocity field. Species i may include precursor species, such as SiH₄ and NH₃ (which may be used to deposit SiN films), as well as radical species, such as SiH₄ and NH₃ that have been radicalized in a plasma. In some embodiments, multiple species may be treated as a single species for purposes of modeling mass transport and reactions. In some embodiments, precursor species of SiH₄ and NH₃ may be modeled as a single species. In some embodiments, radicalized SiH₄ and NH₃ species may be modeled as a single species. In some embodiments, three different species may be modeled: precursors species that have not been radicalized, radical precursor species, and electron species. In some embodiments, electron species may be modeled as high energy and low energy species, as discussed further below.

[0064] The velocity field $\mathbf{u}$ may be determined using a computational fluid dynamics (CFD) model. CFD models may simulate fluid flow given various boundary conditions, including temperature, pressure, and gas flow. A CFD model may also simulate fluid flow based on particular shaped designs, considering how fluid will flow through flow paths of the shaped and from gas distribution ports such as those shown in Figures 4A-B. For example, the design of a shaped and various process conditions such as temperature, pressure, and gas flow may be

provided to a CFD model, which may then simulate the fluid flow to determine a velocity field. In some embodiments, the velocity field may model the effect of inert gas flow from gas distribution ports in zones of the showerhead from which precursors are not flowed. As noted above, during deposition of a non-uniform profile film precursors may only flow from a subset of all gas distribution ports in a showerhead based on zones of the showerhead.

[0065] The diffusion-advection equation may be used to derive several equations that model the deposition of backside films as described herein:

$$J_i = \mathbf{u}c_{i0}, \text{ where } c_{i0} = 0, 1, i = 1, 2 \quad \text{EQ. 2}$$

$$J_{c_1} = (-D_i \nabla c_i) + \mathbf{u}c_i, i = 1, 2 \quad \text{EQ. 3}$$

Equation 2 defines the initial flux for species i flowing from the showerhead, where c_{i0} defines the initial concentration of species i . As noted above, two species that may be modelled include radicalized and precursor species, where $i = 1$ refers to radicals and $i = 2$ refers to precursor or non-radical species. In some embodiments, c_{i0} may have a value of 0 or 1 for each gas distribution port. As noted above, a showerhead may group gas distribution ports into one of a plurality of zones, e.g., a center zone and edge zones. When depositing a curved bar profile film, the concentration of precursors at gas distribution ports in edge zones is 0, as precursor gas is not flowed from such ports. Conversely, when depositing a curved channel profile film, the concentration of precursors at gas distribution ports in a center zone is 0, as precursor gas is not flowed from such ports. The concentration may otherwise be 1 to indicate that the velocity field comprises precursor species. Equation 3 defines the diffusion and convection of species. In some embodiments, equations 2 and 3 are used to model mass transport for precursor species, where $i = 1, 2$ corresponds to non-radical and radical species.

[0066] In some embodiments, precursor and radical species may be modelled as a concentration of solutes in an inert gas flow that is treated as a solvent. For example, inert gas may be flowed from all ports as defined by the velocity field $\mathbf{u}$, with an initial concentration of precursor species depending that depends on the intended deposition area. Inert gas may be flowed independently of precursor species, and the precursor species may be modelled as a concentration within the inert gas flow. For example, when modelling film growth in a center zone, the concentration of precursors in the center zone may be defined by a boundary condition and the concentration of precursors in the edge zones may be zero.

[0067] In some embodiments, the model may also account for the generation of hot electrons

that can interact with the precursors to generate radicals as well as interact with the film to be grounded. Hot electrons are electrons that have a large amount of kinetic energy, typically measured in eV. In some embodiments, a hot electron may have an energy greater than about 2 eV. The generation of hot electrons depends upon the RF power and may be modeled as a
 5 function of RF power:

$$R_{e_{generation}} = k \times RF \text{ power} \quad \text{EQ. 4}$$

A higher RF power will increase the density of hot electrons. K is a constant that relates the RF power to hot electron generation. Hot electrons may then be consumed in 3 ways:

$$10 \quad R_{c_{1,bulk}} = -r_1 e c_1 \quad \text{EQ. 5}$$

$$R_{e_{bulk}} = -r_2 e c_2 \quad \text{EQ. 6}$$

$$R_{e_{surface}} = -r_3 e \quad \text{EQ. 7}$$

Equation 5 defines the consumption of radical species c_1 and hot electrons e to deposit the film, with rate constant r_1 . As the concentration of species c_1 and hot electrons e increases, the flux J_{c1}
 15 increases. R_{c1} is directly correlated to the reaction rate at the surface of the wafer, and thus the growth rate of the film. Equation 6 defines the consumption of precursor species c_2 and hot electrons e to generate excited species and low energy or “cold” electrons with a rate constant r_2 . Equation 7 defines the consumption of hot electrons e as grounded through the wafer without facilitating a reaction (such as shown in equation 4), with rate constant r_3 . Equations 4–7 may be
 20 used to model the generation and depletion of hot electrons during deposition processes.

[0068] Furthermore, hot electrons may diffuse towards the wafer surface by diffusion but not advection due to their fast velocity, as follows:

$$J_e = (-D_e \nabla e) \quad \text{EQ. 8}$$

Where D_e is a diffusion coefficient and ∇e is the electron gradient.

25 [0069] During simulation and modelling, the concentrations c_1 , c_2 , and e may be unknown, with other values known such as rate constants and diffusion coefficients. In some embodiments, rate constants and diffusion coefficients may be determined from empirical data and are assumed to not change based on other process conditions. In some embodiments, rate constants and diffusion coefficients may be a function of, e.g., temperature or pressure, which may be defined
 30 as inputs to the model. A CFD model may determine the velocity field $\mathbf{u}$, and then the system of equations may be solved to determine c_1 , c_2 , and e . As noted above, equation 5 describes the reaction rate on the wafer surface, from which the film growth rate and thickness may be

determined. For example, as shown in Figure 9, a thickness profile of a non-uniform profile film may be determined from J_{e1} in equation 5, above.

[0070] Figure 5 presents a flowchart for a process of simulating deposition profiles according to various embodiments herein. Parameter values may be received for a semiconductor device fabrication process (502). In some embodiments, the semiconductor device fabrication process is to deposit a non-uniform profile film as disclosed herein. The parameter values may include RF power, including LF and HF power, pressure, precursor concentration, gas flow (which may include precursor gas flow and inert gas flow), temperature, or any combinations thereof. In some embodiments, the parameter values may include a showerhead design. A showerhead design may be a design similar to that shown in Figures 4A-B, having a plurality of gas distribution ports. In some embodiments the showerhead design may define flow paths from a reactant source to each gas distribution port.

[0071] Based on the parameter values, a simulation is performed (504). As noted above, the simulation may determine a concentration of precursor radicals and density of hot electrons near a surface of a substrate. The concentration of precursor radicals and electron density, along with a rate constant, may be used to determine a surface reaction flux (506). In some embodiments, a surface reaction flux may directly correspond with a deposition rate or a deposition profile (508). In some embodiments, the concentration of precursor radicals is a concentration field that is defined over the surface of the substrate. In some embodiments, the electron density is an electron density field that is defined over the surface of the substrate.

[0072] In some embodiments, operations 502-508 may be repeated one or more times with different parameter values as a simulated depth of experiment (DOE). Simulating the deposition profile for a range of various parameter values may allow for determining a range of deposition profiles that may be achieved. In some embodiments, the parameter values that are changed do not include the showerhead design. The showerhead design cannot be easily changed compared to, e.g., power or pressure, and thus the showerhead design may be held constant to determine the range of deposition profiles achievable with recipe variations.

[0073] In some embodiments, the simulation model may be calibrated against empirical data (511). A DOE may be performed on coupon wafers to determine the deposition profiles of non-uniform profile films. The deposition profile of the experimental film and the deposition profile of the simulated film may be compared and the model calibrated to minimize differences between the simulated deposition profile and the experimental deposition profile. In some embodiments, the model may be refined to minimize a cost function between the simulated deposition profile and the experimental deposition profile. In some embodiments, the DOE for

experimental films and the DOE for the simulated films may use the same showerhead design (albeit the experimental film using an actual showerhead rather than a simulated one).

5 [0074] In some embodiments, operations 502-511 may be optionally repeated one or more times to further train and refine the simulation model. In some embodiments, the showerhead design used to obtain the experimental and simulated deposition profiles may change or not change. Changing the showerhead design may improve the model by reducing overfitting to a particular showerhead design.

[0075] In some embodiments, the model may then be used to modify the showerhead design (512). As noted above, the deposition profile is strongly influenced by the showerhead design.
10 When depositing non-uniform profile films, it may be advantageous to have different gas distribution ports and flow paths for a center zone compared to an edge zone to achieve different deposition profiles. This may be particularly important for depositing complementary profile films that are substantially flat after deposition of both films. As shown in Figure 3C, it is desirable to have non-uniform profile films that have complementary deposition profiles, such
15 that the combination of films has a uniform thickness. Simulating the deposition profile based on the showerhead design may allow for faster iteration towards a showerhead design that can deposit complementary profile films having a combined uniform thickness.

[0076] In some embodiments, the simulation model may be used along with a targeted deposition profile to determine a showerhead design that would cause the targeted deposition
20 profile. A targeted deposition profile may be a desired deposition profile for a non-uniform profile film, e.g., complementary deposition profiles that form a stacked film that is substantially flat and/or uniform thickness. The targeted deposition profile may be considered a boundary condition, and a velocity field may be determined based on the targeted deposition profile and other parameters, e.g., temperature, pressure, RF power, etc. A showerhead design or portions
25 thereof may then be determined that would result in the velocity field and/or targeted deposition profile.

[0077] In some embodiments, a showerhead design may be based on multiple simulation models. As noted above, a simulation model may be trained for each non-uniform profile and/or material. For example, a model may be trained for depositing a curved-bar profile film and a
30 separate model may be trained for depositing a curved-channel profile film. Additional models may be trained based on the composition of the film, e.g., silicon nitride for a tensile film and silicon oxide for a compressive film. Thus, 4 different models may be trained based on each combination of non-uniform profile and film composition. In some embodiments, additional models may be trained for other materials. In some embodiments, each model may have a

similar velocity field $\mathbf{u}$ but use different rate constants and diffusion coefficients. This may result from the velocity field being defined in large part by the showerhead and thus any model based on the showerhead may use the same or similar velocity field, while various rate constants and diffusion coefficients may change based on the particular species and deposition zones being
5 modelled.

[0078] In some embodiments, it is desirable to have a single showerhead design that may achieve the targeted deposition profile for a curved bar profile film and a curved channel profile film. In such embodiments, the targeted deposition profile for both non-uniform profile films may be used as boundary conditions to determine a showerhead design. In some embodiments, a
10 portion of a showerhead design may be determined, e.g., an arrangement of gas distribution ports that achieve one or more targeted deposition profiles. An engineer may then design the remainder of the showerhead to achieve the one or more targeted deposition profiles.

[0079] Example materials used to make backside layers having tensile internal stress include silicon nitrides (SiN), silicon oxynitrides, and polymer layers. As examples, tensile films can be
15 deposited using CVD or PECVD techniques. To combat wafer bow caused by a frontside layer with a compressive internal force, a compressive film may be used for the bulk backside layers. Compressive films may be formed using specific materials and/or processing conditions. Example materials used to make compressive films include silicon oxides (SiO_x), silicon nitrides, aluminum oxides, aluminum nitrides, and polysilicon. Compressive films can be deposited using CVD or
20 PECVD techniques. The above-recited materials and deposition techniques may apply to any one or more backside layers in a multilayer backside stack. Any two backside layers may be formed by the same or different techniques.

[0080] Deposition by PECVD may proceed by flowing a reactant into a process chamber, and optionally with a co-reactant, while exposing the bowed semiconductor substrate to plasma. The
25 plasma may drive a gas phase reaction that results in deposition of film. The PECVD reactions may generally involve delivering reactant(s) to the semiconductor substrate continuously while the semiconductor substrate is exposed to plasma. In some embodiments, depositing a nitride film on the backside of the substrate includes exposing the backside of the flat and/or bowed semiconductor substrate to a silicon-containing precursor and a nitrogen-containing reactant, and
30 exposing the backside of the semiconductor substrate to plasma to drive a reaction between the silicon-containing precursor and the nitrogen-containing reactant to deposit the nitride film. To protect the frontside of the semiconductor substrate on which circuits, transistors, and other device components are patterned during the backside processes, the frontside is protected from being exposed to plasma and/or reactant or process gases, for example, by keeping the gap between the

frontside of the semiconductor substrate and the showerhead to less than plasma sheath and/or by flowing inert gas(es) onto the frontside of the semiconductor substrate. By depositing on the backside of the semiconductor substrate, the nitride film avoids being deposited on circuits, transistors, and other device components on the frontside of the bowed semiconductor substrate.

- 5 [0081] In some embodiments, the curved bar profile and curved channel profiles described herein may be achieved by controlling precursor concentration adjacent to the bowed semiconductor substrate during deposition. In the present disclosure, precursor concentration adjacent to the bowed semiconductor substrate may be controlled by design features in a showerhead pedestal. Such design features may influence flow dynamics of the precursor from the showerhead pedestal. In some implementations, the showerhead pedestal may be divided into multiple zones as shown in Figure 3A. For example, precursor gas may be delivered in a first zone and not a second zone and inert gas may be delivered in the first and second zones, and/or different flow rates or concentrations of precursor and inert gas may be delivered to different zones to control the thickness and/or properties of the films deposited in different zones. This may modulate the concentration of precursor gas adjacent to the bowed semiconductor substrate. In some implementations, the precursor gas may be delivered via a first supply tube and the inert gas may be delivered via a second supply tube.
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- 15

Apparatus

- [0082] In some embodiments, FIG. 6A is a block diagram that illustrates a substrate processing system 632 used to perform processing on a wafer 602, according to some embodiments. As shown, the substrate processing system may include a processing chamber (or a chamber) 634. A center column may be configured to support a pedestal for when a top surface (or a frontside) of the wafer 602 is being processed, e.g., a film is being formed on the top surface of the wafer 602, or on the backside of the wafer 602. The pedestal, in accordance with some embodiments disclosed herein, may be referred to as a showerhead pedestal ("ShoPed") 606. A showerhead 636 may be disposed over the ShoPed 606.
- 20
- 25

- [0083] In some embodiments, the showerhead 636 may be electrically coupled to power supply 638 via a match network 640. The power supply 638 may be controlled by a control module 642, e.g., a controller. In some embodiments, power may be provided to the ShoPed 606 instead of the showerhead 636, or power may be provided to both the ShoPed 606 and the showerhead 636. The control module 642 may be configured to operate the substrate processing system 632 by executing process input and control for specific process recipes. Depending on whether the top surface of the wafer 602 is receiving a deposited layer or layer stack or the bottom surface of the wafer 602 is receiving a deposited layer or layer stack, the controller module 642 may set various operational
- 30

inputs for a process recipe, such as power levels, timing parameters, process gasses, mechanical movement of a wafer 602, and/or the height of the wafer 602 relative to the ShoPed 606 (and the distance between the wafer 602 and the showerhead 636).

[0084] In some embodiments, the center column may also include lift pins, which are controlled by a lift pin control. Such lift pins may be used to raise the wafer 602 from the ShoPed 606 to allow an end effector (not shown) to pick the wafer and to lower the wafer 602 after being placed by the end effector. The end effector may also place the wafer 602 over spacers 644. As will be described below, the spacers 644 may be sized to provide a controlled separation of the wafer 602 between a bottom surface of the showerhead 636 (facing the wafer) and a top surface of the ShoPed 606 (facing the wafer).

[0085] In some embodiments, the substrate processing system 632 may further include a first gas manifold 646 that is connected to first gas sources 648, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the purposes and processing being performed over a top surface of the wafer 602, the control module 642 may controls the delivery of first gas sources 648 via the first gas manifold 646. The chosen gases may then be flown into the showerhead 636 and distributed in a space volume defined between a face of the showerhead 636 that faces that wafer 602 when the wafer is resting over the pedestal or ShoPed.

[0086] In some embodiments, the substrate processing system 632 may further include a second gas manifold 650 that is connected to second gas sources 652, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a bottom surface of the wafer 602, the control module 642 may control the delivery of second gas sources 652 via the second gas manifold 650. The chosen gases may then be flown into the showerhead 636 and distributed in a space volume defined between a face of the ShoPed 606 that faces an under surface or under side (e.g., backside) of the wafer 602 when the wafer is resting over the ShoPed 606 and/or spacers 644. The spacers 644 may provide for a separation that optimizes deposition to the under surface of the wafer 602, while reducing deposition over the top surface of the wafer 602. In some embodiments, while deposition is targeted for the under surface of the wafer 602, an inert gas may be flown over the top surface of the wafer 602 via the showerhead 636, which may push reactant gases away from the top surface and enable reactant gases provided from the ShoPed 606 to be directed to the under surface of the wafer 602. Spacers 644 and/or other similar substrate support features may be used to provide controlled separation between the wafer and the ShoPed and the showerhead. Spacers 644 and/or other similar substrate support features may be connected or supported by the ShoPed such that the wafer (or its reference plane, when the wafer is bowed)

may maintain an even and/or parallel distance from the top surface of the ShoPed, even when there is an unwanted movement or oscillation at the system or chamber level.

[0087] In some embodiments, either showerhead 636 or ShoPed 606, or both, may have a zonal deposition design similar to that shown in Figure 3A. For example, gas manifold 650 may be fluidically linked to control the delivery of gases to either zones 302 or zone 304. By controlling the flow of gases to either zones 302 or zone 304 films may be deposited as shown in Figures 3B and 3C. In some embodiments, either showerhead 636 or ShoPed, or both, may have a zonal deposition design different from that shown in Figure 3A. For example, with reference to Figure 5, when the bowing of wafer is measured or identified (502), a showerhead and/or ShoPed that has corresponding zonal deposition design to that specific wafer may be used to deposit films to the backside of the wafer, or gas flows through a showerhead and/or ShoPed may be tuned to correspond to the profile of the wafer bow.

[0088] Further, the gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct gases are delivered during the deposition and plasma treatment phases of the process. Process gases may exit the chamber 634 via one or more exhausts or outlets. A vacuum pump (e.g., a one or two stage mechanical dry pump and/or a turbomolecular pump) may draw process gases out and maintains a suitably low pressure within the reactor by a close loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0089] In some embodiments, a carrier ring 654 may encircle an outer region of the ShoPed 606. When the top surface of the wafer 602 is being processed, e.g., a material is being deposited thereon, the carrier ring 654 may be configured to sit over a carrier ring support region that is a step down from a wafer support region in the center of the ShoPed 606. The top surface of the carrier ring 654 is generally coplanar with the top surface of the wafer 602. The carrier ring 654 may include an outer edge side of its disk structure, e.g., outer radius, and a wafer edge side of its disk structure, e.g., inner radius, that is closest to where the wafer 602 sits. The carrier ring 654 may be associated with an inner diameter (ID). The inner diameter may extend to an inner perimeter of the carrier ring and generally surround a substrate (e.g., wafer 602) in a processing chamber. The wafer edge side of the carrier ring 654 may also include a plurality of contact support structures or “tabs” which may be configured to lift the wafer 602 when the carrier ring 654 is held by the spacers 644. The carrier ring 654 may include a plurality of tabs with a quantity selected from a range to support the wafer 602 during processing. Additional details regarding embodiments of the tabs will follow. In some embodiments, a wafer may be placed directly upon, or supported directly by, spacers or other similar substrate support features without a carrier ring.

[0090] FIG. 6B is a block diagram that illustrates another version of substrate processing system 632 used to perform processing on the wafer 602, according to some embodiments. In some embodiments, spider forks 656 may be used to lift and maintain the carrier ring 654 in its process height, e.g., to allow depositing in the under surface (backside) of the wafer 602. The carrier ring
5 654 may therefore be lifted along with the wafer 602. In some implementations, the carrier ring 654 may be rotated to another station, e.g., in a multi-station system. In some embodiments, a spider forks or any other transfer mechanism may be used to lift or move the wafer directly without a carrier ring.

[0091] Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD
10 films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead 636) and a ShoPed 606. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination of showerhead and pedestal, which enables deposition on a backside of the wafer. The electrode
15 geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal or ShoPed may include an embedded controlled heater (or distributed heater or heater elements), wafer lift mechanisms, ability to hold plasma suppression rings, and movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

20 [0092] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the ShoPed, showerhead, and/or electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side
25 that gets deposited.

[0093] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow
30 the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0094] In some embodiments, the gap between the side of the wafer that does not need plasma/deposition may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment

from about 1 mm to about .05 mm (limited by the wafer bow), and such gap can be controlled. The gap maybe controlled depending on process conditions.

[0095] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposition film in different areas of the backside of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0096] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 654 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0097] Figure 7A shows a cross-sectional view of an edge region of the ShoPed 606. This view provides a cross-sectional representation of the carrier ring 654, which has a carrier ring inner radius 654a and a carrier ring outer radius 654b. In some embodiments, the carrier ring 654 includes support extensions 654c, which extend below the substantial flat surface of the carrier ring 654.

[0098] The support extensions 654c are configured to mate and sit within support surfaces defined into a top surface of the spacers 644. The support surfaces provide a complementary mating surface for the support extensions 654c, such that the carrier ring 654 is prevented from sliding or moving when supported by the spacers 644. Although three spacers are shown as spacers 644 are shown in Figure 7B, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 606, and spacing is defined for supporting wafer 602 at a spaced apart relationship from a top surface of the ShoPed 606.

[0099] Further shown is that a top surface of the ShoPed 606 will include a hole pattern 606a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 606a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 606 and extend to an outer periphery of the ShoPed 606. At least one hole pattern 606a is provided at an edge hole region 607 of the hole pattern, and orifices defined in the edge hole region 607 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 606.

[0100] In one example, the angle or tilt at which the orifices in the edge hole region 607 is defined to tilt or angle away from the center of the ShoPed 106. In one embodiment, the angle is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 607, additional distribution of process gases can be provided during backside deposition of the wafer 602. In one embodiment, the remainder orifices 606d of the hole pattern 606a are oriented substantially perpendicular to the surface of the ShoPed 106 and directed toward the underside of the wafer 602.

[0101] Figure 7B illustrates that when the wafer 602 is held by the carrier ring 654, the wafer 602 edge will sit on an edge region closer to the carrier ring inner radius 654a of the carrier ring 654. The surface of the showerhead 636 facing the top surface of the wafer 602, when positioned using spacers 644, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the wafer 602.

[0102] By way of example, the distance between the top of the wafer 602 and the surface of the showerhead 636 is preferably between about 2 mm to about .5 mm, and in some embodiments about 1 mm to about .5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about .5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about .5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 636 is configured to supply an inert gas flow over the top side of the wafer 602 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 606.

[0103] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0104] Figure 8 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 800 includes a transfer module 803. The transfer module 803 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 803 is a multi-station reactor 809 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 809 may include multiple stations 811, 813, 815, and 817 that may sequentially perform operations in accordance with disclosed embodiments. Stations may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0105] Mounted on the transfer module 803 may be one or more single or multi-station modules 807 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 800 also includes one or more wafer source modules 801, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 819 may first remove wafers from the wafer source modules 801 to loadlocks 821. A wafer transfer device (generally a robot arm unit) in the transfer module 803 moves the wafers from loadlocks 821 to and among the modules mounted on the transfer module 803.

[0106] In various embodiments, a system controller 842 is employed to control process conditions during deposition. The system controller 842 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0107] The system controller 842 may control all the activities of the deposition apparatus. The system controller 842 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 842 may be employed in some embodiments.

[0108] The depicted embodiment includes a user interface associated with the system controller 842. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0109] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by

“programming.” Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor.

5 System control software may be coded in any suitable computer readable programming language.

[0110] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may
10 be hard coded.

[0111] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

15 [0112] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 842. The signals for controlling the process are output on the analog and digital output connections of the system 800.

[0113] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of
20 the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0114] In some implementations, a system controller 842 is part of a system, which may be part
25 of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the
30 “controller,” which may control various components or subparts of the system or systems. The system controller 842, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching
35 circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and

operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

System Controllers

[0115] Broadly speaking, a controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. Such controller may be used in or with any of the apparatus described herein. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0116] A system controller may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, a system controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located

remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0117] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0118] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0119] A system controller may include various programs. A substrate positioning program may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control program may include code for controlling gas composition, flow rates, pulse times, and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck.

[0120] Examples of chamber sensors that may be monitored during deposition include mass flow controllers, pressure sensors such as manometers, and thermocouples located in the pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0121] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of

the following steps, each step provided with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively
5 remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

Conclusion

[0122] Although the foregoing embodiments have been described in some detail for purposes of
10 clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Embodiments disclosed herein may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. Further, while the disclosed embodiments will be described in conjunction with
15 specific embodiments, it will be understood that the specific embodiments are not intended to limit the disclosed embodiments. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

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CLAIMS

What is claimed is:

1. A computer program product, comprising a non-transitory computer readable medium
5 having computer-executable instructions for:
 - (a) receiving parameter values for a plurality of parameters of a semiconductor device fabrication process to deposit a non-uniform profile film on a substrate, wherein the semiconductor device fabrication process is performed by a process chamber having a showerhead with a plurality of zones;
 - 10 (b) performing a simulation of the semiconductor device fabrication process based on the parameter values; and
 - (c) determining a deposition profile of the non-uniform profile film based on the simulation.
- 15 2. The computer program product of claim 1, wherein the plurality of parameters comprises a showerhead design.
3. The computer program product of claim 1, wherein the simulation is performed using a model for curved-bar profile films.
- 20 4. The computer program product of claim 1, wherein the simulation is performed using a model for curved-channel profile films.
5. The computer program product of claim 1, wherein the simulation is performed using a
25 model for silicon nitride films.
6. The computer program product of claim 1, wherein the simulation is performed using a model for silicon oxide films.
- 30 7. The computer program product of claim 1, comprising additional computer-executable instructions for determining a concentration field of precursor radicals and an electron density field at the substrate surface during the semiconductor device fabrication process, wherein the deposition profile is based on the concentration field of precursor radicals and the electron density field at the substrate surface.

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8. The computer program product of claim 7, wherein the electron density field represents hot electrons.
9. The computer program product of claim 1, wherein the plurality of parameters comprises RF power.
10. The computer program product of claim 1, wherein the plurality of parameters comprises RF power.
11. The computer program product of claim 1, wherein the plurality of parameters comprises pressure.
12. The computer program product of claim 1, wherein a first parameter value for a first parameter for a first zone of the plurality of zones is different from a second parameter value for the first parameter for a second zone of the plurality of zones.
13. The computer program product of claim 12, wherein the first parameter is a flow rate.
14. The computer program product of claim 12, wherein the first parameter is a concentration of precursor species.
15. The computer program product of claim 1, wherein the non-uniform profile film comprises silicon oxide or silicon nitride.
16. A method, comprising:
- (a) receiving parameter values for a plurality of parameters of a semiconductor device fabrication process to deposit a non-uniform profile film on a substrate, wherein the semiconductor device fabrication process is performed by a process chamber having a showerhead with a plurality of zones;
 - (b) performing a simulation of the semiconductor device fabrication process based on the parameter values; and
 - (c) determining a deposition profile of the non-uniform profile film based on the simulation.