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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 21 /768, 23 /532 — A1

(11) International Publication Number: WO 00/05773

(43) International Publication Date: 3 February 2000 (03.02.00)

(21) International Application Number: PCT/US99/16558

(22) International Filing Date: 21 July 1999 (21.07.99)

(30) Priority Data:
09/121,236 23 July 1998 (23.07.98) US

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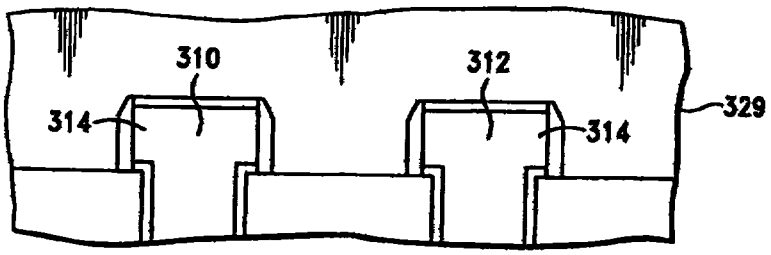
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(81) Designated States: JP, KR, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: INTEGRATED CIRCUIT INTERCONNECT LINES HAVING SIDEWALL LAYERS

(57) Abstract



The present invention provides Cu lines which are enclosed within Cu diffusion barrier layers, for IC structures such as semiconductor devices. The Cu lines (310) have conventional top (316) and bottom (318) Cu diffusion barrier layers and novel sidewall layers (324 and 326) comprising Cu diffusion barrier materials. The present invention also provides for conductive interconnect lines for semiconductor devices which compensate partly or completely for a misalignment between the line etch pattern and the underlying contact element, such as a via plug. The misalignment tolerant line (430) is formed by fabricating novel sidewalls (438 and 440) on the line wherein the sidewalls have a thickness which equals or exceeds the width of the gap (431) which is caused by the misalignment. The misalignment tolerant line compensates for the misalignment gap and thereby prevents etching a trench in the contact element. Trench formation is reduced rather than prevented when the sidewall is thinner than the width of the misalignment gap. In additional embodiments, manufacturing systems (510) are provided for fabricating the structures of the present invention. These systems include a controller (500) which is adapted for interacting with a plurality of fabrication stations (520, 522, 524, 526 and 528).