SEMICONDUCTOR DIE PACKAGES WITH RECESSED INTERCONNECTING STRUCTURES AND METHODS FOR ASSEMBLING THE SAME

TECHNICAL FIELD

The present invention relates to ball grid array semiconductor packages and methods of attaching, and interconnecting the same. In particular, the present invention relates to interposers for mounting a semiconductor die to a substrate with which the semiconductor die is in electrical communication The semiconductor die may be encapsulated upon the interposer to form a complete semiconductor die package. The interposer may be constructed in order to allow a number of similar semiconductor die packages to be electrically connected to a single substrate in a stack.

BACKGROUND ART

Ball grid array ("BGA") packages are well known in the art. BGA packages typically comprise a substrate, such as a printed circuit board, with a semiconductor die mounted on top of the substrate. The semiconductor die has a multitude of bond pads electrically connected to a series of metal traces on the top side of the printed circuit board. This series of metal traces is connected to a second series of metal traces located on the underside of the printed circuit board by a series of vias. The second series of metal traces each terminate with a contact pad where a conductive element is attached. The conductive elements are typically solder balls or conductive filled epoxy. The conductive elements are arranged in an array pattern and the semiconductor die along with its electrical connections are encapsulated with a molding compound.

As die and grid array densities increase, the desire in packaging semiconductor dies has been to reduce the overall size of the package, allowing the mounted packages to take up less "real estate" or area within a device. A BGA package mounted in a flip chip fashion conserves real estate laterally by eliminating the connection structures (wirebond, TAB, etc) around the package. Conserving real estate vertically presents different challenges. One way this has been accomplished is by reducing the overall height or profile of BGA packages. Another way is by using molded packages with leadframes that can be stacked atop one another.

Stacking BGA packages allows additional lateral real estate to be conserved in exchange for vertical space. The height of a BGA package, including the substrate,

semiconductor die, wirebonds, encapsulant and conductive elements, limits the effectiveness of this method. One example of an attempt to reduce the height of BGA packages in a stack is disclosed in U.S. Patent No. 6,072,233 issued to Corisis et al June 6, 2000. The disclosed packages consist of a semiconductor die mounted face down on a thin substrate. The die is electrically connected to the substrate by centrally located wirebonds, which are encapsulated on the base of the substrate. Solder balls which have a height greater than the combined heights of the mounted semiconductor die and the wirebond encapsulant are spaced along the perimeter of the substrate. By moving the encapsulant to the lower surface of the package and using a thin substrate a fine ball grid array (FBGA) can be used, reducing the overall height of a package. The ability to reduce the height of the package is still limited by the placement and size restrictions on the solder balls, which must have a diameter greater than the combined heights of the semiconductor dies and wirebond encapsulant. The substrate must be rigid to hold the individual packages apart. The solder balls are exposed at the side of the stack, increasing the chances of breakage or contamination.

Therefore, it would be advantageous to develop an apparatus and method that allows for the height of stacked packages to be reduced in comparison to conventional packages. It would further be advantageous for such an apparatus and method to provide for at least enclosing the conductive elements, providing enhanced support as well as protection from breakage and contamination. It would be an additional advantage for certain embodiments of such an apparatus and method to employ at least somewhat flexible substrates, allowing use in increased applications.

DISCLOSURE OF INVENTION

The present invention includes apparatus and methods for preparing semiconductor device packages, or assemblies. An interposer may be constructed from a flexible material, such as a polyimide tape. A pattern of conductive traces is disposed on a first surface of the interposer in electrical communication with a semiconductor die attached to that first surface. Interconnect recesses accessible are opposite, second surface each allow contact with at least one conductive trace. A conductive element, such as a solder ball, disposed substantially within the interconnect recess is used to mechanically and electrically connect the assembly to a carrier substrate or to another,

similar assembly. By substantially receiving the conductive element within the interconnect recess, the height of the completed assembly is reduced.

A number of assemblies may be stacked to form stacked semiconductor arrays. Interconnect structures, such as connection pads, or enlarged traces upon the first surface may allow for interaction between stacked assemblies. Assemblies may be stacked stepwise, or directly aligned.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side view of a substrate useful in assembling some embodiments of devices made in accordance with the principles of the present invention;

FIG. 2 is a sectional side view of a portion of one embodiment of an interposer made in accordance with the principles of the present invention;

FIG. 3 is a sectional side view of one embodiment of a semiconductor package made in accordance with the principles of the present invention, shown prior to mounting;

FIG. 4 is a sectional side view of the embodiment of FIG. 3, as attached to a substrate;

FIG. 5 is a sectional side view of one possible stacked assembly of two alternative embodiments of semiconductor packages made in accordance with the principles of the present invention; and

FIG. 6 is a sectional side view of a portion of another stacked assembly of a fourth alternative embodiment of semiconductor packages made in accordance with the principles of the present invention.

FIG. 7 is a side sectional view of another alternative embodiment of stacked assemblies of semiconductor device packages made in accordance with the principles of the present invention.

BEST MODE OR MODES FOR CARRYING OUT THE INVENTION

Reference will now be made to FIGS. 1 and 2. A portion of an interposer 20 includes a substrate 22 with a recess 30 and adjacent conductive traces 24. Substrate 22 may be formed of any suitable material, including FR-4 resin and bismaleinidetrizaine (BT) resin, among others. In embodiments where it is desired that interposer 20 have

flexibility, the substrate 22 may be formed from a flex material, such as polyimide tape. One such suitable tape is Kapton®, available from E.I. Du Pont Nemours and Company.

A recess 30 is located in a second surface 28 of the interposer body or substrate 22. Adjacent conductive traces 24 are disposed on the opposite, first surface 26 and are accessible through the recess 30. Conductive traces 24 may be in electrical communication with a semiconductor die attached to the interposer 20. Conductive traces 24 may be formed from any suitable material, including metallic traces made of copper alloys or other metals, a conductive epoxy, a plastic material containing conductive particles, or a conductive ink.

A conductive element 32 may be disposed in the recess 30, making an electrical connection with the conductive traces 24 therethrough. Desirably, recess 30 is configured such that a major portion of the conductive element 32 resides substantially within the recess 30. It will be appreciated that conductive element 32 may be formed from any number of electrically conductive attachment materials suitable for use in the interconnection of interposer 20 with higher level packaging. Examples of conductive elements 32 include solder balls and columnar structures of conductive and conductor-filled epoxies, among others. All such suitable conductive elements 32 are within the scope of the present invention.

Where the conductive elements 32 comprise solder balls, the solder balls may be disposed within the recesses by any suitable method. Examples of such methods include: the direct placement of preformed solder balls into a pattern of recesses 30 on the second surface 28; the flooding of the second surface 28 with a plurality of solder balls followed by the removal of those balls protruding more than fixed distance from the second surface 28 and therefore not disposed in a recess 30; and the disposition of a solder paste directly within the recesses 30, followed by reflowing the solder to form spherical elements protruding from the openings of recesses 30 or, if the recesses are sized to constrain formulation of spheres, to form hemispherical protrusions of solder from the mouths of recesses 30. A solder mask may be applied to the second surface 28 to facilitate solder ball formulation in the latter manner.

Recess 30 may be formed in the substrate 22 by any suitable means, including both additive and subtractive methods. In FIG. 1 is depicted a substrate blank 10 that may be used for forming some embodiments of interposers 30 in accordance with the

present invention. Blank 10 includes a substrate layer 12 and a conductive layer 14. Recess 32 may be formed in the substrate layer by the removal of material. For example, substrate layer 12 may be cut with a laser, drilled, punched, chemically etched, or treated with an electroforming chemical to a depth sufficient to expose conductive layers. These subtractive methods may utilize a stencil or patterned resist applied to the substrate layer 12 prior to treatment. In alternative embodiments, the substrate 22 may be formed from an additive method, with the recess 30 preformed in the substrate material and laminated to a conductive layer thru the use of tape adhesive.

Conductive traces 24 may similarly be formed by any suitable method, including both additive and subtractive methods. In FIG.1, the conductive layer 14 may be etched to form a desired pattern of conductive traces 24. This may be accomplished by applying a stencil or by patterning a and then removing conductive material through a chemical etch or other means. In alternative embodiments, the pattern of conductive traces 24 may be formed by depositing the conductive traces 24 on the substrate 22. Any suitable additive technique can be used, such as by preforming the traces 24 or by etching or stamping and applying them to substrate 22, by applying a conductive polymer to form devices, by printing with a conductive ink, or otherwise as known in the art.

FIGS. 3 and 4 depict a semiconductor assembly 40 made in accordance with the principles of the present invention. It will be appreciated that FIGS. 3 and 4 are not to scale, but are only representative. A semiconductor die 54 is attached to an interposer 42. In the depicted embodiment, the semiconductor die 54 is attached in a flip chip fashion, depicted by conductive columns 56, although it will be appreciated that any method known to those skilled in the art may be used and all such methods are within the scope of the present invention. A pattern of conductive traces 40 is disposed on the first surface 46 of the interposer 42. Recesses 50 are located on opposite surface 48. Each of the conductive elements 52 residing substantially within the recesses 50 make electrical contact with at least one of the conductive traces 44, traces 44 being in electrical communication with the semiconductor die 54 through conductive columns 56. The positioning of a number of recesses 50 on the interposer 42 may be used to provide a grid array, such as a ball grid array (BGA) or

fine ball grid array (FBGA), for attachment and interconnection of the assembly 40 to higher level packaging.

Semiconductor assembly 40 may be attached to higher level packaging in the form of a carrier substrate S, which may be a printed circuit board (PCB) or any other suitable structure. Assembly 40 is placed on the substrate S, such that the conductive elements 52 are located on and bonded to conductive attachment points, such as the contact pads 58. It will be appreciated that in addition to contact pads 58, the attachment points may be formed of any suitable structure, including conductive traces, among others. In embodiments where the conductive elements 52 are solder balls, this may be accomplished by reflowing the solder.

The positioning of conductive elements 52 substantially within the recesses 50 allows the interposer 42 to be mounted closely to the substrate S, reducing the overall height of the assembly 40. In certain embodiments, the interposer 40 second surface 48 may even be disposed directly on the substrate S. This may be accomplished as solder ball conductive elements are reflowed and flow to fill any space remaining around the solder ball within the recess 50. With embodiments where the interposer 42 has reduced rigidity, as when formed from a polymide tape, the assembly 40 may flex towards the substrate S, further reducing the overall height.

FIG. 5 depicts a side, cross sectional view of a stack of semiconductor assemblies fabricated in accordance with the principles of the present invention. It will be appreciated that FIG. 5, like the other figures in the present application, is not to scale but is instead representational of the principles of the present invention. A first semiconductor assembly 70 is attached to a substrate S, as discussed above with respect to FIGS. 2 and 3. Conductive elements 82, substantially residing within recesses 80 are connected to contact pads 88 of the substrate S. A semiconductor die 84 is disposed on a first surface 76 of the interposer 72 and is in electrical communication with the conductive element 82 through the conductive traces 74. Interposer 72 of assembly 70 includes an interconnect structure allowing for connection with another assembly 100 stacked on the first surface 76. In the depicted embodiment, the interconnect structure is represented by the interconnect pads 92. Interconnect pads 92 function similar to contact pads 88, allowing another semiconductor assembly to be electrically attached thereto. Interconnect pads 92 may be connected to the pattern of conductive traces 74,

and to conductive elements 82 therethrough, or may be directly connected to a recess 80, with a conductive element therein. Alternatively, a via or other connective structure may be used to connect the stacked assembly with either the substrate S or the first assembly 70.

A second semiconductor assembly 100 is stacked adjacent the first assembly 70. Second assembly 100 includes a semiconductor die 114 attached to the first surface 106 of an interposer 102. The semiconductor die 114 is in electrical communication with a pattern of conductive traces 104, located on the first surface 106, depicted in this embodiment through the wirebond connection 115. Recesses 110 are disposed in the second surface 108 and pass through the body of the interposer 102 to allow communication with the conductive traces 104. Each recess 110 may allow electrical communication with one or more conductive traces 104. Conductive elements 112 are disposed in the recesses 110 and may be used for attachment of the assembly 100 and electrical communication with the semiconductor die 114. Note that second assembly 100 includes a solder mask 109 disposed adjacent to the second surface 108 for facilitating the formation of conductive elements 112.

The second assembly further includes a die recess 90 accessible on the second surface 108. Die recess 90 may be formed in any suitable manner, as discussed above with respect to the interconnection recesses 110. The die recess 90 is configured to contain at least a portion of die 84. The dimensions of the die recess 90 may vary with different embodiments to accomplish this purpose. If necessary, die recess 90 may extend to or even through the first surface 106, desirably at a location other than die 114, or conductive traces 104.

Second assembly 100 is positioned with second surface 102 adjacent to the first surface 76 of the first assembly 70. Second assembly 100 is positioned such that conductive elements 112 are aligned with the interconnect pads 92, and die recess 90 is aligned with die 84. Conductive elements 112 are then bonded to the interconnect pads 92, coupling the assemblies into a stacked array, and establishing electrical communication therebetween the assemblies 70 and 100 and the substrate S.

Turning to FIG. 6, there is depicted a portion of a stack 120 of semiconductor assemblies 128 and 158. The first semiconductor assembly, 158 includes a semiconductor die 164 attached to the first surface 166 of an interposer 160.

Semiconductor die 164 is in electrical communication with a pattern of conductive traces 174 disposed on the first surface. A recess 170 is accessible on the second opposite surface 168 of the interposer. A conductive element 172 is disposed substantially within the recess. Note that in the depicted embodiment die 164 is encapsulated with an encapsulant material 163, providing additional protection to the die 164. First assembly 158 is attached to a substrate S, with conductive element 172 bonded to contact pad 178 of substrate S, and second surface 168 adjacent to substrate S. It will be appreciated that the embodiment of first assembly 158, as shown in FIG. 6, may include a plurality of recesses 170 and conductive elements 172 forming an array, such as a ball grid array. All such embodiments are included within the scope of the present invention.

Second semiconductor assembly 128 similarly includes a semiconductor die 134 attached to the first surface 136 of interposer 130. Die 134 is in electrical communication with at least one member of a pattern of conductive traces 144 disposed on first surface 136, depicted here by wirebond 135. Die 134 and the electrical connection to the conductive traces may be encapsulated with an encapsulant material 133. An interconnect recess 150 is accessible on the opposite second surface 148 and passes into the body of the interposer 130. At least one member of the conductive traces 144 is accessible through the interconnect recess 150. A conductive element, such as solder ball 152 is disposed in the interconnect recess 150, in an electrically communicative connection with at least one member of the conductive traces 144. It will be appreciated that second assembly 130 may include any number of interconnect recesses 150 and solder balls 152, forming a grid array on the second surface 148 for connection of the assembly 128.

A stack assembly 120 is formed by attaching the second surface 148 of second assembly 128 to the first surface 166 of first assembly 158. Recess 150 is aligned with an interconnect structure, allowing the assemblies to be attached in electrical communication, through solder ball 152. In the embodiment depicted in FIG. 6, the interconnect structure is represented as one or more members of conductive traces 174 disposed on first surface 166 of the first assembly 158. As discussed above, the interconnect structure may be any structure known, or readily ascertainable, to those skilled in the art that may be used establishing electrical communication between first

assembly 158 and second assembly 128. All such structures are within the scope of the present invention.

As solder ball 152 is reflowed to attach the interconnect structures of the pattern of conductive traces 174, any space remaining within recess 150 is filled by solder. This allows second surface 148 to draw closer to the first surface 166, further reducing the height of the stacked assembly 120. In embodiments where interposer 130 is constructed from a flexible material, such as a polyimide tape, the reduced rigidity of second assembly 128 allows further reduction in height. A non-rigid embodiment of first assembly 128 is able to flex and adjust within the available space, drawing closer to the adjacent first assembly 158. Through these attributes, some embodiments of the present invention may be used to create stacks of semiconductor assemblies with a reduction in the overall height of the stacked assemblies, conserving real estate in a device in both lateral and vertical directions.

Turning to FIG. 7 is depicted a side, cross sectional view of multiple component stack of semiconductor assemblies fabricated in accordance with the principles of the present invention. It will be appreciated that FIG. 7, like the other figures in the present application, is not to scale but is instead representational of the principles of the present invention. Similar to FIG. 5, a first semiconductor assembly 220 is attached to a substrate S, which may be a printed circuit board (PCB) or similar structure, as discussed elsewhere herein. Conductive elements 222, substantially residing within recesses 221 are connected to contact pads 304 of the substrate S, on first surface 301 thereof. A semiconductor die 228 is disposed on a first surface 227 of the interposer 226 and is in electrical communication with the conductive element 222 through the conductive traces 224. Interposer 226 includes an interconnect structure allowing for connection with another assembly 210 stacked on the first surface 227. In the depicted embodiment, the interconnect structure is represented by the interconnect pads 224, as discussed with respect to FIGS. 5 and 6.

A second semiconductor assembly 210 is stacked adjacent the first assembly 220. Second assembly 210 includes a semiconductor die 218 attached to the first surface 217 of an interposer 216. The semiconductor die 218 is in electrical communication with a pattern of conductive traces 214, located on the first surface 217, depicted in this embodiment through the wirebond connection 219. Recesses 211 are disposed in the

second surface 215 and pass through the body of the interposer 216 to allow communication with the conductive traces 214. Each recess 211 may allow electrical communication with one or more conductive traces 214. Conductive elements 212 are disposed in the recesses 211 and may be used for attachment of the assembly 210 and electrical communication with the semiconductor die 218. Second assembly 210 may include a die recess as in the embodiment of FIG. 5.

Second assembly 210 is positioned with second surface 215 adjacent to the first surface 227 of the first assembly 220. Second assembly 210 is positioned such that conductive elements 212 are aligned with the interconnect pads 224. Conductive elements 212 are then bonded to the interconnect pads 224, coupling the assemblies into a stacked array, and establishing electrical communication therebetween the assemblies 210 and 220 and the substrate S.

Similarly, a stack of semiconductor assemblies fabricated in accordance with the principles of the present invention is located at a second surface 302 of the substrate S. A third semiconductor assembly 240 is attached to the second surface 302 of substrate S. Conductive elements 242, substantially residing within recesses 241 are connected to contact pads 305 of the substrate S, on the second surface 302. A semiconductor die 248 is disposed on a first surface 247 of the interposer 246 and is in electrical communication with the conductive element 242 through the conductive traces 244. Interposer 246 includes an interconnect structure allowing for connection with another assembly 250 stacked on the second surface 249. In the depicted embodiment, the interconnect structure is represented by the interconnect pads 243 located on the second surface 249 and similar to those discussed previously herein.

A fourth semiconductor assembly 250 is stacked adjacent the first assembly 240. Fourth assembly 250 includes a semiconductor die 258 attached to the first surface 257 of an interposer 256. The semiconductor die 258 is in electrical communication with a pattern of conductive traces 254, located on the first surface 257, depicted in this embodiment through the wirebond connection 259. Recesses 251 are disposed in the first surface 255 and contain a conductive elements 252 protruding slightly therefrom. Conductive elements 252 may be used for attachment of the assembly 250 and electrical communication with the semiconductor die 258. Third assembly 240 may include a die recess as in the embodiment of FIG. 5.

Fourth assembly 250 is positioned with first surface 255 adjacent to the second surface 249 of the third assembly 240. Fourth assembly 250 is positioned such that conductive elements 252 are aligned with the interconnect pads 243. Conductive elements 252 are then bonded to the interconnect pads 243, coupling the assemblies into a stacked array, and establishing electrical communication therebetween the assemblies 240 and 250 and the substrate S.

It will be appreciated that the stacked assemblies 210, 220, 230 and 240 are representational only and that as many assemblies as desired may be utilized to forma stacks on a surface of a substrate S. By stacking multiple assemblies on the different surfaces of the substrate S, further reductions of the amount of space consumed by an assembly inside an electronic device may be realized.

In accordance with the description provided, the present invention includes a method of forming a stackable semiconductor assembly with recessed interconnections. This method may be practiced by providing a substrate to form an interposer body having first and second surfaces, then disposing electrically conductive traces on the first surface, disposing a stacking electrical interconnection structure on the first surface and forming a connection recess in the second surface and passing through the interposer body to expose at least one exposed electrically conductive trace disposed on the first surface. A semiconductor die is then provided to the first surface, such that said semiconductor die is in electrical communication with at least one connecting electrically conductive trace disposed on the first surface then an electrically conductive connection material is disposed substantially within the connection recess, such that the electrically conductive material is in electrically conductive contact with the at least one exposed one electrically conductive trace.

When the method is practiced, a number of options may be utilized to optimize the procedure. For example, the die may be attached in conventional or flip chip fashion. The act of disposing the electrically conductive compound in the connection recess could include disposing the electrically conductive compound in electrically conductive contact with the at least one connecting electrically conductive trace. The electrically conductive compound connection may be a solder paste disposed in the recesses and reflowed to form solder balls. The substrate may be a polyimide flex tape, or other material. The electrically conductive traces could be formed by etching a

metallic layer disposed on the first surface or by disposing traces directly upon the first surface. An electrically conductive trace may serve as the interconnect structure, or a separate connection pad may be used. Further, a die recess may be formed in the second surface, if desired. It will be appreciated that these options are illustrative only and that other useful options known or readily ascertainable to those skilled in the art may be used.

Further, it will be appreciated that the present invention includes a method of forming a semiconductor assembly. This method may be practiced by providing a nonrigid substrate to form an interposer body having first and second surfaces, disposing electrically conductive traces on the first surface and forming a connection recess in the second surface and passing through the interposer body to expose at least one exposed electrically conductive trace disposed on the first surface. A semiconductor die is then provided and attached to the first surface in electrical communication with at least one connecting electrically conductive trace. Next, an electrically conductive connection compound is disposed substantially within the connection recess in electrically conductive contact with the at least one exposed one electrically conductive trace.

As above, when this method is practiced, a number of options can be utilized to optimize the procedure. For example, the die may be attached in conventional or flip chip fashion. The act of disposing the electrically conductive compound in the connection recess could include disposing the electrically conductive compound in electrically conductive contact with the at least one connecting electrically conductive trace. The electrically conductive compound connection may be a solder paste disposed in the recesses and reflowed to form solder balls, this process may be aided with the application of a solder mask to the second surface. Alternatively, the second surface may be flooded with solder balls, followed by the removal of those that protrude above a certain distance. The substrate may be a polyimide flex tape, or other material. The electrically conductive traces may be formed by etching a metallic layer disposed on the first surface or by disposing traces directly upon the first surface. An electrically conductive trace may serve as the interconnect structure, or a separate connection pad may be used. Further, a die recess may be formed in the second surface, if desired. It will be appreciated that these options are illustrative only and that other useful options known or readily ascertainable to those skilled in the art may be used.

It will be appreciated that the present invention also includes a method of forming a stack of semiconductor assemblies. A first semiconductor assembly is assembled by taking a first substrate to form a first interposer body having first and second surfaces, disposing first electrically conductive traces on the first surface, forming at least a first connection recess in the second surface and passing through the first interposer body to expose at least one exposed first electrically conductive trace disposed on the first surface, providing a first semiconductor die, attaching the first semiconductor die to the first surface in electrical communication with at least one connecting first electrically conductive trace disposed on the first surface, disposing an electrically conductive connection compound substantially within the at least first connection recess and in electrically conductive contact with the at least one exposed first electrically conductive trace. A second semiconductor assembly is assembled by taking a second substrate to form a second interposer body having third and fourth surfaces, disposing second electrically conductive traces on the third surface, disposing at least a first stacking electrical interconnection structure on the third surface, forming at least a second connection recess in the fourth surface and passing through the second interposer body to expose at least one exposed second electrically conductive trace disposed on the third surface, providing a second semiconductor die, attaching the second semiconductor die to the third surface in electrical communication with at least one connecting second electrically conductive trace disposed on the second surface, and disposing an electrically conductive connection compound substantially within the at least second connection recess and in electrically conductive contact with the at least one exposed one second electrically conductive trace. The second surface of the first semiconductor assembly is attached to the third surface of the second semiconductor assembly, such that the at least first recess is aligned with the stacking electrical interconnection structure, and the electrically conductive connection compound disposed within the at least first recess makes electrically conductive contact to the at least first stacking electrical interconnection structure.

It will be apparent that details of the apparatus and methods herein described can be varied considerably without departing from the concept and scope of the invention. The claims alone define the scope of the invention as conceived and as described herein.

CLAIMS

What is claimed is:

1. A semiconductor assembly comprising:

a semiconductor die;

a nonrigid interposer comprising an interposer body having a first surface and a second surface, the interposer further comprising:

electrically conductive traces disposed on the first surface, at least one electrically conductive trace being electrically connected to the semiconductor die;

a connection recess formed in the second surface and passing through the interposer body to expose at least one electrically conductive trace disposed on the first surface;

a die recess formed in the second surface, the die recess sized and configured to receive a portion of a semiconductor die on another semiconductor assembly therein; and

an electrically conductive material disposed substantially within the connection recess, in contact with the at least one exposed electrically conductive trace.

2. The semiconductor assembly of claim 1, wherein the semiconductor die is disposed on the second surface.

3. The semiconductor assembly of claim 1, wherein at least one exposed electrically conductive trace comprises the at least one electrically connected electrically conductive trace.

4. The semiconductor assembly of claim 1, wherein the semiconductor die is electrically connected with the at least one electrically connected electrically conductive trace by a wirebond connection.

5. The semiconductor assembly of claim 1, wherein the semiconductor die is disposed on the first surface.

6. The semiconductor assembly of claim 5, wherein the semiconductor die is flip chip attached to the first surface.

7. The semiconductor assembly of claim 6, wherein the semiconductor die is attached to the first surface by at least one solder connection to the at least one connected electrically conductive trace.

8. The semiconductor assembly of claim 1, wherein the electrically conductive material comprises a solder.

9. The semiconductor assembly of claim 1, wherein the interposer body comprises a flex tape.

10. The semiconductor assembly of claim 9, wherein the flex tape comprises a polyimide tape.

11. The semiconductor assembly of claim 1, wherein the electrically conductive traces comprise metallic traces disposed on the first surface.

12. The semiconductor assembly of claim 11, wherein the metallic traces comprise a copper alloy.

13. The semiconductor assembly of claim 1, further comprising an encapsulant disposed over and encapsulating the semiconductor die.

14. An interposer comprising:

a nonrigid interposer body having a first surface and a second surface;

electrically conductive traces disposed on the first surface;

a connection recess formed in the second surface and passing through the interposer body to expose at least one of the electrically conductive traces disposed on the first surface, the connection recess having sufficient volume to substantially contain a solder ball protruding therefrom; and

a die recess formed in the second surface and passing into the interposer body, the die recess sized and configured to receive at least a portion of a semiconductor die attached to a semiconductor assembly separate from the interposer therein.

15. The interposer of claim 14, wherein the interposer body comprises a flex tape.

16. The interposer of claim 15, wherein the flex tape comprises a polyimide tape.

17. The interposer of claim 14, wherein the electrically conductive traces comprise metallic traces disposed on the first surface.

18. The interposer of claim 17, wherein the metallic traces comprise a copper alloy.

19. A method of forming a semiconductor assembly comprising:

forming an interposer body having first and second surfaces from a nonrigid substrate;

disposing a plurality of electrically conductive traces on the first surface of the interposer body;

forming a plurality of connection recesses from the second surface passing through the interposer body to respectively expose a portion of one of the plurality of electrically conductive traces ;

disposing a preformed solder ball in each of the plurality of connection recesses;

heating the solder balls disposed in the recesses of the plurality to reflow and protrude slightly beyond a mouth of each connection recess; and

attaching a semiconductor die to the first surface of interposer body and placing the semiconductor die in electrical communication with at least one of the plurality of electrically conductive traces.

20. The method of claim 19, further comprising disposing an encapsulant over the semiconductor die.

21. The method of claim 19, wherein attaching the semiconductor die to the first surface comprises attaching the semiconductor die to the first surface with an adhesive and placing the semiconductor die in electrical communication with the at least one of the electrically conductive traces comprises forming a wirebond connection between the semiconductor die and the at least one of the plurality of electrically conductive traces.

22. The method of claim 19, wherein attaching the semiconductor die to the first surface and placing the semiconductor die in electrical communication with the at least one of the electrically conductive traces comprises attaching the semiconductor die in flip chip fashion to the first surface with an electrically conductive material to make an electrical and mechanical connection between the semiconductor die and the at least one of the plurality of electrically conductive traces.

23. The method of claim 22, wherein attaching the semiconductor die to the first surface and placing the semiconductor die in electrical communication with the at least one of the electrically conductive traces comprises disposing the semiconductor die bearing an array of solder balls on the first surface and reflowing the solder balls to electrically and mechanically connect the semiconductor die to the at least one of the plurality of electrically conductive traces.

24. The method of claim 19, wherein forming an interposer body from a nonrigid substrate comprises forming the interposer body from a polyimide flex tape.

25. The method of claim 19, wherein disposing a plurality of electrically conductive traces comprises forming metallic traces on the first surface.

26. The method of claim 25, wherein forming metallic traces comprises etching a metallic layer disposed on the first surface.

27. A semiconductor assembly comprising:

a semiconductor die;

an interposer comprising an interposer body having a first surface and a second surface, the interposer further comprising:

electrically conductive traces disposed on the first surface, at least one electrically conductive trace being electrically connected with the semiconductor die,

a stacking electrical interconnection structure for making electrical connection to a second interposer disposed on the first surface,

a die recess formed in the second surface of the interposer and passing into the interposer body, the die recess sized and configured to receive at least a portion of a semiconductor die attached to another semiconductor assembly therein,

a connection recess formed in the second surface and passing through the interposer body to expose at least one electrically conductive trace disposed on the first surface; and

an electrically conductive material disposed substantially within the connection recess in contact with the exposed at least one electrically conductive trace.

28. The semiconductor assembly of claim 27, wherein the semiconductor die is disposed on the second surface.

29. The semiconductor assembly of claim 27, wherein at least one exposed electrically conductive trace comprises the at least one electrically connected electrically conductive trace.

30. The semiconductor assembly of claim 27, wherein the semiconductor die is in electrical connection with the at least one electrically connected electrically conductive trace by a wirebond connection.

31. The semiconductor assembly of claim 27, wherein the semiconductor die is disposed on the first surface.

32. The semiconductor assembly of claim 31, wherein the semiconductor die is mounted in flip chip fashion on the first surface.

33. The semiconductor assembly of claim 32, wherein the semiconductor die is attached to the first surface by a soldered connection that electrically connects the semiconductor die to the at least one connected electrically conductive trace.

34. The semiconductor assembly of claim 27, wherein the stacking electrical interconnection structure comprises an electrical connection pad.

35. The semiconductor assembly of claim 27, wherein the stacking electrical interconnection structure comprises an electrically conductive trace disposed on the first surface.

36. The semiconductor assembly of claim 27, wherein the electrically conductive material comprises a solder.

37. The semiconductor assembly of claim 27, wherein the interposer body comprises a flex tape.

38. The semiconductor assembly of claim 37, wherein the flex tape comprises a polyimide tape.

39. The semiconductor assembly of claim 27, further comprising a die recess formed in the second surface and the interposer body, the die recess configured to contain at least a portion of a second semiconductor die.

40. The semiconductor assembly of claim 27, wherein the electrically conductive traces comprise metallic traces disposed on the first surface.

41. The semiconductor assembly of claim 40, wherein the metallic traces comprise a copper alloy.

42. The semiconductor assembly of claim 27, further comprising an encapsulant material encapsulating the semiconductor die.

43. An interposer comprising:

an interposer body having a first surface and a second surface, electrically conductive traces disposed on the first surface, and a stacking electrical interconnection structure disposed on the first surface;

a die recess formed in the second surface and the interposer body, the die recess configured to receive and contain at least a portion of a semiconductor die attached to another interposer; and

a connection recess formed in the second surface and passing through the interposer body to expose at least one of the electrically conductive traces disposed on the first surface, the connection recess configured to contain a solder ball substantially within the connection recess.

44. The interposer of claim 43, wherein the stacking electrical interconnection structure comprises an electrical connection pad.

45. The interposer of claim 43, wherein the stacking electrical interconnection structure comprises an electrically conductive trace disposed on the first surface.

46. The interposer of claim 43, wherein the interposer body comprises a flex tape.

47. The interposer of claim 46, wherein the flex tape comprises a polyimide tape.

48. The interposer of claim 43, further comprising a die recess formed in the second surface and the interposer body, the die recess configured to contain at least a portion of a semiconductor die.

49. The interposer of claim 43, wherein the electrically conductive traces comprise metallic traces disposed on the first surface.

50. The interposer of claim 49, wherein the metallic traces comprise a copper alloy.

51. An interposer comprising:

an interposer body having a first surface and a second surface;

electrically conductive traces disposed on the first surface, the traces in electrical communication with a conductive element accessible on the second surface; and

a die recess formed in the second surface and the interposer body, the die recess configured to receive and contain at least a portion of a semiconductor die attached to an interposer of another semiconductor assembly.

52. A method of forming a semiconductor assembly comprising:

forming an interposer body having a first surface and a second surface from a nonrigid substrate;

disposing a plurality of electrically conductive traces on the first surface;

disposing a plurality of electrically conductive interconnect structures on the first surface at locations laterally offset from locations of connection recesses;

forming a plurality of connection recesses from the second surface passing through the interposer body to respectively expose a portion of one of the plurality of electrically conductive traces;

disposing an electrically conductive material in the form of a solder within each of the plurality of connection recesses in a volume sufficient to reside substantially within each of the plurality of connection recesses;

heating the solder within each of the plurality of connection recesses to reflow and protrude slightly beyond a mouth of each recess; and

attaching a semiconductor die to the first surface of the interposer body, placing the semiconductor die in electrical communication with at least one of the plurality of electrically conductive traces.

53. The method of claim 52, further comprising disposing an encapsulant over the semiconductor die.

54. The method of claim 52, wherein attaching the semiconductor die to the interposer body comprises attaching the semiconductor die to the first surface with an adhesive and placing the semiconductor die in electrical communication with at least one of the plurality of conductive traces comprises forming a wirebond connection between the semiconductor die and the at least one of the plurality of electrically conductive traces.

55. The method of claim 52, wherein attaching the semiconductor die to the first surface and placing the semiconductor die in electrical communication with the at least one of the plurality of electrically conductive traces comprises attaching the semiconductor die in flip chip fashion on the first surface with an electrically conductive material to make an electrical and mechanical connection between the semiconductor die and the at least one of the plurality of electrically conductive traces.

56. The method of claim 55, wherein attaching the semiconductor die to the first surface and placing the semiconductor die in electrical communication with the at least one of the plurality of electrically conductive traces comprises disposing the semiconductor die bearing an array of solder balls on the first surface and reflowing the solder balls to electrically and mechanically connect the semiconductor die to the at least one of the plurality of electrically conductive traces.

57. The method of claim 52, wherein disposing a plurality of electrically conductive interconnect structures comprises disposing a plurality of electrical connection pads on the first surface.

58. The method of claim 52, wherein disposing a plurality of electrically conductive interconnect structures comprises disposing a second plurality of electrically conductive traces on the first surface.

59. The method of claim 52, wherein disposing a solder within each of the connection recesses comprises flooding the second surface with a plurality of solder balls and then removing solder balls not residing substantially within one of the plurality of connection recesses.

60. The method of claim 52, wherein disposing solder within each of the plurality of connection recesses comprises disposing a solder paste within each of the connection recesses.

61. The method of claim 60, further comprising disposing a solder mask over the second surface, prior to disposing the solder.

62. The method of claim 52, wherein providing a nonrigid substrate to form an interposer body comprises providing a polyimide flex tape.

63. The method of claim 52, further comprising forming a recess in the second surface sized and configured to receive at least a portion of a semiconductor die therein.

64. The method of claim 52, wherein disposing a plurality of electrically conductive traces comprises forming metallic traces on the first surface.

65. The method of claim 64, wherein forming metallic traces comprises etching a metallic layer disposed on the first surface.

66. A method of forming a stacked semiconductor assembly comprising:

forming a first semiconductor assembly by:

forming a first interposer body having first and second surfaces from a nonrigid substrate,

forming a die recess in the second surface sized and configured to receive at least a portion of a semiconductor die therein,

disposing first electrically conductive traces on the first surface,

forming at least a first connection recess from the second surface passing through the first interposer body to expose a portion of at least one first electrically conductive traces disposed on the first surface,

attaching a first semiconductor die to the first surface in electrical communication with at least one first electrically conductive traces disposed on the first surface, and

disposing an electrically conductive material substantially within the at least first connection recess and in electrically conductive contact with the exposed portion of the at least one first electrically conductive trace;

forming a second semiconductor assembly by:

forming a second interposer body having third and fourth surfaces from a nonrigid substrate,

disposing second electrically conductive traces on the third surface,

disposing at least a first stacking electrical interconnection structure on the third surface,

forming at least a second connection recess from the fourth surface passing through the second interposer body to expose a portion of at least one second electrically conductive trace disposed on the third surface,

attaching a second semiconductor die to the third surface in electrical communication with at least one second electrically conductive trace disposed on the third surface,

disposing an electrically conductive material substantially within the at least second connection recess and in electrically conductive contact with the at least one exposed one second electrically conductive trace; and

superimposing the first semiconductor assembly on the second semiconductor assembly, such that at least a portion of the second semiconductor die is received within the die recess, the at least first recess is aligned with the stacking electrical interconnection structure, and the electrically conductive material disposed within the at least first recess makes electrically conductive contact to the at least first stacking electrical interconnection structure.

67. The method of claim 66, wherein forming a die recess in the second surface sized and configured to receive at least a portion of a semiconductor die recess therein is effected concurrently with forming the at least a first connection recess.

68. The method of claim 66, wherein receiving the at least a portion of the second semiconductor die within the die recess aligns the at least first connecting recess with the at least first stacking electrical interconnection structure.

69. The method of claim 66, wherein disposing the electrically conductive material in the at least first connection recess comprises disposing the electrically conductive material in electrically conductive contact with the at least one connecting electrically conductive trace.

70. The method of claim 66, wherein disposing at least a first stacking electrical interconnection structure comprises disposing an electrical connection pad.

71. The method of claim 70, wherein disposing at least a first stacking electrical interconnection structure comprises disposing an electrically conductive trace on the first surface.

72. The method of claim 66, wherein disposing an electrically conductive material substantially within the at least first connection recess comprises disposing solder within the at least first connection recess.

73. The method of claim 72, wherein disposing solder within the at least first connection recess comprises flooding the second surface with a number of solder balls and then removing solder balls not disposed substantially within the at least first connection recess.

74. The method of claim 72, wherein disposing solder substantially within the at least first connection recess comprises disposing a solder paste within the at least first connection recess and then reflowing the solder to form a solder ball.

75. The method of claim 74, further comprising disposing a solder mask over the second surface, prior to disposing the solder paste.

76. The method of claim 66, wherein forming the first interposer body from a nonrigid substrate comprises using a polyimide flex tape.

77. The method of claim 66, wherein forming the second interposer body from a nonrigid substrate comprises using a polyimide flex tape.

78. The method of claim 66, wherein disposing first electrically conductive traces comprises forming first metallic traces on the first surface.

79. The method of claim 78, wherein forming first metallic traces comprises etching a first metallic layer disposed on the first surface.

80. The method of claim 79, wherein disposing second electrically conductive traces comprises forming second metallic traces on the third surface.

81. The method of claim 80, wherein forming second metallic traces comprises etching a second metallic layer disposed on the third surface.

82. A method of forming a stacked semiconductor assembly comprising:
forming a first semiconductor assembly by:

forming a first interposer body having first and second surfaces from a nonrigid substrate,

disposing at least a first electrically conductive trace on the second surface,

forming at least a first connection recess from the first surface passing through the first interposer body to expose a portion of at least one first electrically conductive trace disposed on the second surface,

forming a die recess in the first surface sized and configured to receive at least a portion of a semiconductor die therein,

attaching a first semiconductor die to the second surface,

disposing an electrically conductive material substantially within the at least first connection recess and in electrically conductive contact with the exposed portion of the at least one first electrically conductive trace;

forming a second semiconductor assembly by:

forming a second interposer body having third and fourth surfaces from a second nonrigid substrate,

disposing at least a first electrically conductive trace on the fourth surface,

disposing at least a first stacking electrical interconnection structure on the fourth surface,

forming at least a second connection recess from the third surface passing through the second interposer body to expose at least one second electrically conductive trace disposed on the fourth surface,

attaching a second semiconductor die to the fourth surface,

disposing an electrically conductive material substantially within the at least second connection recess and in electrically conductive contact with the exposed portion of the at least one second electrically conductive trace; and

superimposing the first semiconductor assembly on the second semiconductor assembly, with at least a portion of the second semiconductor die received within the die recess, the at least first recess aligned with the stacking electrical interconnection structure, and the electrically conductive material disposed within the at least first recess making electrically conductive contact to the at least first stacking electrical interconnection structure.

83. The method of claim 82, wherein forming a die recess in the first surface is effected concurrently with forming the at least a first connection recess.

84. The method of claim 82, wherein receiving the at least a portion of the second semiconductor die within the die recess aligns the at least first connecting recess with the at least first stacking electrical interconnection structure.

85. The method of claim 82, wherein disposing the electrically conductive material in the at least first connection recess comprises disposing the electrically conductive material in electrically conductive contact with the at least one connecting electrically conductive trace.

86. The method of claim 82, wherein disposing at least a first stacking electrical interconnection structure comprises disposing an electrical connection pad.

87. The method of claim 82, wherein disposing at least a first stacking electrical interconnection structure comprises disposing an electrically conductive trace on the third surface.

88. The method of claim 82, wherein disposing an electrically conductive material substantially within the at least first connection recess comprises disposing solder within the at least first connection recess.

89. The method of claim 88, wherein disposing solder substantially within the at least first connection recess comprises disposing a solder paste within the at least first connection recess and then reflowing the solder to form a solder ball.

90. The method of claim 89, further comprising disposing a solder mask over the first surface, prior to disposing the solder paste.

91. The method of claim 82, wherein forming the first interposer body from a nonrigid substrate comprises using a polyimide flex tape.

92. The method of claim 82, wherein forming the second interposer body from a second nonrigid substrate comprises using a polyimide flex tape.

93. The method of claim 82, wherein disposing first electrically conductive traces comprises forming first metallic traces on the second surface.

94. The method of claim 93, wherein forming first metallic traces comprises etching a first metallic layer disposed on the second surface.

95. The method of claim 93, wherein disposing second electrically conductive traces comprises forming second metallic traces on the fourth surface.

96. The method of claim 95, wherein forming second metallic traces comprises etching a second metallic layer disposed on the fourth surface.