The invention relates to a control circuit for a liquid crystal display.

Known liquid crystal displays comprise two substrates which are disposed at a defined distance from one another. A liquid crystal material is located between the substrates. The substrates are selected in dependence on the application such that one or both can be seen through i.e. that one or both is transparent. A transparent earth plane conductor is disposed on one of these substrates. The opposite substrate comprises a matrix of individual electrode elements which are called pixel electrodes. A semiconductor switch, preferably a thin film transistor, is associated with each of these pixel electrodes and is disposed on the substrate including these electrodes. These transistor switches are constructed either from amorphous silicon or polycristalline silicon. The amorphous silicon technology is to be preferred for general consumer applications because of the much lower operating temperatures. The individual pixel electrodes of the matrix function in effect as capacitors using the liquid crystal material as a dielectric. The application of a voltage to a pixel electrode controls the transparency of the liquid crystal material. This transformation or regrouping of the liquid crystals enables text or graphical information to be displayed which is then visible on the device. An individual semiconductor switch, which can be switched on or off, is associated with each pixel element so that each individual pixel element can be controlled by signals which are supplied to its associated semiconductor switch.

Each transistor is a crossing point of a column m and a row n of the matrix. The columns m are data lines, the rows n being selection lines. The control electrode of each one of the transistor switches is connected to a selection line and the source or drain electrode of the transistor switch is connected to a data line. The drain or source electrode is connected to the pixel electrode.

In operation, a signal level is applied continuously to each of the data lines for writing a row. The scanning lines are activated continuously in order for the voltages occurring on the data lines to be applied to the pixel electrodes via their corresponding semiconductor switching elements. When, for example, an item of picture information is to be reproduced, the voltages representing the grey values for example, are applied to the data lines and the scanning lines are activated during the rows that are to be written in correspondence therewith. After a short, but necessary, charging time for the liquid crystal capacitor, another scanning line is activated and the associated data voltages for this row are applied sequentially to the pixel columns. In the case of television applications, this writing process takes place from top to bottom in e.g. $1/25^{th}$ or $1/50^{th}$ of a second. Consequently, a complete picture is displayed on the screen during this time period.

Parasitic capacitances, which influence the signal transmission from the data lines to the liquid crystal capacitors in an undesired manner, are associated with the capacitance of the liquid crystal capacitor. On the one hand there are parasitic capacitances between the data lines and the pixel electrodes and secondly, there are the parasitic gate / source and gate / drain capacitances in the switching element itself. During the operation of a display of this type, the voltage is applied to a pixel merely while it is being addressed. The semiconductor switch is then blocked and the voltage has to remain constant until such time as the row is written afresh during the renewed build-up of the picture.

A minimum charging time is required in order to charge up the liquid crystal capacitor to the voltage value determined by the information on the data line as well as to charge up the parasitic capacitances. This charging time cannot be arbitrarily shortened due to the very low mobility exhibited by the amorphous silicon being used.

A control circuit for a liquid crystal display, which consists of an active matrix display and comprises signal driver circuits for the rows and columns, is known from EP-A1-0 298 255. The column control circuit comprises shift registers and also two sample-and-hold circuits for each column. The items of data for a row are written into the first sample-and-hold circuit sequentially. After the row has been written, its entire contents are transferred to the second sample-and-hold circuit which then controls the liquid crystal display elements. In this process, it is necessary to take care that the voltage of the first column is kept constant for a long time, i.e. until the sample-and-hold circuit of the last column has loaded. In addition to this, an individual terminal lead has to be used for each column.

In the EP-A-0 238 867, a group of successive columns form a respective block. The analogue picture signals being supplied are buffer stored blockwise in column capacitors until the respective items of data for a complete row have been stored in these column capacitors. Following this process, this row is then brought up for display.

A display control circuit in which the control signals are pulse width modulated is described in GB-A-2 204 174.

The object of the invention is to provide a control circuit for a liquid crystal display which, in a simple manner, keeps the charge voltage constant over a period of time and thereby makes it possible to have a uniform distribution of the brightness over the full width of the display and in which the number of terminal leads is reduced.

This object is achieved by the features indicated in claim 1. Advantageous developments of the invention are specified in the appendant claims.

In order to achieve the object, the control circuit is, in accordance with the invention, operated in multiplex mode. Thereby, prior to or following the connection of the data voltage to a pixel element, the selection line of the relevant row is switched on and thereafter or beforehand, the data voltage is applied to the relevant column. To this end, a number of columns are combined into blocks whereby the video signal for a respective block is applied to the relevant columns of the display element and the video signal is switched onwards in block-like manner. For the multiplex mode, there thereby results a charging time for each pixel element which is equal to the duration of the row divided by the number of blocks. Since the number of blocks is appreciably smaller than the number of columns, the charging time is appreciably greater.

In order to avoid high current peaks as well as to achieve a uniform distribution of the brightness over the full width of the display, the video signal is buffer stored and all the capacitors of the individual columns of a block are charged in parallel.

The embodiment in accordance with the invention will be explained with the help of the drawing.

Fig. 1 the control of the display

Fig. 2 a buffer storage arrangement

Fig. 3 a buffer storage arrangement including a current amplifier

Fig. 4 a block circuit diagram of a time - voltage conversion process

Fig. 5 a circuit for the time - voltage conversion process in accordance with Fig. 4

Fig. 6 a further voltage - time conversion circuit

Fig. 7 a storage circuit

Fig. 8 a first timing diagram

Fig. 9 a second timing diagram

Fig. 10 an expanded preliminary stage

Fig. 11 a third timing diagram

Fig. 12 a timing diagram for Fig. 6

Fig. 1 shows the control process for a liquid crystal display in accordance with the invention. The liquid crystal display is divided into 25 blocks 1 - 25 each having 30 vertical control leads. Here, the video signal for a respective block is transmitted in parallel on the 30 input leads 1 - 30 whereby input clock pulses switch over to the next block after each writing of the columns of a block. For this multiplex mode, there ensues per block or for one pixel, the time of p_{Pixel} = 64 µsec / 25 = 2.5 µsec. A sufficiently great time span for controlling the pixels is realised by virtue of the distribution of the control process for the liquid crystal electrodes in accordance with the invention. One possible method of controlling the pixel electrodes could be effected by directly charging the column capacitors of a block. For this however, a very high peak current is necessary which is something that has to be viewed as disadvantageous overall. In addition to this, the distribution of the brightness over the full width of the liquid crystal display is not uniform since the individual columns of the blocks 1 - 25 receive the items of video information one after the other and the voltage on the pixel capacitor of the columns of the first block has already fallen when the columns of the last block receive the video signal.

Consequently, in accordance with the invention, the video signal is buffer stored and a common charging of all of the capacitors in the individual columns is carried out.

Fig. 2 shows such a buffer storage circuit. The video signal is supplied in a multiplex mode to the block switches 26, 27, 28. The switches are closed blockwise, one after the other, in the multiplex mode. The charging capacitors 32, 33, 34 are successively charged in the closed state of the switches 26, 27, 28. The switches 29, 30, 31 are closed simultaneously after the row has been written i.e. after all of the capacitors 32, 33, 34 have been charged so that the storage capacitors 32, 33, 34 are simultaneously connected to the column capacitors 35, 36, 37. The stored voltages are passed row-by-row to the display by activating the selection line.

Fig. 3 shows a buffer storage circuit including a current amplifier 44. A storage circuit for one column is shown. The storage capacitor 32 is charged via the switch 26. After all of the storage capacitors in the storage circuit have been block wise charged during the line period, the switch 29 is closed. The current amplifier 44 amplifies the discharge current of the charging capacitor 29 and guides it to the column capacitor 35.

Fig. 4 shows a circuit for the voltage / time conversion 51, 52 of the video signal as a current amplifier 44. As an example, assuming a voltage range of 0 to 6 volts for the video signal, the video information, which represents a certain voltage value and is stored in a store 50, is converted into a pulse width modulated signal by a voltage - time converter 51. Thereafter, this pulse width modulated signal is supplied to the pixel capacitors via a time - voltage conversion circuit 52.

Fig. 5 shows a circuit for the time - voltage conversion process. The pulse width modulated signal 60 is supplied to the gate 61 of a transistor 63. A voltage, which decays with a constant slope from a maximum value of e.g. 6 volts to 0 volts,

is present on the source electrode 62 of the transistor 63. Consequently, a capacitor 65 connected to the source electrode is charged by means of this ramp voltage. The parasitic gate / drain capacitors of the transistor switches of the non-activated rows in the same column may be utilised as the capacitor. The output of the capacitor 65 is supplied to a column of the liquid crystal display element. One obtains different length pulses from the voltage / time converter 51 in dependence on the magnitude of the video input voltage so that the relevant voltage can be derived from the capacitor 65.

Fig. 6 shows a circuit for the storage and production of a voltage - time conversion of the video signal. The associated timing diagram is reproduced in Fig. 12. The items of input data are supplied via an input 77 to the source or drain electrode of a transistor 70. The signal is supplied to the gate electrode of the transistor 70 for switching over a block D_{in}. A reference voltage $V_{reframp}$ is applied via an input 78 to the drain or source electrode of a transistor 75 whose gate electrode is connected to a control voltage $V_{refctrl}$ 79 for the reference voltage $V_{reframp}$. The two output electrodes of the transistors 70, 75 are connected together, point A, and lead to a capacitor 72. The second terminal of the capacitor 72 leads in turn to the drain / source electrode of a transistor 71 and also to the gate electrode of a transistor 73 at the point B. The gate electrode of the transistor 71 is connected to the lead used for switching over a block. One electrode of the transistor 73 is connected to earth. The other electrode of the transistor 73 is connected to a second electrode of the transistor 71 as well as to a drain / source electrode of the transistor 74. This common connecting point C leads to an output 76 of the circuit which conveys an output signal to the circuit for the time / voltage conversion process e.g. in accordance with Fig. 4. The transistor 74 is connected at its input electrode to a supply voltage V. This supply V is applied simultaneously to the gate electrode of the transistor 74. The capacitor 72 corresponds to the capacitors

32, 33, 34 of Fig. 2. The capacitor 72 serves for the buffer storage of the video signal.

Both transistors 70, 71 are conductive at the start of the charging time t_{load}. Consequently, an equilibrium voltage, which is only dependent upon the dimensioning of the magnitudes of the two transistors 73, 74 e.g. upon the width of the channel in the FET transistors 73, 74 being used, appears at the point B. This circuit serves as an invertor having rapid on- and off-switching of the transistor 73. To this end, in accordance with the invention, the channel in the transistor 74 is selected to be as small as possible, that of the transistor 73 being selected to be as large as possible. The capacitor 72 is now charged with the data voltage at the point A. Once the capacitor 72 is charged, the two transistors 70, 71 are switched off and the reference voltage $V_{reframp}$ is applied to the point A via the transistor 75.

The voltage at the point B alters as follows:

$$U_B = U_{BO} + U_{ramp} - U_{data}$$

where, in this case, U_{BO} is the voltage which appears when the transistor 71 is conductive i.e. the voltage which occurs due to the dimensioning of the transistors 73, 74. An equilibrium voltage thus occurs. Assuming a reference voltage of 6 volts having a constant decay down to 0 volts and a data voltage V_{data} = 3 volts, the following voltage occurs at the point B:
$U_B = 4V + 6V - 3V = 7V$

Since the capacitor 72 is, in effect, not discharged during the time that now follows, the voltage U_B follows the reference ramp 78 at an interval which is virtually parallel therewith and which is dependent on the magnitude of the initially applied data voltage U_{data}.

If the voltage U_B is smaller than U_{BO}, then the transistor 73 becomes blocked and the voltage at the point C very rapidly becomes larger. This voltage at the point C is inverted with the aid of a not shown invertor and is used for controlling the transistor 63 in accordance with Fig. 5 in the circuit for the time - voltage conversion.

Thus, the pulse width modulation comes about due to the voltage at the point B being dependent on the data voltage and sooner or later blocking the transistor 73. The voltage waveforms A, B, C shown in Fig. 12 correspond to the voltage waveforms at the points A, B, C for the example mentioned above.

Fig. 8 shows the charging and processing process in a row such as is effected in Fig. 6. The 25 blocks 1 - 25 are loaded with the data signal during equal time periods t_{load1}, ..., t_{load25} in the course of the time period for one row of 64 µs. The total loading time is less than the time period for the whole row of 64 µs. Assuming that the processing time amounts to $t_{processing}$ = 20 µs, there results therefrom a charging time for the capacitor 72 of 1.7 µs.

Fig. 7 shows a preliminary stage for the circuit in accordance with Fig. 6. The items of input data are supplied to a transistor 100 whose gate electrode is controlled by a control signal for the purposes of buffer storage, which signal is applied to the gate electrodes en bloc. The voltage representing the items of data is stored on a capacitor 101. This item of information stored as a voltage value is supplied to the input 77 of the circuit in accordance with Fig. 6. All 25 preliminary stage blocks are thereby initially loaded one after the other and the items of data are then transmitted together into the next circuit in accordance with Fig. 6. In accordance with Fig. 11, the processing of the items of data for the rows n + 1 runs simultaneously during the loading process for the preliminary stage of the rows n. The transfer time $t_{transfer}$ in accordance with Fig. 11 corresponds to the time which is available for the

charging of the capacitor 72 in the circuit in accordance with Fig. 6 and corresponds for example, to the time t_{load1} in accordance with Fig. 8. In this preliminary stage, the transistor may be dimensioned to be larger than the transistors 70, 71 so that charging of the capacitor 101 in the preliminary stage can be carried out more quickly than the charging of the capacitor 72 in the circuit in accordance with Fig. 6. The reason for this larger dimensioning being possible, is that the voltage differences, which occur here when the transistor is switched off and which are caused by the parasitic gate - drain and gate - source capacitances, do not produce such large effects upon the rest of the circuit as for the transistors 70 and 71. The charging time for the capacitor 101 of the preliminary stage block amounts to 2.3 µs for a transfer time of e.g. 5 µs.

Fig. 10 shows an expanded preliminary stage circuit for the circuit in accordance with Fig. 6. The video data signals 80 are supplied to a transistor 81 and also to a transistor 87. The respective other electrodes of the transistors 81, 87 are connected on the one hand to the capacitors 83, 88 as well as to the input electrodes of the transistors 82, 84. The outputs of the transistors 82, 84 are led together to the charging capacitor 72 to which the reference voltage $V_{reframp}$ is supplied via the transistor 75 in correspondence with Fig. 6.

By means of this preliminary circuit, a whole row can now be used, in accordance with Fig. 9, for loading the preliminary stages so that there results a charging time t_{load83}, t_{load88} of 2.5 µs for the transistors 83/88. Moreover, this time is completely independent of the transfer time $t_{transfer}$. The control process for the transistor 81 is effected by a block switching process Bu2n every $2n^{th}$ rows, for the transistor 87 by a block switching signal Bu2n+1 every $2n+1^{th}$ row, for the transistor 82 by a row switching signal Z2n+1 every $2n-1^{th}$ row and for the transistor 84 by a row switching signal Z2n every $2n^{th}$ row.

The circuit in accordance with Fig. 6 is comprised in each block 1 - 25 in correspondence with the column count per block. The inputs of the gate electrodes of the transistors 70, 71 are switched in parallel on a block like basis. The control signal 79 is applied during a processing time after writing all of the blocks 1 - 25.

* C L M S *

Claims

1. Control circuit for a liquid crystal display in which pixel elements are controllable, for display purposes, by means of a matrix consisting of columns formed by data lines and rows formed by selection lines, wherein a number of columns is combined into respective blocks (1, 2, ..., 25) and the relevant part of the signal to be displayed is respectively supplied in parallel via switches (26, 27, 28, 70) to the columns of a block and successively to each of the blocks, wherein a capacitor (35, 36, 37, 65) for storing the signal to be displayed is correspondingly charged for each column and, in accordance with the control process of the blocks of a row, the corresponding row for the display is selected via the selection lines, characterised in that, the signal to be displayed is additionally buffer stored in a charging capacitor (32, 33, 34, 72) associated with each of the columns and that, in each case following the charging of the charging capacitors of a row, the column capacitors (35, 36, 37, 65) are charged in parallel via a current amplifier (44).

2. Control circuit in accordance with Claim 1, characterised in that, the signal to be displayed is converted in the current amplifiers (44) into a pulse width modulated signal (60) with which a respective one of the columns is controlled via a time - voltage converter circuit (52; 63, 65).

3. Control circuit in accordance with Claim 2, characterised in that, the pulse width modulated signal (60) is generated with the help of a voltage - time converter (73, 74) in a transistor circuit (70, 71, 73, 74, 75) which receives the input signal that is to be displayed for the data lines at a first input (77) and a ramp shaped reference voltage ($V_{reframp}$) at a second input (78) and in which a respective one of the charging capacitors (32, 33, 34, 72) is disposed and which is activated at a third input (D_{in}) in accordance with the currently selected block.

4. Control circuit in accordance with Claim 3, characterised in that, the signal to be displayed is connected during a charging time (t_{load}) via a first transistor arrangement (70) to a second transistor (75) to which the reference voltage ($V_{reframp}$) is applied, that a first connection point (A) of the first and second transistors (70, 75) leads to the charging capacitor (72), that a second connection point (B) connects the other side of the charging capacitor to an input of a third transistor (71) and to the control electrode of a fourth transistor (73), that a third connection point (C) of the output or input electrodes of the third and fourth transistors is coupled to the output (76) of the transistor circuit and also to the output of a fifth transistor (74) which is connected to a supply voltage (V) at its input and its control electrode.

5. Control circuit in accordance with Claim 4, characterised in that, the first transistor arrangement (70) is a transistor.

6. Control circuit in accordance with Claim 4, characterised in that, the transistors (70, 71, 73, 74, 75) are FET or TFT transistors.

7. Control circuit in accordance with any of the Claims 4 to 6, characterised in that, the channel of the fifth transistor (74) is selected to be as small as possible and that of the fourth transistor (73) to be as large as possible.

8. Control circuit in accordance with any of the Claims 4 to 7, characterised in that, the first and the third transistor (70, 71) are blocked after the charging capacitor (72) has charged up and a reference ramp ($V_{reframp}$) is applied to the first connection point (A) via the second transistor (75).

9. Control circuit in accordance with any of the Claims 4 to 8, characterised in that, the signal to be displayed for each input line is supplied blockwise to a second capacitor (101) via a sixth transistor (100) during a charging time, that the stored

items of data are applied line-by-line to the input of the first transistor (70) following the blockwise charging of each of the second capacitors (101).

10. Control circuit in accordance with Claim 4, characterised in that, the first transistor arrangement (70) consists of a parallel circuit including a first branch which contains a seventh transistor (81), a third capacitor (83) and an eighth transistor (82) and a second branch which contains a ninth transistor (87), a fourth capacitor (88) and a tenth transistor (84).