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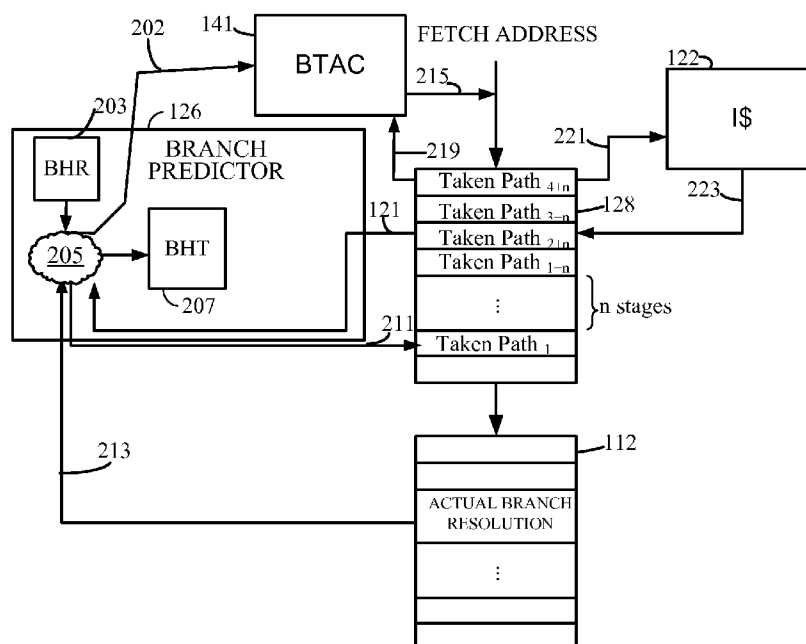
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(54) Title: METHODS AND APPARATUS FOR PROACTIVE BRANCH TARGET ADDRESS CACHE MANAGEMENT



(57) Abstract: A multiple stage branch prediction system including a branch target address cache (BTAC) and a branch predictor circuit is disclosed. The BTAC is configured to store a BTAC entry. The branch predictor circuit is configured to store state information. The branch predictor circuit utilizes the state information to predict the direction of a branch instruction and to manage the BTAC entry based on the stored state information in response to actual resolution of the branch instruction.

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