

ABSTRACT OF THE DISCLOSURE

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

5 A nonvolatile semiconductor memory device according to
an embodiment includes a memory cell array that includes NAND
cell units; and a write/erase circuit configured to execute
a select gate write operation, the select gate write operation
executing a programming operation for setting a threshold
10 voltage of a drain side select gate and a verify operation
for judging whether said threshold voltage has reached a
certain value, and, when it is judged by the verify operation
on the drain side select gate that the threshold voltage of
the drain side select gate has not reached the certain value,
15 repeatedly executing a programming operation for setting a
threshold voltage of a drain side dummy cell connected to the
drain side select gate and a verify operation for judging
whether said threshold voltage has reached a certain value,
until the threshold voltage of the drain side dummy cell has
20 reached the certain value.

Fig. 1



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