PROCESS FOR FABRICATING A STRUCTURE HAVING A BURIED DIELECTRIC LAYER OF UNIFORM THICKNESS

FIELD OF THE INVENTION

The present invention relates to the fabrication of a final structure comprising in succession a useful semiconductor layer, a dielectric layer and a carrier substrate. These structures are especially applicable in the fields of microelectronics, micromechanics, photonics, etc.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

Various processes allowing an intermediate structure comprising in succession an upper semiconductor layer, a dielectric layer, and a carrier substrate to be formed are known from the prior art. It may for example be a question of layer-transfer fabrication processes (such as the processes known by the names Smart Cut™ or Eltran™) or even of the oxygen-implantation fabrication process (and known by the acronym SIMOX: Separation by Implantation of Oxygen).

This intermediate structure, during a following finishing step, undergoes various treatments in order to convert the upper layer into a useful layer having all the expected properties especially in terms of average thickness, thickness uniformity, roughness, crystal quality, etc.

These known processes are especially employed for the fabrication of silicon-on-insulator substrates. In this case, the upper layer, the useful layer and the carrier

typically consist of silicon and the dielectric layer of silicon dioxide.

These silicon-on-insulator substrates must satisfy very precise specifications. This is especially the case for the average thickness and the thickness uniformity of the dielectric layer. Satisfaction of these specifications is required for the good operation of the semiconductor devices that will be formed in and on the useful layer.

In certain cases, the architecture of the semiconductor devices requires a silicon-on-insulator substrate having a dielectric layer of very insubstantial average thickness to be provided. Thus, the dielectric layer may be specified to have an average thickness smaller than or equal to 50 nm and typically comprised between 10 and 25 nm. It is particularly important in the case of insubstantial average thickness to control with precision the thickness of the dielectric layer at every point.

Among the conventional finishing treatments applied to an intermediate structure, smoothing anneal treatments, consisting in exposing the upper layer or useful layer to a neutral or reducing atmosphere raised to a high temperature, typically higher than 1100°C, are known. This treatment, *inter-alia*, allows, by surface reconstruction, the roughness of the layer exposed to the high-temperature atmosphere to be decreased.

However, this treatment is liable, via an oxide dissolution effect, to modify the properties of the subjacent dielectric layer, such as its thickness. This phenomenon is especially reported in the document "Novel trends in SOI Technology for CMOS applications" by O. Kononchuck *et al.* published in the review Solid State

Phenomena, volume 156 - 158 (2010) p 69 to 76. Specifically, this document explains that in the high-temperature reducing or neutral treatment atmospheres oxygen atoms of the dielectric layer are liable to diffuse through the upper layer and to react with the surface thereof to produce volatile species that are evacuated by the atmosphere of the furnace. This document also explains that for SOI substrates having a thin upper layer, the phenomenon of diffusion is limited by the capacity of evacuation of volatile species from the surface of the substrate, and therefore that the magnitude of the dissolution phenomenon is locally related to the gas speed of the atmosphere of the furnace in proximity to the surface.

As a result thereof, generally, at the end of this treatment, the substrate has a dielectric layer with a severely degraded thickness uniformity. Thus, Figure 1a shows an intermediate structure 1 obtained according to a prior-art process described by way of introduction. It will be noted that this structure has a dielectric layer 2 of uniform thickness positioned between an upper semiconductor layer 3 and a carrier 4.

Figure 1b for its part shows a final structure 5 after application of a smoothing anneal treatment similar to that presented in the document introduced above. In this particular example, the dissolution of the dielectric layer 2 through the upper layer 3 is nonuniform and it is more substantial on the periphery of the substrate than at its centre. This leads to the formation of a final structure 5 having a nonuniform dielectric layer 2', under the useful layer 3'.

Researched solutions to this problem aim to modify the parameters of the anneal or the configuration of the annealing equipment in order to limit the magnitude thereof. These solutions are generally imperfect or require expensive investments in particular pieces of equipment.

SUBJECT OF THE INVENTION

One aim of the invention is therefore to provide a process for fabricating a structure comprising a useful semiconductor layer, a dielectric layer and a carrier substrate, the dielectric layer having a well-controlled thickness uniformity and the process not having the aforementioned drawbacks.

BRIEF DESCRIPTION OF THE INVENTION

The present invention relates, in its most general acceptance, to a process for fabricating a final structure comprising in succession a useful semiconductor layer, a dielectric layer and a carrier substrate, the process comprising:

- a step of providing an intermediate structure including an upper semiconductor layer, the dielectric layer and the carrier substrate; and
- a step of finishing the intermediate structure to form the final structure, comprising a treatment modifying nonuniformly the thickness of the dielectric layer following a determined dissolution profile.

According to the invention, the dielectric layer of the intermediate structure has a thickness profile complementary to the determined dissolution profile.

Contrary to the solutions of the prior art, it is not sought to improve the uniformity of the dissolution phenomenon that acts during the finishing step; but this phenomenon is compensated for by providing a nonuniform dielectric layer in the intermediate structure, of complementary profile to the dissolution profile. This process thus allows the thickness uniformity of the dielectric layer to be controlled without making modifications to the equipment used to fabricate the structures.

According to other advantageous and nonlimiting features of the invention, taken individually or in any combination thereof:

- the useful layer is made of silicon and the dielectric layer is made of silicon oxide.

- the carrier substrate is a silicon substrate.
- The useful layer has an average thickness smaller than 100 nm and the dielectric layer of the final structure has an average thickness smaller than or equal to 50 nm.

- The dielectric layer has an average thickness comprised between 5 and 50 nm and preferably between 10 and 25 nm.

- The thickness uniformity of the dielectric layer of the final structure is lower than 3%.

- The intermediate and final structures take the form of circular wafers of 300 mm diameter or more.

- the step of providing the intermediate structure comprises:
  - forming a dielectric layer on a donor substrate;
  - forming a weak plane in the donor substrate defining with a main surface of the donor substrate a layer to be removed;
  - assembling the main face of the donor substrate with the carrier substrate; and
  - detaching the layer to be removed from the donor substrate in order to add it to the carrier substrate.

- the weak plane is produced by implanting light species or by porosification of a surface of a starting substrate and by epitaxial deposition of the upper layer on the starting substrate.

- the process includes a finishing step which comprises thinning the upper layer by sacrificial oxidation in order to form the useful layer.

- the finishing step comprises a treatment by stabilization anneal of the intermediate structure or the final structure.

- the treatment modifying the thickness of the dielectric layer comprises exposing the useful layer or the upper layer to a neutral or reducing atmosphere at a temperature comprised between 1150 and 1200°C.

- the exposure to the neutral or reducing atmosphere is carried out for a length of time comprised between 5 minutes and 5 hours.

- the thickness profile of the dielectric layer of the intermediate structure and the dissolution profile have a circular symmetry of axis perpendicular to the plane of the structure and passing through its centre.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood in light of the following description of one particular nonlimiting embodiment of the invention given with reference to the appended figures, in which:

- Figure 1 shows an intermediate and final structure obtained according to a prior-art process;

- Figure 2 shows the steps of the process of one particular embodiment of the present invention; and

- Figure 3 shows an exemplary dissolution profile.

DETAILED DESCRIPTION OF THE INVENTION

The process according to the invention is generally applicable to the fabrication of a final structure comprising a useful semiconductor layer, a dielectric layer and a carrier substrate.

With reference to Figure 2a, the process comprises providing an intermediate structure 1 comprising in succession an upper semiconductor layer 3, a dielectric layer 2, and a carrier substrate 4. This intermediate

structure 1 is treated in a following finishing step so as to form the useful layer 3′ having the required properties (thickness, thickness uniformity of the various layers, crystal quality) from the upper layer 3.

The finishing step may thus comprise one treatment or a plurality of treatments chosen for example from the following treatments: a sacrificial oxidation, a heat treatment under neutral or reducing atmosphere, dry or wet etching, chemical-mechanical polishing, etc.

Furthermore, according to the invention, the step of finishing the intermediate structure comprises at least one treatment modifying nonuniformly the thickness of the dielectric layer 2 of the intermediate structure 1. This step is shown in Figure 2b.

For the record, it will be recalled that the nonuniformity of a layer may be measured by the difference between its maximum thickness and its minimum thickness divided by its average thickness. In the present invention, a layer will be considered to be nonuniform when its measurement exceeds 3%. The thickness of the dielectric layer 3, 3′ may be measured by techniques such as ellipsometry or reflectometry.

By way of example, the treatment modifying nonuniformly the thickness of the dielectric layer 2 may correspond to a smoothing anneal, in a batch anneal furnace, consisting in exposing the upper layer 3 to a neutral or reducing atmosphere having a temperature above 1100°C, and more precisely comprised between 1150 and 1200°C, in order to improve the smoothing effect of the anneal. This exposure to neutral or reducing atmosphere is

carried out at the plateau value for a length of time that may be comprised between 5 minutes and five hours.

The preceding treatment may alternatively or in addition be applied to the useful layer 3′ of the final structure 5, i.e. at the end of the finishing step or after the latter, when the intermediate structure 1 has already received one or more of the aforementioned treatments.

As was seen in the introduction and as is documented in the cited document, this type of smoothing anneal modifies nonuniformly the thickness of the dielectric layer 2 that is located under the upper layer 3 treated. Furthermore, determined treatment conditions lead the thickness of the dielectric layer 2 of the intermediate structure 1 to be modified nonuniformly following a determined dissolution profile.

This determined dissolution profile corresponds to the difference between the thickness profile of the dielectric layer 2′ (of the final structure 5) after the treatment and the thickness profile of the dielectric layer 2 before this treatment (of the intermediate structure 1).

The determined dissolution profile may be represented by a set of measurement points (x, y, e); x and y allowing a point on the surface of the substrate to be located and e indicating the thickness variation of the dielectric layer at this point. Alternatively, the measurement point may be located by its polar coordinates, especially in the case of a substrate of circular shape.

The set of measurement points has a chosen cardinal direction that, in combination with the positions of these points, allows the dissolution profile to be represented

with sufficient precision. Such a profile is shown graphically by way of example in Figure 3.

For a substrate taking the form of a circular wafer of 300 mm diameter, 41 measurement points distributed uniformly over the surface of the wafer may be sufficient.

When the treatment is carried out in a batch anneal furnace, the geometrical configuration of this furnace leads to a dissolution profile generally having a circular symmetry of axis perpendicular to the plane of the substrate and passing through its centre. This is especially the case when the substrate is also driven to rotate during the treatment. In this case, the profile may be represented by a parametric functional form relating the variation in the thickness of the dielectric layer to each point of the structure, for example taking the form $D(r) = k.r^2$ or the form $D(r) = k.|r|$, where r represents the distance from the point to the centre of the structure and k is a parameter of the function.

The determined dissolution profile is representative of the finishing sequence applied to the intermediate structure 1 and more particularly is representative of the treatment affecting the thickness of the dielectric layer 2.

This profile may be obtained in a step prior to the process of the invention. This prior step may consist in applying, to a similar structure to the intermediate structure 1 or final structure 5 of the invention, the envisaged treatment or finishing sequence. The measurement of the thickness profiles of the dielectric layer 2, 2' before and after the application of this sequence or this treatment allows all of the measurement points or the

parameters of the parametric function specifying the determined dissolution profile to be established.

Alternatively, the profile may be obtained by calculation or simulation from parameters (for example: duration, temperature, uniformity) of the treatment.

So as to compensate for the thickness nonuniformity of the dielectric layer liable to be created by the treatment of the finishing step, the invention makes provision for the intermediate structure 1 to have a dielectric layer 2 the thickness profile of which is complementary to the determined dissolution profile.

By complementary thickness profile, what is meant is a thickness profile that, combined with the determined dissolution profile, leads to a profile having a lesser nonuniformity than that of the dissolution profile itself. Practically, the complementary thickness profile of the dielectric layer 2 may be obtained by subtracting the determined dissolution profile from the uniform thickness profile desired for the final structure 5.

Thus, after the treatment and/or the finishing sequence, a final structure 5 made up of a useful layer 3', the dielectric layer 2' and the carrier 4 is obtained. The dielectric layer 2' has a smaller thickness nonuniformity than that of the dissolution profile.

The intermediate structure 1 may be produced using various techniques and especially by layer transfer or using the SIMOX technology. In any case, the formation parameters of the dielectric layer 2 will be adjusted so that its profile is indeed complementary to the determined dissolution profile.

In one particular example, the intermediate structure 1 is thus produced by oxidation of a donor semiconductor substrate, to form the dielectric layer 2, then by transferring to the carrier substrate a layer removed from the donor substrate, this layer comprising the upper layer 3 and the dielectric layer 2. Alternatively, or in addition, the dielectric layer 2 may be formed on the carrier substrate 4.

The upper layer 3 may be transferred by forming a weak plane in the donor substrate thus defining with a surface of this substrate the layer to be removed. The donor substrate is then assembled with the main face of the carrier. The layer to be removed is lastly detached from the donor substrate level with the weak plane in order to thus transfer it to the carrier substrate 4.

As is well known *per se*, the weak plane may be formed by implantation of a light species, or by porosification of a surface of a starting substrate and epitaxial deposition of the layer to be removed on this porosified starting substrate.

Whatever the technique deployed to provide the intermediate structure 1, at the end of this step a structure including an upper layer 3, an oxide layer 2, and a carrier substrate 4 is obtained.

Advantageously, the upper layer 3 is made of silicon and the dielectric layer 2 of silicon oxide. The carrier substrate 4 may also be made of silicon. The structure is then a conventional silicon-on-insulator structure.

The silicon oxide layer may be produced by exposing the donor substrate in a furnace, to a (dry or moist) oxygen-rich atmosphere. This substrate may be placed, during this step, on a carrier that is driven to rotate around an axis perpendicular to its main plane and passing through its centre, thereby leading an oxide layer to be formed the profile of which has a radial symmetry. As is known *per se*, control of the parameters of the furnace allows an oxide layer to be formed the thickness profile of which is chosen. In this regard, the reader may refer to documents FR2843487 or US2009246371 which illustrate such methods.

The structure 1 may take the form of a circular wafer having a diameter of 200, 300 mm or more.

The invention is particularly useful for the formation of final structures 5 in which the dielectric layer 2′ is relatively thin, for example having an average thickness smaller than or equal to 50 nm, such as comprised between 5 and 50 nm, or even comprised between 10 and 25 nm. It allows a dielectric layer 2′ to be obtained, in the final structure 5, that has a nonuniformity lower than 3%.

The invention is also advantageous when the useful layer 3′ of the final structure 5 has an average thickness smaller than 100 nm, the processes for obtaining such structures being particularly sensitive to dissolution phenomena, and leading to a dielectric layer 2′ with a degraded uniformity.

Finally, it is possible for the treatment modifying nonuniformly the thickness of the dielectric layer 2 to also be liable to affect the thickness uniformity of the useful layer 3′. This phenomenon, when its effect is

noticeable, may be compensated for by adjusting the parameters of the various treatments composing the finishing step (sacrificial oxidation, etching, thinning, etc.) so as to obtain a sufficiently uniform useful layer 3' in the final structure 5.

By way of example, a silicon oxide dielectric layer is formed on a first donor substrate consisting of a circular bulk silicon wafer of 300 mm diameter. This layer is formed by exposing the wafer to a heat treatment in a furnace, the atmosphere of the furnace being rich in oxygen.

The oxidation heat treatment comprises a first plateau at 750°C, followed by a plateau at 770°C, then a temperature ramp to reach a plateau of 800°C, and lastly a ramp decreasing to 750°C.

This treatment leads a silicon dioxide layer having an average thickness of **27 nm** and a symmetric and concave profile to be formed, the thickness at the periphery of the wafer having a thickness larger by 0.4 nm than the thickness at its centre.

By way of comparison, a dielectric layer made of silicon dioxide of essentially uniform average thickness identical to 27 nm (i.e. not having a symmetric and concave profile) is formed on a second donor substrate that is identical to the first.

Next, in these two silicon wafers, each equipped with their dielectric layer made of silicon dioxide, a weak plane is formed by implantation of light species, such as hydrogen and/or helium, as is well known *per se*.

These silicon wafers are then each assembled with a carrier substrate, also formed from a circular bulk silicon wafer of 300 mm diameter. The wafers are assembled, in the particular case of this example, by bringing the silicon dioxide surface of the donor substrates into direct contact with the silicon surfaces of the carrier substrates, according to the direct bonding technique.

These assemblies are then treated in order to fracture the donor substrates level with the weak planes, for example during a weakening anneal having a temperature comprised between 300°C and 500°C. The fracture itself may be obtained during this anneal or by applying additional exterior forces.

In the particular context of the example, what is obtained is, on the one hand, residual silicon donor substrates, and on the other hand, the intermediate structures each comprising:

- a 265 nm-thick upper layer made of silicon;
- the silicon oxide dielectric layer having an average thickness of 27 nm (in one case with an extra thickness of 0.4 nm on the periphery, in the other case with a substantially uniform thickness); and
- the carrier substrate.

These intermediate structures are then treated by a succession of finishing steps, which are identical for each of the two structures, allowing the final silicon-on-insulator structures having all the desired properties to be formed.

In this particular example, firstly a stabilizing treatment is carried out, this treatment comprising a first

step of oxidation of the exposed surfaces of the upper layers, followed by an annealing step at 950°C allowing certain defects in the upper layers to be healed. After this heat treatment, the oxidized portion of the upper layers is removed, for example by chemical etching in a bath comprising HF. This treatment is therefore a first step of thinning the upper layers.

Next, a smoothing treatment is applied to the exposed surface of the upper layers of the intermediate structures. This is achieved by exposing these layers to a hydrogen atmosphere at 1170°C during a plateau of 5 minutes. This smoothing treatment affects, by dissolution, the uniformity of the buried silicon dioxide layers.

Lastly, a second step of thinning the upper layers, by simple sacrificial oxidation, is carried out to form the useful layers having a desired thickness, in this example of 15 nm. The oxidation of the upper layers may be carried out at about 900 or 950°C, for a sufficient length of time that at the end of this treatment the useful layers have the desired thickness.

After these treatments, it is observed that the first final structure (obtained from the first donor substrate on which a nonuniform dielectric layer was formed) has an average thickness of 25 nm and a variation in thickness of the dielectric layer made of silicon dioxide of 0.7 nm, i.e. a variation of 2.8%.

The second final structure (obtained from the second donor substrate on which a uniform dielectric layer was formed) has an average thickness of 25 nm and a variation in thickness of the dielectric layer made of silicon dioxide of 1.2 nm of 4.8%.

It will therefore clearly be understood from this example the advantage of providing a dielectric layer in the intermediate structure having a thickness profile complementary to the dissolution profile of the finishing sequence.

CLAIMS

1. Process for fabricating a final structure (5) comprising in succession a useful semiconductor layer (3′), a dielectric layer (2′) and a carrier substrate (4), the process comprising:

   - A step of providing an intermediate structure (1) including an upper semiconductor layer (3), the dielectric layer (2) and the carrier substrate (4); and
   - a step of finishing the intermediate structure to form the final structure (5), comprising a treatment modifying nonuniformly the thickness of the dielectric layer (2) following a determined dissolution profile;

   The process being characterized in that the dielectric layer (2) of the intermediate structure (1) has a thickness profile complementary to the determined dissolution profile.

2. Process according to Claim 1, in which the useful layer (3′) is made of silicon and in which the dielectric layer (2, 2′) is made of silicon oxide.

3. Process according to Claim 1 or 2, in which the carrier substrate (4) is a silicon substrate.

4. Process according to one of the preceding claims, in which the dielectric layer (2′) of the final structure has an average thickness smaller than or equal to 50 nm.

5. Process according to one of the preceding claims, in which the step of providing the intermediate structure (1) comprises:

- forming a dielectric layer (2) on a donor substrate;
- forming a weak plane in the donor substrate defining with a main surface of the donor substrate a layer to be removed;
- assembling the main face of the donor substrate with the carrier substrate (4); and
- detaching the layer to be removed from the donor substrate in order to add it to the carrier substrate (4).

6. Process according to one of the preceding claims, in which the finishing step comprises thinning the upper layer (3) by sacrificial oxidation in order to form the useful layer (3').

7. Process according to one of the preceding claims, in which the finishing step comprises a treatment by stabilization anneal of the intermediate structure (1).

8. Process according to one of the preceding claims, in which the treatment modifying the thickness of the dielectric layer (2) comprises exposing the useful layer (3') or the upper layer (3) to a neutral or reducing atmosphere at a temperature comprised between 1150 and 1200°C.

9. Process according to the preceding claim, in which the exposure to the neutral or reducing atmosphere is

carried out for a length of time comprised between 5 minutes and 5 hours.

10. Process according to one of the preceding claims, in which the thickness profile of the dielectric layer (2) of the intermediate structure (1) and the dissolution profile have a circular symmetry of axis perpendicular to the plane of the structure and passing through its centre.