CLAIMS

1. A method comprising:

forming a plurality of first interconnects and a plurality of second interconnects on opposite sides of an integrated circuit device layer comprising a plurality of circuit devices, wherein forming ones of the plurality of first interconnects and a plurality of second interconnects comprises embedding memory devices therein; and

coupling ones of the memory devices to each of respective ones of the plurality of first interconnects and the plurality of second interconnects and to ones of the plurality of circuit devices.

2. The method of claim 1, wherein forming a plurality of first interconnects comprises forming the plurality of first interconnects on an integrated circuit device layer of a first substrate and the method further comprises:

coupling the first substrate to a second substrate wherein the plurality of first interconnects are juxtaposed to the second substrate;

removing a portion of the first substrate to expose the circuit device layer;

forming memory devices on the exposed circuit device layer; and

forming the plurality of second interconnects on the exposed circuit device layer.

3. The method of claim 2, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

4. The method of claim 3, further comprising forming contact points to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

5. The method of any of claims 1-2, wherein forming a plurality of first interconnects comprises forming the plurality of first interconnects on an integrated circuit device layer of a first substrate and, prior to forming at least a portion of the plurality of first interconnects, the method further comprises forming the plurality of circuit devices and forming memory devices, wherein ones of the memory devices are coupled to respective ones of the plurality of circuit devices.

6. The method of claim 5, further comprising after forming the plurality of first interconnects, the method further comprises:

coupling the first substrate to a second substrate wherein the plurality of first interconnects are juxtaposed to the second substrate;

removing a portion of the first substrate to expose the circuit device layer; and

forming the plurality of second interconnects on the exposed circuit device layer.

7. The method of any of claims 1-2, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

8. The method of claim 6, further comprising forming contacts to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

9. The method of any of claims 1-2, wherein the memory devices comprise magnetoresistive random access memory devices.

10. A three-dimensional integrated circuit made by any of the methods of claims 1-9.

11. An apparatus comprising:

a substrate comprising a plurality of first interconnects and a plurality of second interconnects on opposite sides of an integrated circuit device layer comprising a plurality of circuit devices, wherein ones of the plurality of first interconnects and a plurality of second interconnects comprises memory devices embedded therein and ones of the memory devices are coupled to each of respective ones of the plurality of first interconnects and the plurality of second interconnects and to ones of the plurality of circuit devices.

12. The apparatus of claim 11, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

13. The apparatus of any of claims 11-12, further comprising contact points to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

14. The apparatus of any of claims 11-13, wherein the memory devices comprise

magnetoresistive random access memory devices.

15. The apparatus of claim 12, wherein the memory devices are embedded in ones of the plurality of second interconnects.

16. The apparatus of claim 12, wherein the memory devices are embedded in ones of the plurality of first interconnects.

17. A method comprising:

forming a plurality of first interconnects on an integrated circuit device layer on a first substrate;

coupling the first substrate to a second substrate wherein the plurality of first interconnects are juxtaposed to the second substrate;

removing a portion of the first substrate to expose the circuit device layer;

forming a plurality of second interconnects on the exposed circuit device layer;

embedding memory devices in one of the plurality of first interconnects and the plurality of second interconnects; and

coupling ones of the memory devices to each of respective ones of the plurality of first interconnects and the plurality of second interconnects and to ones of the plurality of circuit devices.

18. The method of claim 17, wherein the memory devices are embedded in the plurality of first interconnects.

19. The method of any of claims 17-18, wherein the memory devices are embedding the plurality of second interconnects.

20. The method of any of claims 17-19, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

21. The method of claim 19, further comprising forming contact points to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

22. A three-dimensional integrated circuit made by any of the methods of claims 17-21.

CLAIMS

1. A method comprising:

forming a plurality of first interconnects and a plurality of second interconnects on opposite sides of an integrated circuit device layer comprising a plurality of circuit devices, wherein forming ones of the plurality of first interconnects and a plurality of second interconnects comprises embedding memory devices therein; and

coupling ones of the memory devices to each of respective ones of the plurality of first interconnects and the plurality of second interconnects and to ones of the plurality of circuit devices.

2. The method of claim 1, wherein forming a plurality of first interconnects comprises forming the plurality of first interconnects on an integrated circuit device layer of a first substrate and the method further comprises:

coupling the first substrate to a second substrate wherein the plurality of first interconnects are juxtaposed to the second substrate;

removing a portion of the first substrate to expose the circuit device layer;

forming memory devices on the exposed circuit device layer; and

forming the plurality of second interconnects on the exposed circuit device layer.

3. The method of claim 2, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

4. The method of claim 3, further comprising forming contact points to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

5. The method of claim 1, wherein forming a plurality of first interconnects comprises forming the plurality of first interconnects on an integrated circuit device layer of a first substrate and, prior to forming at least a portion of the plurality of first interconnects, the method further comprises forming the plurality of circuit devices and forming memory devices, wherein ones of the memory devices are coupled to respective ones of the plurality of circuit devices.

6. The method of claim 5, further comprising after forming the plurality of first interconnects, the method further comprises:

coupling the first substrate to a second substrate wherein the plurality of first interconnects are juxtaposed to the second substrate;

removing a portion of the first substrate to expose the circuit device layer; and

forming the plurality of second interconnects on the exposed circuit device layer.

7. The method of claim 1, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

8. The method of claim 6, further comprising forming contacts to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

9. The method of claim 1, wherein the memory devices comprise magnetoresistive random access memory devices.

10. An apparatus comprising:

a substrate comprising a plurality of first interconnects and a plurality of second interconnects on opposite sides of an integrated circuit device layer comprising a plurality of circuit devices, wherein ones of the plurality of first interconnects and a plurality of second interconnects comprises memory devices embedded therein and ones of the memory devices are coupled to each of respective ones of the plurality of first interconnects and the plurality of second interconnects and to ones of the plurality of circuit devices.

11. The apparatus of claim 10, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

12. The apparatus of claim 11, further comprising contact points to ones of the plurality of second interconnects, the contact points operable for connection to an external source.

13. The apparatus of claim 10, wherein the memory devices comprise magnetoresistive

random access memory devices.

14. The apparatus of claim 11, wherein the memory devices are embedded in ones of the plurality of second interconnects.

15. The apparatus of claim 11, wherein the memory devices are embedded in ones of the plurality of first interconnects.

16. A method comprising:

forming a plurality of first interconnects on an integrated circuit device layer on a first substrate;

coupling the first substrate to a second substrate wherein the plurality of first interconnects are juxtaposed to the second substrate;

removing a portion of the first substrate to expose the circuit device layer;

forming a plurality of second interconnects on the exposed circuit device layer;

embedding memory devices in one of the plurality of first interconnects and the plurality of second interconnects; and

coupling ones of the memory devices to each of respective ones of the plurality of first interconnects and the plurality of second interconnects and to ones of the plurality of circuit devices.

17. The method of claim 16, wherein the memory devices are embedded in the plurality of first interconnects.

18. The method of claim 16, wherein the memory devices are embedding the plurality of second interconnects.

19. The method of claim 17, wherein dimensions of ones of the plurality of second interconnects are larger than dimensions of ones of the plurality of first interconnects.

20. The method of claim 19, further comprising forming contact points to ones of the plurality of second interconnects, the contact points operable for connection to an external source.