BOARD-ON-CHIP PIN-GRID ARRAY SEMICONDUCTOR PACKAGE AND METHOD OF CONSTRUCTION

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of electronic devices, and more particularly to a pin-grid array semiconductor package and method of construction.

BACKGROUND OF THE INVENTION

Electronic devices such as televisions, telephones, radios, and computers are often constructed using semiconductor components, such as integrated circuits, memory chips, and the like. The semiconductor components are generally incorporated into a circuit board. The circuit board provides a stable surface for assembly of each of the various semiconductor components. The circuit board includes conductive regions that allow the semiconductor components to communicate with each other and with the other electronic components that form the electronic device.

In many applications, the circuit board includes receiving sockets designed to receive respective semiconductor components. This allows for semiconductor components to be fabricated separately from the circuit board, and subsequently plugged into the receiving sockets of the circuit board. Fabricating the circuit board separately from the semiconductor component allows the semiconductor component and the circuit board to be tested independently, thereby reducing the rejection rate if either the board or the semiconductor component fails. Testing the semiconductor components individually and separately from the circuit board makes it much easier to pinpoint a faulty semiconductor component or circuit board than by testing a semiconductor components which are pre-fabricated into a circuit board. Separate fabrication of the individual semiconductor components also allows semiconductor components to be removed or exchanged, such as to incorporate upgraded semiconductor components on the circuit board, without altering the circuit board itself.

Packaging of the semiconductor component has increased in complexity and importance in the industry.

Semiconductor components, such as integrated circuit chips, are often packaged in the form of leadless chip carriers, letter chip carriers, flat packs, outline ICs for service mounting, and pin-grid arrays for through-hole mounting to the circuit board. The pin-grid array semiconductor package generally incorporates the terminals, or pins, into one surface of the package. These pins allow electrical communication between the integrated circuit contained in the pin-grid array semiconductor package and the circuit board. Depending upon the application, the pins may be inserted into sockets in the circuit board or may be inserted through holes in the circuit board and soldered into place.

In many applications, the area on the circuit board is at a premium, requiring the need to minimize the size of pin-grid array semiconductor packages. In addition, semiconductor components have become more complex and powerful and often require a greater number of input-output terminals for communication. In many applications, the size of the pin-grid array semiconductor package is proportional to the number of communication terminals, or pins, within the package. Furthermore, the increased complexity and capability of the semiconductor components has increased the need for additional space on the integrated circuit chip. For example, the processing speed of an integrated circuit chip can often be increased by increasing the resident chip memory of the chip, which often requires additional space on the chip.

SUMMARY OF THE INVENTION

Accordingly, a need has arisen for an improved semiconductor package. The present invention provides a pin-grid array semiconductor package that substantially eliminates or reduces problems associated with prior methods and systems.

In accordance with one embodiment of the present invention, a pin-grid array semiconductor package is

provided. The pin-grid array semiconductor package comprises a housing that has a first surface and a second surface. A semiconductor die comprising a number of conductive wires is located within the housing. Each conductive wire is coupled to a lateral conductor contained within the housing. Each lateral conductor is coupled to a pin. Each pin has a first end and a second end. The first end of each pin protrudes beyond the first surface of the housing. The second end of each pin forms a receptacle on the second surface of the housing. In a particular embodiment, a second pin-grid array semiconductor package is coupled to the pin-grid array semiconductor package to form a three-dimensional semiconductor stack.

The present invention provides several important technical advantages. For example, the present invention eliminates the need for a lead frame and substantially reduces the size of the semiconductor package. The present invention provides a semiconductor package having an increased density of terminals, or pins, allowing an increased number of terminals per semiconductor package and smaller semiconductor packages. In particular, the present invention allows for a true chip size package to be formed. In addition, the present invention allows for high-speed packaging processes to be utilized. Accordingly, the production rate of semiconductor packages may be increased.

Another technical advantage of the present invention is that the lateral conductors provide an improved method of connecting the conductive wires to the pins, when compared to some conventional methods. Accordingly, interconnection defects and shorts are reduced, which reduces the overall cost of production. In addition, the pins provide a reliable and removable connection to the circuit board.

Yet another technical advantage of the present invention is that the pin-grid array semiconductor

package may incorporate pins that have receptacles that allow interconnection with other semiconductor packages to form a three-dimensional semiconductor stack. The three-dimensional semiconductor stack allows an increased number of semiconductor components to be mounted on a particular circuit board. The three-dimensional semiconductor stack may also increase the computing power, speed, efficiency, and memory of an electronic device.

Other technical advantages will be readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like referenced numerals represent like parts, in which:

FIGURE 1 is an exploded view of a circuit board assembly constructed in accordance with the present invention;

FIGURE 2 is a cross-sectional view of a pin-grid array semiconductor package constructed in accordance with the present invention; and

FIGURE 3 is an exploded cross-sectional view with portions broken away of a three-dimensional semiconductor stack constructed in accordance with the present invention.

INVENTION DETAILED DESCRIPTION OF THE

FIGURES 1-3 illustrate various embodiments of a pin grid array semiconductor package. As described in more detail below, the pin-grid array semiconductor package utilizes a stair-step, or multilevel, construction in conjunction with lateral conductors to increase the number of terminals and to improve the manufacturability of the pin-grid array semiconductor

package. The pin-grid array semiconductor package may also include a pin-grid array that allows connection to both a circuit board and other array semiconductor packages to form a three-dimensional pin-grid array semiconductor package stack.

FIGURE 1 is an exploded view of a circuit board assembly 10 comprising a circuit board 11, a receiving socket 12, and a pin-grid array semiconductor package 14. The receiving socket 12 is soldered or otherwise suitably connected to the circuit board 11. The pin-grid array semiconductor package 14 comprises a number of pins 16 that are arranged in rows and columns that form a pin grid array 18. The pin grid array 18 corresponds to a matching set of receiver holes in the receiving socket 12. The receiving socket 12 provides an interconnection between the pin-grid array semiconductor package 14 and the circuit board 11 such that the pin-grid array semiconductor package 14 may be removed from the receiving socket 12 and replaced with relative ease.

The pin-grid array semiconductor package 14 may be otherwise suitably attached to the circuit board 11 via the pins 16 without departing from the scope of the present invention. For example, the pins 16 may be directly soldered to the circuit board 11.

The pins 16 comprising the pin-grid array 18 may be arranged in any number of configurations. For example, the pin-grid array 18 may be arranged in a single row of pins 16 extending along the perimeter of two sides of the pin-grid array semiconductor package 14. In another configuration, the pin-grid array 18 may comprise rows and columns of the pins 16 on all four sides of the pin-grid array semiconductor package 14 as illustrated in FIGURE 1. The pin-grid array 18 may be otherwise configured without departing from the scope of the present invention.

FIGURE 2 illustrates a cross-section of the pin-grid array semiconductor package 14 constructed in

accordance with one embodiment of the present invention. The pin-grid array semiconductor package 14 comprises a housing 20 having a first surface 22 and a second surface 24. The pins 16 comprising the pin grid array 18 protrude beyond the first surface 22 of the housing 20. In one embodiment, as illustrated in FIGURE 2, the housing 20 comprises a recess 26 formed in the second surface 24 of the housing 20. It will be understood that the recess 26 may alternatively be formed within the first surface 22 of the housing 20 without departing from the scope of the present invention. As will be discussed in greater detail below, the recess 26 is sized to receive a semiconductor die.

The housing 20 also comprises a stair-stepped cutout 28 between the recess 26 and the surface opposite the recess 26. In the embodiment illustrated in FIGURE 2, the stair-stepped cutout 28 is disposed between the recess 26 and the first surface 22 of the housing 20. The stair-stepped cutout 28 comprises at least one stair 30. Each stair 30 comprises a number of lateral conductors 32 extending generally parallel to the first and second surface 22 and 24 of the housing 20. Each lateral conductor 32 is electrically insulated from the other lateral conductors 32 to prevent shorting. The lateral conductors 32 may be formed in a film of lateral conductors 41 that comprises conductive and insulative regions, in which the conductive regions form the lateral conductors 32 and the insulative regions electrically insulate the lateral conductors 32 from each other. It will be understood that the lateral conductors 32 may be fabricated by any suitable method without departing from the scope of the present invention.

Each lateral conductor 32 is coupled to an individual pin 16 that extends through the housing 20. The lateral conductors 32 corresponding to a single stair 30 are generally attached to a single row of pins

16. For example, as illustrated in FIGURE 2, the stair-stepped cutout 28 comprises three individual stairs 30, each stair 30 corresponding to one set lateral conductors 32, and each set of lateral conductors 32 coupled to one rows of pins 16. It will be understood that the lateral conductors 32 corresponding with each stair 30 may be otherwise suitably configured without departing from the scope of the present invention.

In one embodiment, the housing 20 is fabricated from a number of sheets 40 that are stacked together and bonded to form the housing 20. In this embodiment, the film of lateral conductors 41 is placed between the sheets 40 to build the required pin-grid array semiconductor package 14. The sheets 40 are fabricated from an electrically non-conducting material. In one embodiment, the sheets 40 are fabricated from FR-4, a commercially available circuit board material. It will be understood that the housing 20 may be otherwise fabricated without departing from the scope of the present invention.

In the embodiment illustrated in FIGURE 2, a first sheet 42 and a second sheet 44 are bonded together to form a baseboard 46. The baseboard 46 has a first side 48 and a second side 50. As illustrated, the first side 48 of the baseboard 46 corresponds to the second surface 24 of the housing 20 and comprises the recess 26. However, it will be understood that the first side 48 of the baseboard 46 may correspond to the first surface 22 of the housing 20 without departing from the scope of the present invention. A first film of lateral conductors 52 is disposed between the second side 50 of the baseboard 46 and a third sheet 54. A second film of lateral conductors 56 is disposed between the third sheet 54 and a fourth sheet 58. A third film of lateral conductors 60 is disposed between the fourth sheet 58 and a fifth sheet 62. The individual lateral conductors 32 contained in each of

the first, second, and third films of lateral conductors 52, 56, and 60 are coupled to their respective pins 16. Although the present invention has been described in reference to the embodiment illustrated in FIGURE 2, it will be understood that the pin-grid array semiconductor package 14 may include any number of sheets 40 and films of lateral conductors 41 without departing from the scope of the resent invention.

A semiconductor die 64 is disposed within the recess 26 and may be temporarily attached to the baseboard 46 with an adhesive 66. The semiconductor die 64 includes a number of conductor wires 68 that are routed through the stair-stepped cutout 28. Each individual conductor wire 68 from the semiconductor die 64 is electrically coupled to an individual lateral conductor 32. Thus, the semiconductor die 64 may communicate with the circuit board 11 via an electrical path through the conductor wires 68, lateral conductors 32, and pins 16, which are received in the receiving socket 12 or otherwise coupled to the circuit board 11.

The conductor wires 68 are surrounded by an insulating mold material 70 which fills the stair-stepped cutout 28. The insulating mold material 70 electrically isolates the individual conductor wires 68 from each other and protects the conductor wires 68 from damage. In one embodiment, the insulating mold material 70 also surrounds the semiconductor die 64 such that the recess 26 is filled with the insulating mold material 70. However, it will be understood that the recess 26 may be partially filled or not filled with the insulating mold material 70 and remain within the scope of the present invention. For example, the recess 26 may remain open to the environment to enhance cooling of the semiconductor die 64 during operation.

As discussed previously, each conductor wire 68 from the semiconductor die 64 is electrically coupled to a specific pin 16. Each pin 16 comprises a first-

end 72 and a second-end 74. In the embodiment illustrated in FIGURE 2, the first-end 72 of the pin 16 protrudes beyond the first surface 22 of the housing 20. In this embodiment, the second-end 74 of each pin 16 forms a receptacle 76 at the second surface 24 of the housing 20. As will be discussed below, the receptacle 76 is sized to receive a corresponding pin of another semiconductor package. It will be understood that the second-end 74 of each pin 16 may be otherwise configured without departing from the scope of the present invention. For example, the second-end 74 of each pin 16 may be disposed within the housing 20 without forming the receptacle 76. The stair-stepped design of the housing 20 allows the overall size of the pin-grid array semiconductor package 14 to be reduced to approach the size of the semiconductor die 64. Accordingly, the area required by the pin-grid array semiconductor package 14 on the circuit board 11 is reduced.

As will be discussed in greater detail below, multiple semiconductor packages may be connected to the pin-grid array semiconductor package 14 by stacking one on top of another. To facilitate communication with multiple semiconductor packages, a number of direct communication pins 78 may be included within the pin grid array 18. The direct communication pins 78 are not electrically coupled to the semiconductor die 64. The direct communication pins 78 operate to provide individual communication with the multiple semiconductor packages that are coupled to the pin-grid array semiconductor package 14.

FIGURE 3 is an exploded cross-sectional view with portions broken away of a three-dimensional semiconductor stack 80 constructed in accordance with one embodiment of the present invention. Individual semiconductor packages are stacked on the pin-grid array semiconductor package 14 to form the three-dimensional semiconductor stack 80. The three-

dimensional semiconductor stack 80 is generally coupled to the receiving socket 12, shown in FIGURE 1. As illustrated in FIGURE 3, the three-dimensional semiconductor stack 80 comprises a second semiconductor package 114 coupled to the pin-grid array semiconductor package 14. The pin-grid array semiconductor package 14 includes pins 16 that have receptacles 76. The second semiconductor package 114 comprises a number of pins 116 in a second pin-grid array 118 that may correspond to the pattern of receptacles 76 in the pin-grid array semiconductor package 14. When the second semiconductor package 114 and the pin-grid array semiconductor package 14 are stacked together, the pins 116 of the second semiconductor package 114 are received in the receptacles 76 of the pin-grid array semiconductor package 14.

In one embodiment, as shown in FIGURE 3, the pin-grid array 18 of the pin-grid array semiconductor package 14 may include the direct communication pins 78 that allow communication between the circuit board 11 and the second semiconductor package 114. The pin-grid array semiconductor package 14 may also include additional pins 16 that operate to provide communication with the second semiconductor package 114 without directly communicating with the circuit board 11. For example, if the pin-grid array semiconductor package 14 is an integrated circuit chip, the second semiconductor package 114 could be a memory chip that provides additional resident memory for the integrated circuit chip. It will be understood that additional semiconductor packages may be stacked together to form the desired three-dimensional stack 80. Each additional pin-grid array semiconductor package 14 may contain pins 16 and direct communication pins 78 in any desired pattern such as to allow communication throughout the three-dimensional stack 80 and with the circuit board 11. It will be understood that the pin grid array 18 and the three-dimensional stack 80 may be

otherwise configured without departing from the scope of the present invention. For example, additional pins 16 having receptacles 76 may be incorporated into the pin-grid array semiconductor package 14 such that the number of receptacles 76 used for communicating with the second semiconductor package 114 is greater than the number of pins 16 that communicate with the receiving socket 12.

The three-dimensional stack 80 allows additional computing power to be incorporated into a small space on the circuit board 11. The three-dimensional stack 80 also increases the flexibility of the pin-grid array semiconductor package 14. For example, the three-dimensional stack 80 may be used to increase the memory of the pin-grid array semiconductor package 14, upgrade the pin-grid array semiconductor package 14, or other suitable applications.

Although the present invention has been described with reference to several specific embodiments, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications that follow within the scope of the invention which is solely defined by the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a housing comprising a first surface and a second surface;

a semiconductor die disposed within the housing, the semiconductor die comprising a plurality of conductor wires;

a lateral conductor coupled to each of the plurality of conductor wires;

a pin coupled to each of the lateral conductors, each pin comprising a first end and a second end, the second end comprising a receptacle at the second surface of the housing.

2. The semiconductor package of Claim 1, further comprising at least one direct communication pin extending between the first side and the second side of the housing.

3. The semiconductor package of Claim 1, wherein the semiconductor die is disposed within a recess in the housing, and the housing comprises a stair stepped cutout between the recess and the first surface of the housing.

4. The semiconductor package of Claim 1, wherein the housing comprises a plurality of sheets.

5. The semiconductor package of Claim 1, wherein the housing has at least one stair, with each stair having a portion of the plurality of lateral conductors.

6. The semiconductor package of Claim 1, further comprising a molding material surrounding the semiconductor die and filling the recess.

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7. The semiconductor package of Claim 1, wherein the lateral conductors are constructed within at least one film of lateral conductors.

8. The semiconductor package of Claim 1, wherein the housing comprises a film of lateral conductors disposed between a baseboard and a sheet.

9. The semiconductor package of Claim 1, wherein at least one of the pins have a first end that protrudes beyond the first surface of the housing.

10. A semiconductor package comprising:

a housing having at least one stair;

a plurality of lateral conductors disposed within each stair;

a semiconductor die disposed within the housing, the semiconductor die having a plurality of conductor wires with each conductor wire coupled to a lateral conductor; and

a pin coupled to each of the lateral conductors.

11. The semiconductor package of Claim 10, further comprising a direct communication pin disposed between a first surface and a second surface of the housing.

12. The semiconductor package of Claim 10, wherein a second end of a number of the pins comprises a receptacle.

13. The semiconductor package of Claim 10, wherein the plurality of lateral conductors are constructed within a film of lateral conductors associated with each stair.

14. The semiconductor package of Claim 10, further comprising a second semiconductor package coupled to the pin-grid array semiconductor package.

15. A method fabricating a semiconductor package, the method comprising:

providing a housing having a recess and a stair stepped cutout that forms a stair, the stair having a number of lateral conductors, with each lateral conductor electrically isolated from the other lateral conductors;

disposing a semiconductor die into the recess of the housing, the semiconductor die having a plurality of conductor wires that extend through the stair stepped cutout of the housing;

coupling each conductor wire to a lateral conductor;

coupling a pin to each of the lateral conductors; and

encapsulating the conductor wires in a mold material.

16. The method of Claim 15, further comprising the step of encapsulating the semiconductor die in a mold material.

17. The method of Claim 15, wherein the step of coupling a pin to each of the plurality of lateral conductors comprises the step of press fitting a pin into each of the plurality of lateral conductors, the pin extending through the housing and extending past a surface of the housing.

18. The method of Claim 15, wherein the step of providing a housing comprises the step of providing a housing having a recess and a stair stepped cutout that forms a stair, the stair constructed from at least one sheet and a number of lateral conductors constructed

within a film of lateral conductors, each lateral conductor electrically isolated from the other lateral conductors.

19. The method of Claim 15, further comprising the step of coupling a second semiconductor package to the pin-grid array semiconductor package to form a three-dimensional semiconductor package stack.

20. The method of Claim 15, wherein the step of coupling a pin to each of the plurality of lateral conductors comprises the step of coupling a pin having a receptacle to each of the plurality of lateral conductors.