PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H05K 3 /00 — A2

(11) International Publication Number: WO 00/04753

(43) International Publication Date: 27 January 2000 (27.01.00)

(21) International Application Number: PCT/US99/16121

(22) International Filing Date: 16 July 1999 (16.07.99)

(30) Priority Data:
09/119,467 20 July 1998 (20.07.98) US

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, P.O. Box 58119, Santa Clara, CA 95052 (US).

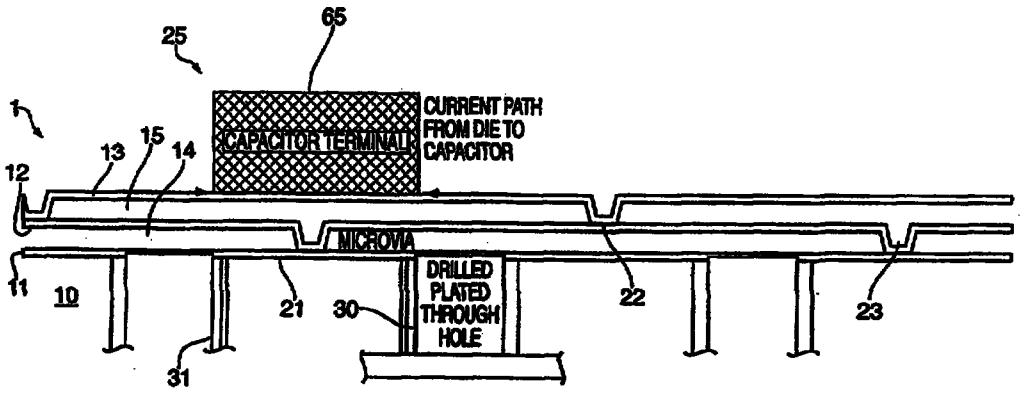
(71)(72) Applicant and Inventor: BURTON, Edward, A. [US/US]; 679 N.E. Valarie Court, Hillsboro, OR 97124 (US).

(74) Agents: O'DOWD, Shawn, W. et al.; Kenyon & Kenyon, Suite 600, 333 W. San Carlos Street, San Jose, CA 95110 (US).

(81) Designated States: CN, DE, GB, KR, SG.

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: ALIGNMENT OF VIAS IN CIRCUIT BOARDS OR SIMILAR STRUCTURES



(57) Abstract

An improvement is presented for connecting conductive components of a built–up circuit board. Rather than using vias or micro vias to connect a conductive layer to a conductive component separated by an insulating layer, an elongated via is used. In one embodiment, the elongated via has a length that is sufficient to directly coupled a first layer to the edge of a via in a lower layer. Thus, it can be said that the elongated via "self–aligns" with the via in the lower layer. In doing so, electrical connections from one side of a circuit board to a component coupled to the other side of the circuit board are more direct leading to a reduction in parasitic induction.