

P. 1114 4.1.11
C. A. Clark

PATENT SPECIFICATION

(11) 1 351 352

1 351 352

- (21) Application No. 11067/71 (22) Filed 23 April 1971
(31) Convention Application No. 7 006 143
(32) Filed 28 April 1970 in
(33) Netherlands (NL)
(44) Complete Specification published 24 April 1974
(51) International Classification H04N 9/02 5/48
(52) Index at acceptance
H4F D1B1 D1D9 D1K1 D1X D30A D30C D30Q



(54) CIRCUIT FOR A COLOUR TELEVISION RECEIVER INCLUDING A CHROMINANCE SIGNAL AMPLIFIER STAGE

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a circuit for a colour television receiver comprising a chrominance signal amplifier stage, comprising a long-tailed pair of first and second transistors with the output current path of a third transistor in the tail, a load impedance being connected to the output electrode of the first transistor.

A circuit of this kind is known from co-pending Application 15556/69 (Serial No. 1241128) in which the output electrode of the second transistor is coupled through a further impedance to the output electrode of the first transistor and supplies a chrominance signal which can be influenced by a voltage between the bases of these transistors. This voltage originates from a contrast adjusting circuit and is combined with a beam current limiting voltage.

However, optimum amplification is not obtained for the burst signal component of the chrominance signal with this known circuit.

An object of the present invention is to provide a circuit including a chrominance signal amplifier stage which can have a large amplification for the burst signal.

The invention provides a circuit for a colour television receiver, comprising a chrominance signal amplifier stage comprising a long-tailed pair of first and second transistors with the output current path of a third transistor in the tail, a load impedance connected to the output electrode of the first transistor, and a fourth transistor having its output current path connected between a first point on the connection between the load impedance and the output

electrode of the first transistor and a second point on the connection between the third transistor and the pair, the circuit including a pulse source having its output coupled to said stage for feeding a pulse thereto during each occurrence of a burst component of a chrominance signal to render the coupling between the fourth transistor and the load impedance during each said occurrence substantially independent of the current balance between the transistors of the pair in the absence of said pulse and a burst signal processing circuit having its input coupled to said load impedance.

With this circuit the amplification for the burst signal component can be equal to the maximum amplification of the chrominance signal.

In order that the invention may be readily carried into effect, embodiments thereof will now be described in detail, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of a colour television receiver including a chrominance signal amplifier stage shown in detail, and

Figure 2 is a block diagram of a colour television receiver including a chrominance signal amplifier stage shown in detail, which stage also serves as a separator stage for burst and chrominance signals.

In Figure 1 an RF, IF and detection section 1 of the receiver has an aerial input 3, an output 5 for a luminance signal Y, an output 7 for a chrominance signal Chr, and an output 9 for a synchronizing signal S.

The output 5 of the section 1 is connected to an input 11 of a luminance signal amplifier 13, an output 15 of which is connected to an input 17 of a picture display section 19. A control signal input 21 of the luminance signal amplifier 13 is connected to an output 23 of a combination circuit 25. An input 27 of this combination circuit is connected to a contrast adjusting circuit 29 and an input 31 is connected to an output 33 of a deflection

[Price 25p]

Price 75c

current and EHT generator 35, an input 37 of which is fed from the output 9 of the section 1.

5 The generator 35 supplies a beam current limiting voltage at its output 33, and also vertical and horizontal deflection currents to the display section 19 and pulses to two outputs 39 and 41 which will be further referred to hereinafter.

10 The chrominance signal output 7 of the section 1 is connected to an input 43 of an amplifier 45 an output 47 of which is connected to an input 49 of a chrominance signal amplifier stage 51.

15 The chrominance signal amplifier stage 51 has an output 53 which is connected to an input 55 of a demodulation and matrix circuit 57 and to an input 59 of a burst gate 61.

20 The burst gate 61 has an input 63 to which are applied burst gating pulses from the output 39 of the generator 35. During the occurrence of these gating pulses the burst gate 61 conducts and supplies a burst signal at an output 65. The output 65 is connected to an input 67 of a rectifier circuit 69 which converts the burst signal into a direct voltage which appears at an output 71. The output 71 is connected to a gain control signal input 73 of the amplifier 45, in a sense such that the automatic gain control loop established thereby tends to maintain the amplitude of the burst at the output 53 of the amplifier stage 51 constant.

35 The chrominance signal amplifier stage 51 comprises transistors 75, 79, 83, 87, 91 and 93 connected as shown. The emitter of transistor 75 is connected to earth through a resistor 77. The collector of transistor 79 is connected through a load resistor 81 to a positive voltage supply and also direct to the output 53. The bases of transistors 79 and 91 are connected to voltage supplies V_1 and V_2 respectively. The base of transistor 83 is connected to an adjusting signal input 85 of the stage 51 which is supplied from the output 23 of the combination circuit 25 with a voltage which is dependent on the contrast adjustment and the beam current in a display tube in the section 19.

50 The collectors of transistors 83 and 93 are connected to a positive supply voltage independently of that of transistor 79.

55 The base of transistor 87 is connected to an input 89 which is connected to the output 41 of the generator 35. A positive pulse is applied to this input 89 during each line flyback period.

60 The base of transistor 93 is connected to an input 95 which is connected to a saturation adjusting circuit 97.

65 The operation of the chrominance signal amplifier stage 51 is as follows. A chrominance signal applied to the base of transistor 75 appears in an amplified form at

its collector. Transistor 87 conducts during the occurrence of the positive-going pulses at its base and the transistors 91 and 93 are cut off. The entire collector current of the transistor 75 then passes through the transistor 87 to the load resistor 81.

During the line scan periods the voltage at the base of transistor 87 is such that this transistor is cut off. The collector current of the first transistor 75 then divides between the transistors 91 and 93 in a ratio which is dependent on the voltage difference between the bases of these transistors and hence on the adjustment of the saturation adjusting circuit 97.

The portion of the current flowing through the transistor 91 is itself divided between the transistors 79 and 83 in a ratio which depends on the voltage difference between the bases of these transistors and hence on the contrast adjusting circuit 29 and the beam circuit limiting voltage.

Hence, a burst signal is periodically produced across the load resistor 81, which burst signal is independent of the adjustments of contrast and saturation. This burst signal alternates with a chrominance signal which is dependent on said adjustments. The ratio between these signals is independent of the gain control voltage which is applied to the input 73 of the amplifier 45, which control voltage is determined only by the burst amplitude (because of the provision of the gate 61) but which is present continuously (because of the action of the rectifier circuit 69) and therefore affects the amplitudes of the burst and chrominance signals at input 49 in the same way.

The saturation adjusting circuit may be omitted if desired, in which case transistors 91 and 93 can be omitted and the emitters of transistors 79 and 83 connected directly to the collector of transistor 75. Alternatively, the function of the transistor pair 79, 83 may be interchanged with that of transistor pair 91, 93 by interchanging the signals applied to inputs 85 and 95.

The amplifier 45 may be omitted and a first further transistor may be included, for example, between the collector of transistor 75 and the emitters of transistors 87, 91 and 93, the emitter of the further transistor being connected to the collector of transistor 75 and its collector being connected to the emitters of the transistors 87, 91 and 93. The collector of transistor 75 should then be also connected to the emitter of a second further transistor whose collector is connected to a positive supply voltage in such manner that its collector circuit is independent of that of the first further transistor, the automatic gain control voltage being applied between the bases of these further transistors.

A direct current compensation circuit

70

75

80

85

90

95

100

105

110

115

120

125

130

may, if desired, be provided for each of the transistor pairs 79, 83 and 91, 93 of the amplifier stage 51 or the various transistor pairs in the stage may be driven in push-pull.

The bias voltages applied to inputs 85 and 95 may alternatively be applied in different ways to the corresponding transistor pairs, for example, to the base of the other transistor of the pair or with opposite variation to the bases of both transistors of one pair.

The stage 51 is eminently suitable for construction as an integrated circuit.

In Figure 2 corresponding components are denoted by the same reference numerals as those in Figure 1.

The circuit arrangement of Figure 2 differs from that of Figure 1 in the following:

A pulse signal originating from the output 41 of the generator 35 is applied to the base of transistor 83 through a combination circuit 99 in which it is combined with a direct voltage originating from the saturation adjusting circuit 97.

The collector of transistor 83 is connected to the positive supply voltage through a load resistor 82 and also to an output 54 which is connected to the input 55 of the demodulation and matrix circuit 57.

The output 53 is connected directly to the input 67 of the rectifier circuit 69 without the interposition of a burst gate (61 in Figure 1).

The input 85 is connected to the base of transistor 91 and transistor 93 of Figure 1 is omitted.

The bases of transistors 87 and 79 are connected to voltage supplies V_3 and V_4 respectively.

The contrast adjusting voltage at the input 85 influences the current distribution between the transistors 87 and 91 because it varies the voltage difference between the bases of these transistors.

Of the portion of the current flowing through transistor 91, part flows through the transistor 83 to the load resistor 82 thereof. This part and hence the saturation can be adjusted by means of the output of the saturation adjusting circuit 97.

However, during the occurrence of the burst signal transistor 83 is cut off as a result of the (now negative-going) pulse signal effectively applied between the bases of transistors 79 and 83 and originating from the output 41 of the generator 35. The output current from transistor 91 then flows through transistor 79 to the load resistor 81 thereof. Thus the entire output current of transistor 75 always flows through the load resistor 81 during the occurrence of the burst signal, independently of the contrast or saturation adjustment.

The amplifier stage 51 thus also separates the burst portion of the chrominance signal

from the picture content portion thereof.

The possible modifications described with reference to the embodiment of Figure 1 also apply correspondingly to the embodiment of Figure 2. For example, saturation adjusting circuit 97 may be omitted together with transistor 91, the emitters of transistors 79 and 83 then being connected directly to the collector of transistor 75. The output of circuit 25 must then be applied effectively between the bases of transistors 79 and 83, instead of the output of circuit 97.

If the stage 51 is constructed to provide push-pull outputs the burst and chrominance signals may be produced in a balanced form, so that direct current pulses which occur in the outputs as a result of the pulse signal applied from the generator 35 can be suppressed at the inputs of the demodulation and matrix circuit 57 and the circuit 69 by using differential amplifiers (common mode rejection).

It will be evident that the pulse signal may alternatively be applied to the base of transistor 79 with opposite polarity, or partially to each of transistors 79 and 83. One or more of the transistors 87, 79, 83 may be controlled by the pulse signal so as to achieve the desired effect. In the second embodiment the transistor 91 may alternatively be controlled by the pulse signal, thereby operating on the transistor 87 as a result of the coupling between these transistors. In the first embodiment transistors 83 and 93 may be controlled by a pulse signal of opposite polarity instead of transistor 87.

WHAT WE CLAIM IS:—

1. A circuit for a colour television receiver, comprising a chrominance signal amplifier stage comprising a long-tailed pair of first and second transistors with the output current path of a third transistor in the tail, a load impedance connected to the output electrode of the first transistor, and a fourth transistor having its output current path connected between a first point on the connection between the load impedance and the output electrode of the first transistor and a second point on the connection between the third transistor and the pair, the circuit including a pulse source having its output coupled to said stage for feeding a pulse thereto during each occurrence of a burst component of a chrominance signal to render the coupling between the fourth transistor and the load impedance during each said occurrence substantially independent of the current balance between the transistors of the pair in the absence of said pulse and a burst signal processing circuit having its input coupled to said load impedance.

may, if desired, be provided for each of the transistor pairs 79, 83 and 91, 93 of the amplifier stage 51 or the various transistor pairs in the stage may be driven in push-pull.

5 The bias voltages applied to inputs 85 and 95 may alternatively be applied in different ways to the corresponding transistor pairs, for example, to the base of the other transistor of the pair or with opposite variation to the bases of both transistors of one pair.

10 The stage 51 is eminently suitable for construction as an integrated circuit.

15 In Figure 2 corresponding components are denoted by the same reference numerals as those in Figure 1.

The circuit arrangement of Figure 2 differs from that of Figure 1 in the following:

20 A pulse signal originating from the output 41 of the generator 35 is applied to the base of transistor 83 through a combination circuit 99 in which it is combined with a direct voltage originating from the saturation adjusting circuit 97.

25 The collector of transistor 83 is connected to the positive supply voltage through a load resistor 82 and also to an output 54 which is connected to the input 55 of the demodulation and matrix circuit 57.

30 The output 53 is connected directly to the input 67 of the rectifier circuit 69 without the interposition of a burst gate (61 in Figure 1).

35 The input 85 is connected to the base of transistor 91 and transistor 93 of Figure 1 is omitted.

The bases of transistors 87 and 79 are connected to voltage supplies V_3 and V_4 respectively.

40 The contrast adjusting voltage at the input 85 influences the current distribution between the transistors 87 and 91 because it varies the voltage difference between the bases of these transistors.

45 Of the portion of the current flowing through transistor 91, part flows through the transistor 83 to the load resistor 82 thereof. This part and hence the saturation can be adjusted by means of the output of the saturation adjusting circuit 97.

50 However, during the occurrence of the burst signal transistor 83 is cut off as a result of the (now negative-going) pulse signal effectively applied between the bases of transistors 79 and 83 and originating from the output 41 of the generator 35. The output current from transistor 91 then flows through transistor 79 to the load resistor 81 thereof. Thus the entire output current of transistor 75 always flows through the load resistor 81 during the occurrence of the burst signal, independently of the contrast or saturation adjustment.

65 The amplifier stage 51 thus also separates the burst portion of the chrominance signal

from the picture content portion thereof.

The possible modifications described with reference to the embodiment of Figure 1 also apply correspondingly to the embodiment of Figure 2. For example, saturation adjusting circuit 97 may be omitted together with transistor 91, the emitters of transistors 79 and 83 then being connected directly to the collector of transistor 75. The output of circuit 25 must then be applied effectively between the bases of transistors 79 and 83, instead of the output of circuit 97.

If the stage 51 is constructed to provide push-pull outputs the burst and chrominance signals may be produced in a balanced form, so that direct current pulses which occur in the outputs as a result of the pulse signal applied from the generator 35 can be suppressed at the inputs of the demodulation and matrix circuit 57 and the circuit 69 by using differential amplifiers (common mode rejection).

It will be evident that the pulse signal may alternatively be applied to the base of transistor 79 with opposite polarity, or partially to each of transistors 79 and 83. One or more of the transistors 87, 79, 83 may be controlled by the pulse signal so as to achieve the desired effect. In the second embodiment the transistor 91 may alternatively be controlled by the pulse signal, thereby operating on the transistor 87 as a result of the coupling between these transistors. In the first embodiment transistors 83 and 93 may be controlled by a pulse signal of opposite polarity instead of transistor 87.

WHAT WE CLAIM IS:—

1. A circuit for a colour television receiver, comprising a chrominance signal amplifier stage comprising a long-tailed pair of first and second transistors with the output current path of a third transistor in the tail, a load impedance connected to the output electrode of the first transistor, and a fourth transistor having its output current path connected between a first point on the connection between the load impedance and the output electrode of the first transistor and a second point on the connection between the third transistor and the pair, the circuit including a pulse source having its output coupled to said stage for feeding a pulse thereto during each occurrence of a burst component of a chrominance signal to render the coupling between the fourth transistor and the load impedance during each said occurrence substantially independent of the current balance between the transistors of the pair in the absence of said pulse and a burst signal processing circuit having its input coupled to said load impedance.



2. A circuit as claimed in Claim 1, wherein the output current path of one transistor of a second long-tailed pair of transistors is included in the connection between the first pair and said second point.

3. A circuit as claimed in Claim 1, wherein the output electrode of the second transistor is connected to a load impedance and to an input of a chrominance signal handling circuit.

4. A circuit as claimed in Claim 3, wherein the output current path of a fifth transistor is included in the connection between the pair and the second point.

5. A circuit as claimed in any preceding

Claim wherein the output of the pulse source is coupled to an electrode of a said transistor for controlling current in the output current path thereof.

6. A circuit for a colour television receiver, substantially as herein described with reference to Figure 1 or Figure 2 of the accompanying drawings.

C. A. CLARK,
Chartered Patent Agent,
Century House,
Shaftesbury Avenue,
London, W.C.2.,
Agent for the Applicants.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1974.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.



* C L H S *