

MEMORY HAVING A LATCHING BICMOS SENSE AMPLIFIERAbstract of the Disclosure

5 A memory (80) having a latching BICMOS sense amplifier
(20) includes a reduced power data retention mode. The latching
BICMOS sense amplifier (20) senses and amplifies differential
data signals corresponding to data from a selected memory cell
(85). A latch (35) temporarily retains the logic state of the
10 differential data signals in response to a clock signal. The
reduced power data retention mode is provided by utilizing
selectable current sources (66 - 75) responsive to an output
enable signal. The latching BICMOS sense amplifier (20) allows
for very high speed operation, yet provides for reduced power
15 consumption while in a latched state.

(FIG.1 accompanies this abstract)