

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO DIGITAL ELECTRONIC ALARM TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 6-31-1, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to digital electronic alarm timepieces of the kind having digital display means for displaying time or a set alarm time, alarm means for producing a sound alarm when the time, as counted by the timepiece, reaches a set alarm time and control switch means for controlling the operation of the timepiece. Though not limited to its application thereto the invention is primarily intended for, and very advantageous for application to digital electronic alarm wrist watches.

There are numerous known examples of digital electronic alarm timepieces of the kind referred to. Some include a plurality of alarm time memorizing counters whereby a plurality of different alarm times can be set. So far as the applicants are aware, however, all these known examples have the defect that the alarm cannot be sounded (i.e. it is effectively out of action) when the control switch means is being operated by a user of the timepiece. The invention seeks to eliminate this defect.

According to the invention a digital electronic alarm timepiece of the kind referred to includes means, actuated both upon operation of the control switch means of the timepiece and upon the occurrence of coincidence between the time counted by said timepiece and a set alarm time, for causing the alarm means of the timepiece to give an alarm.

The timepiece may include a time-standard quartz crystal controlled high frequency oscillator; counter means for producing timing signals from the oscillatory output of said oscillator; digital display means providing a digital display of time; an alarm time keeping circuit for counting an alarm time; time correcting

means; alarm time setting means; switching means for operating said time correcting means; and means actuated by operation of said time correcting switching means for causing the alarm means to sound an alarm.

There may be a plurality of alarm time keeping circuits.

The timepiece may include switch means operable to control the production of pulses for correction of the counts in counters included in the timing signal counter and in said alarm time keeping circuit or circuits; switch means operable to control the production of shift register control pulses; a shift register controlled by the shift register control pulses and selectively controlling the application of the first mentioned pulses to different counters in said timing signal counter means; a second shift register controlled by the shift register control pulses and selectively controlling the application of said first mentioned pulses to said timing signal counter means on the one hand and to said alarm time keeping circuit or circuits on the other; and means actuated upon operation of any of said switch means for causing the alarm means to sound an alarm.

The invention is illustrated in and further described in connection with the accompanying drawings, in which:—

Figure 1 is a simplified diagram of one embodiment; and

Figure 2 is an explanatory graphical Figure.

Referring to Figure 1, block 1 comprises a time standard oscillator OSC, for example a quartz crystal controlled oscillator, and a frequency divider into which the oscillations from said oscillator are fed and which produces therefrom a lower frequency output, for example a 1Hz output. This output is fed to a time counter system 2 which provides therefrom second, minute, hour and day signals. The apparatus in blocks 1 and 2 may be as well known per se and needs no detailed description here.

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Block 5 comprises a set of switches 5a, 5b, 5c and 5d all of which are connected on one side to the positive terminal of a source of potential (not shown) of value V_{DD} . The other terminals of these switches are connected to respective anti-chatter circuits 6a, 6b, 6c, 6d in block 6 and which serve in known manner to eliminate undesired switch noise or chatter effects produced by switch operation. Block 7 contains circuits 7a, 7b, 7c, 7d, respectively connected to the outputs of the anti-chatter circuits 6a, 6b, 6c and 6d. Circuit 7a is arranged to produce an output of positive potential V_{DD} so long as the switch 5a—which is a safety switch—is closed and to produce an output of negative potential (V_{SS}) when said switch 5a is open. The other circuits 7b, 7c and 7d, associated respectively with the set switch 5b, the mode switch 5c and select switch 5d, are pulse producing circuits arranged to produce pulses of a certain pulse width upon operation of the switch with which it is associated.

The outputs of the circuits 7a and 7b are fed to the respective inputs of an AND gate 8 and the outputs of the circuits 7a and 7d are fed to the respective inputs of an AND gate 9. The output of the circuit 7c is connected to a channel selecting shift register 11. The output of the AND gate 8 is connected to one input of each of three AND gates 12a, 12b, 12c shown in block 12 and also to one input of an AND gate 13a included in block 13 and also to one input of an AND gate 14a included in block 14 and in addition to one input of an AND gate 15a included in block 15.

The output of the AND gate 9 is connected to a time-unit selecting shift register 10, which produces a signal at one of its three output terminals (referenced "Day", "hour" and "minute"), the terminal at which said signal appears being determined by the number of pulses the shift register 10 receives.

The three outputs of the shift register 10 are respectively connected to the remaining inputs of the AND gates 12a, 12b and 12c. The outputs of the AND gates 12a, 12b and 12c are respectively connected to one input of each of the AND gates 13b, 13c and 13d; the output of AND gate 12b is also connected to one input of each of the AND gates 14b and 15b; and the output of AND gate 12c is also connected to one input of each of the AND gates 14c and 15c.

The shift register 11 sequentially generates an output signal at its three output terminals W, M1 and M2 in response to a sequence of output pulses from the circuit 7c. The terminal W is connected to the remaining inputs of the AND gates 13a, 13b, 13c and 13d in the

group 13; the terminal M1 is connected to the remaining inputs of the AND gates 14a, 14b and 14c in the group 14; and the terminal M2 is connected to the remaining inputs of the AND gates 15a, 15b and 15c in the group 15. The terminals W, M1 and M2 are also respectively connected to the three inputs of a discriminating circuit 23 which discriminates between the signals at the output terminals W, M1 and M2 of the shift register 11. Output from the discriminating circuit 23 is applied as one input to a display selecting circuit 16 which, under control by the output from circuit 23, selects for display either a time signal display, a first alarm signal display or a second alarm signal display according as to whether the output from circuit 23 corresponds with an input thereto from terminal W, M1 or M2 respectively.

Outputs from the AND gates in the groups 13, 14, and 15 are respectively applied to the system 2, to a first alarm time counter 3 (for a first alarm time display) and a second alarm time counter 4 (for a second alarm time display).

The contents of the system 2, the first alarm counter 3 and the second alarm counter 4 are respectively applied to the remaining three inputs of the display selecting circuit 16, and are also applied to the respective three inputs of a coincidence detector circuit 19 which produces an output signal when the contents of the counters in the system 2 and the alarm counters 3 and 4 are equal.

The display selecting circuit 16 selects, under the control of the selecting signal produced from the discriminating circuit 23, the contents at 2 or in one of the alarm counters 3 and 4 and the counter contents thus selected are passed on from the circuit 16 to a decoder-driver circuit 17 which converts the said contents in known manner into signals for operating a digital display device 18.

The coincidence signal from the coincidence detector 19 is fed to one input of an OR gate 20 the output from which actuates an alarm driver circuit 21 driving an alarm device 22. The outputs of the AND gates 13a, 13b, 13c and 13d are connected to the respective inputs of an OR gate 24; the outputs of the AND gates 14a, 14b and 14c are connected to the respective inputs of an OR gate 25; and the outputs of the AND gates 15a, 15b and 15c are connected to the respective inputs of an OR gate 26. The outputs of the three OR gates 24, 25 and 26 are connected respectively to three of the inputs of a four-input OR gate 27 the fourth input of which is fed from the output of the circuit 7c and the output from which constitutes the second input to the OR gate 20.

The operation of the embodiment represented in Figure 1 will now be described. When only the switch 5c is closed a pulse wave form as shown at line 7c of Figure 2 appears at the output of the pulse generating circuit 7c and sequential output signals as shown at lines W, M1 and M2 of Figure 2 appear at terminals W, M1 and M2 respectively of the channel selecting shift register 11 in dependence upon the number of pulses appearing at the output. These sequential output signals from register 11 serve to select the contents of the counters 2, 3 and 4 for display by the display device 18. The pulse signal from the pulse circuit 7c can actuate the alarm driver 21 via OR gates 27 and 20 and thus cause sounding of an alarm by the alarm device 22. At the same time there is a display of selected counter contents fed out by the display selecting circuit 16 under the control of the output signal from the discriminating circuit 23.

Now the operation of resetting to zero the seconds counter in the counter system 2 will be described. When the switch 5a is closed the output signal level from the circuit 7a is of logic level "1". If now the switch 5c is pushed ON a time display is produced and, because a pulse is produced at the output of the pulse generating circuit 7b, each time the said switch 5b is pushed ON, only the output of the terminal W of the shift register 11 will be of level "1", the remaining two output terminals M1 and M2 being at level "0". Accordingly, only the AND gate 13a in the group 13 is able to pass a pulse signal and this pulse signal operates to reset the seconds counter in the time counter 2. This signal from the AND gate 13a passes the OR gates 24, 27 and 20, and actuates the alarm driver 21 so that an alarm is sounded. Because there is no output from the AND gate 9 (see line 9 of Figure 2) the three outputs (the day, hour and minute outputs) of the shift register 10 become of level "0", the outputs of the AND gates in the group 12 are at level "0" and the AND gates 13b, 13c and 13d give no output.

The operation of resetting to zero the alarm memory counters 3 and 4 will now be described. This is done by closing the switch 5b after selecting the desired channel by closing the switch 5c the required number of times. In the case of resetting the counter 4, the output terminal M2 of register 11 is selected and a pulsed signal which resets counter 4 appears at the output of AND gate 15a. In the case of resetting counter 3, the register terminal selected is terminal M1 and a pulsed signal to reset counter 3 appears at the output of AND gate 14a. Thus either the memory counter 3 or 4 can be reset and, in either

case, an alarm is sounded by a signal fed to alarm driver 21 via OR gate 20 and OR gate 27 and OR gate 25 (in the case of counter 3) or OR gate 26 (in the case of counter 4).

The time correcting operation will now be described. The switch 5a is closed, thus making the output of circuit 7a of level "1". The time unit required to be corrected is selected by pushing the switch 5d the required number of times. If it is required to correct the day counter incorporated in the time counter system 2 the said switch 5d is closed only once whereby one pulse signal is produced at the output of the circuit 7d. This opens the AND gate 9 and only the "day" output terminal of the time unit selecting register 10 becomes of level "1", the "hour" and "minute" outputs of this register remaining at "0". Now closure of the switch 5b will produce an output pulse from circuit 7b and this pulse is passed through AND gate 8 to AND gate 12a which is the only gate in group 12 having its output at level "1". Because at this time only the output W of shift register 11 is at level "1", only the AND gates 13a and 13b are able to produce a pulse signal. It should be pointed out, however, that if day, hour and minute correcting signals are applied only the day figure will be corrected if a second reset signal is arranged to be ineffective in spite of its application. The day correcting signals from AND gates 13a and 13b also actuate the alarm driver 21 via OR gates 24, 27 and 20 and sound the alarm.

Similarly, in the cases of correcting hours and minutes, channel selection is achieved by a suitable number of closures of the switch 5b and a pulse signal is fed to AND gate 8 at each closure. In the case of minutes correction pulses are produced at the output of AND gate 12c and, in the case of hours correction pulses are produced at the output of AND gate 12b. Pulses are thus produced at the outputs of AND gates 13a and 13c in hours correction or at the outputs of AND gates 13a and 13d for minutes correction. If the seconds preset signal is arranged to be inoperative only hours or minutes correcting signals will be effective. Again the hours and minutes correcting pulse signals actuate the alarm driver 21 via OR gates 24, 27 and 20.

Lines 10d, 10h and 10m, of Figure 2 show respectively the outputs at the day, hour and minute outputs of the shift register 10 in the respective cases of day, hour and minute correction.

As regards setting an alarm time this can be done by selecting the appropriate alarm time memory counter 3 or 4 by the shift register 11, a setting pulse being produced at an output of

a gate in one of the AND gate groups 14 or 15. Again, when this is done, a pulse signal actuates the alarm driver 21 via OR gates 20 and 27 and either OR gate 25 or OR gate 26.

When the actual time, as counted and indicated by the timepiece, coincides with a set alarm time, the output of the coincidence detector circuit 19 becomes of level "1", the alarm driver 21 is actuated via the OR gate 20, and the alarm is sounded.

The invention has the practical advantage that the timepiece will make an alarm sound whenever a switching control operation—such as setting an alarm or correcting the time—is made, so that the user of the timepiece is positively notified of such an operation.

Attention is directed to the specification of our copending application No. 9937/77 (Serial No. 1,539,719).

WHAT WE CLAIM IS:—

1. A digital electronic alarm timepiece of the kind referred to and including means, actuated both upon operation of the control switch means of the timepiece and upon the occurrence of coincidence between the time counted by said timepiece and a set alarm time, for causing the alarm means of the timepiece to give an alarm.

2. A timepiece as claimed in Claim 1 and comprising a time-standard quartz crystal controlled high frequency oscillator; counter means for producing timing signals from the oscillatory output of said oscillator; digital display means providing a digital display of time; an alarm time keeping circuit for counting an alarm time; time correcting means; alarm time setting means; switching means for operating said

time correcting means; and means actuated by operation of said time correcting switching means for causing the alarm means to sound an alarm.

3. A timepiece as claimed in Claim 1 or 2 wherein there is a plurality of alarm time keeping circuits.

4. A timepiece as claimed in any of the preceding claims and including switch means operable to control the production of pulses for correction of the counts in counters included in the timing signal counter and in said alarm time keeping circuit or circuits; switch means operable to control the production of shift register control pulses; a shift register controlled by the shift register control pulses and selectively controlling the application of the first mentioned pulses to different counters in said timing signal counter means; a second shift register controlled by the shift register control pulses and selectively controlling the application of said first mentioned pulses to said timing signal counter means on the one hand and to said alarm time keeping circuit or circuits on the other; and means actuated upon operation of any of said switch means for causing the alarm means to sound an alarm.

5. Digital electronic alarm timepieces substantially as herein described with reference to the accompanying drawings.

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10

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time correcting means; and means actuated by operation of said time correcting switching means for causing the alarm means to sound an alarm.

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