CLAIMS

1. A method for forming a semiconductor device, the method comprising:

forming a nanosheet stack over a substrate, the nanosheet stack comprising alternating semiconductor layers and sacrificial layers;

forming a sacrificial liner over the nanosheet stack;

forming a dielectric gate structure over the nanosheet stack and the sacrificial liner;

forming a first inner spacer on a sidewall of the sacrificial layers;

forming a gate over channel regions of the nanosheet stack, the gate comprising a conductive bridge that extends over the substrate in a direction orthogonal to the nanosheet stack; and

forming a second inner spacer on a sidewall of the gate.

2. The method of claim 1, wherein forming the gate further comprises removing a portion of the nanosheet stack and the dielectric gate structure to expose sidewalls of the sacrificial layers.

3. The method of claim 2, wherein forming the gate further comprises removing the sacrificial liner and the sacrificial layers.

4. The method of claim 1, wherein forming the first inner spacer comprises recessing the sacrificial layers.

5. The method of claim 1, wherein forming the gate further comprises:

forming a gate dielectric;

forming a conductive region over the gate dielectric; and

removing exposed portions of the gate dielectric.

6. The method of claim 1 further comprising forming a first source or drain region on a sidewall of the first inner spacer and forming a second source or drain region on a sidewall of the second inner spacer.

7. The method of claim 1 further comprising forming a gate contact on a surface of the conductive bridge.

8. A semiconductor device comprising:

a nanosheet stack over a substrate;

a gate over channel regions of the nanosheet stack, the gate comprising a conductive bridge that extends over the substrate in a direction orthogonal to the nanosheet stack;

a dielectric gate structure over the nanosheet stack and the gate;

a first inner spacer on a first end of the nanosheet stack; and

a second inner spacer on a second end of the nanosheet stack;

wherein a gate dielectric extends between the first inner spacer and the gate but not between the second

inner spacer and the gate.

9. The semiconductor device of claim 8 further comprising a first source or drain region on a sidewall of the first inner spacer.

10. The semiconductor device of claim 9 further comprising a second source or drain region on a sidewall of the second inner spacer.

11. The semiconductor device of claim 8 further comprising a gate contact on a surface of the conductive bridge.

12. The semiconductor device of claim 11, wherein the dielectric gate structure is positioned between the nanosheet stack and the gate contact.

13. A method for forming a semiconductor device, the method comprising:

forming a nanosheet stack over a substrate, the nanosheet stack comprising alternating semiconductor layers and sacrificial layers;

forming a spacer layer over a sidewall of the nanosheet stack;

forming a first dielectric gate structure over the substrate and on a sidewall of the spacer layer;

forming a sacrificial liner on the first dielectric gate structure;

forming a second dielectric gate structure on the sacrificial liner; and

replacing the sacrificial layers, spacer layer, and sacrificial liner with a gate, the gate comprising a conductive bridge positioned between the first dielectric gate structure and the second dielectric gate structure.

14. The method of claim 13 further comprising forming a first inner spacer on a sidewall of the sacrificial layers.

15. The method of claim 14 further comprising forming a second inner spacer on a sidewall of the gate.

16. The method of claim 15 further comprising forming a first source or drain region on a sidewall of the first inner spacer and forming a second source or drain region on a sidewall of the second inner spacer.

17. The method of claim 13 further comprising forming a gate contact on a surface of the conductive bridge.

18. A semiconductor device comprising:

a nanosheet stack over a substrate, the nanosheet stack comprising semiconductor layers;

a first dielectric gate structure on the substrate;

a gate over channel regions of the nanosheet stack, the gate comprising a conductive bridge that extends over the substrate in a direction orthogonal to the nanosheet stack, the conductive bridge on a surface of the first dielectric gate structure; and

a second dielectric gate structure on the conductive bridge.

19. The semiconductor device of claim 18, wherein a gate dielectric extends along a top surface, a bottom surface, and a first sidewall of the semiconductor layers but not along a second sidewall of the semiconductor layers.

20. The semiconductor device of claim 18 further comprising a gate contact on a surface of the conductive bridge.

21. The semiconductor device of claim 20, wherein the gate contact extends through a portion of the second dielectric gate structure.

22. A semiconductor device comprising:

a first nanosheet stack over a substrate;

a second nanosheet stack over the substrate;

a first dielectric gate structure on the substrate, the first dielectric gate structure between the first nanosheet stack and the second nanosheet stack;

a gate having a first portion and a second portion, the first portion over channel regions of the first nanosheet stack and the second portion over channel regions of the second nanosheet stack, the gate comprising a conductive bridge between the first portion and the second portion, the conductive bridge on a surface of the first dielectric gate structure; and

a second dielectric gate structure on the conductive bridge.

23. The semiconductor device of claim 22, wherein a gate dielectric extends along a top surface, a bottom surface, and a first sidewall of a nanosheet of the first nanosheet stack but not along a second sidewall of the nanosheet.

24. The semiconductor device of claim 22 further comprising a gate contact on a surface of the conductive bridge.

25. The semiconductor device of claim 24, wherein the gate contact extends through a portion of the second dielectric gate structure.