FIG. 1

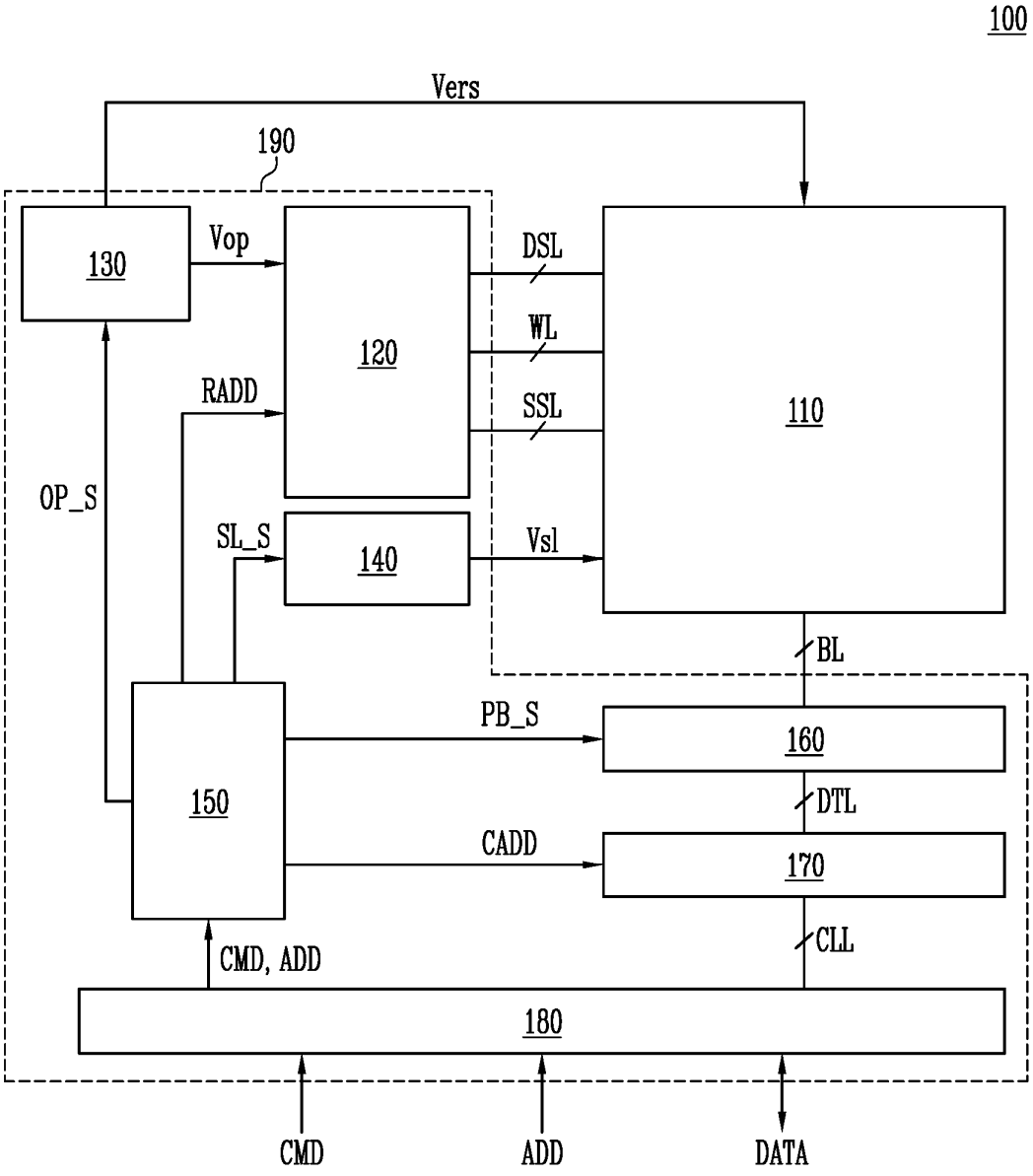

100
Vers
190
130
Vop
120
DSL
WL
SSL
110
RADD
OP_S
SL_S
140
Vsl
BL
PB_S
160
150
DTL
CADD
170
CLL
CMD, ADD
180
CMD
ADD
DATA

FIG. 2

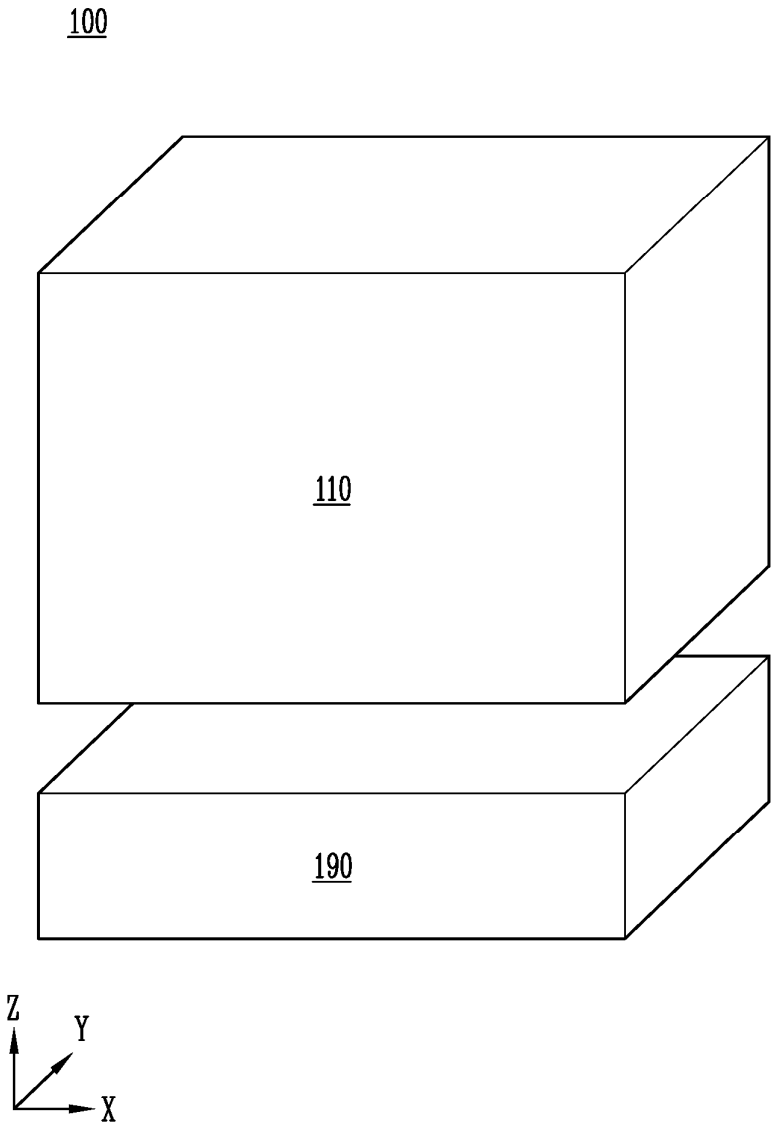


FIG. 3

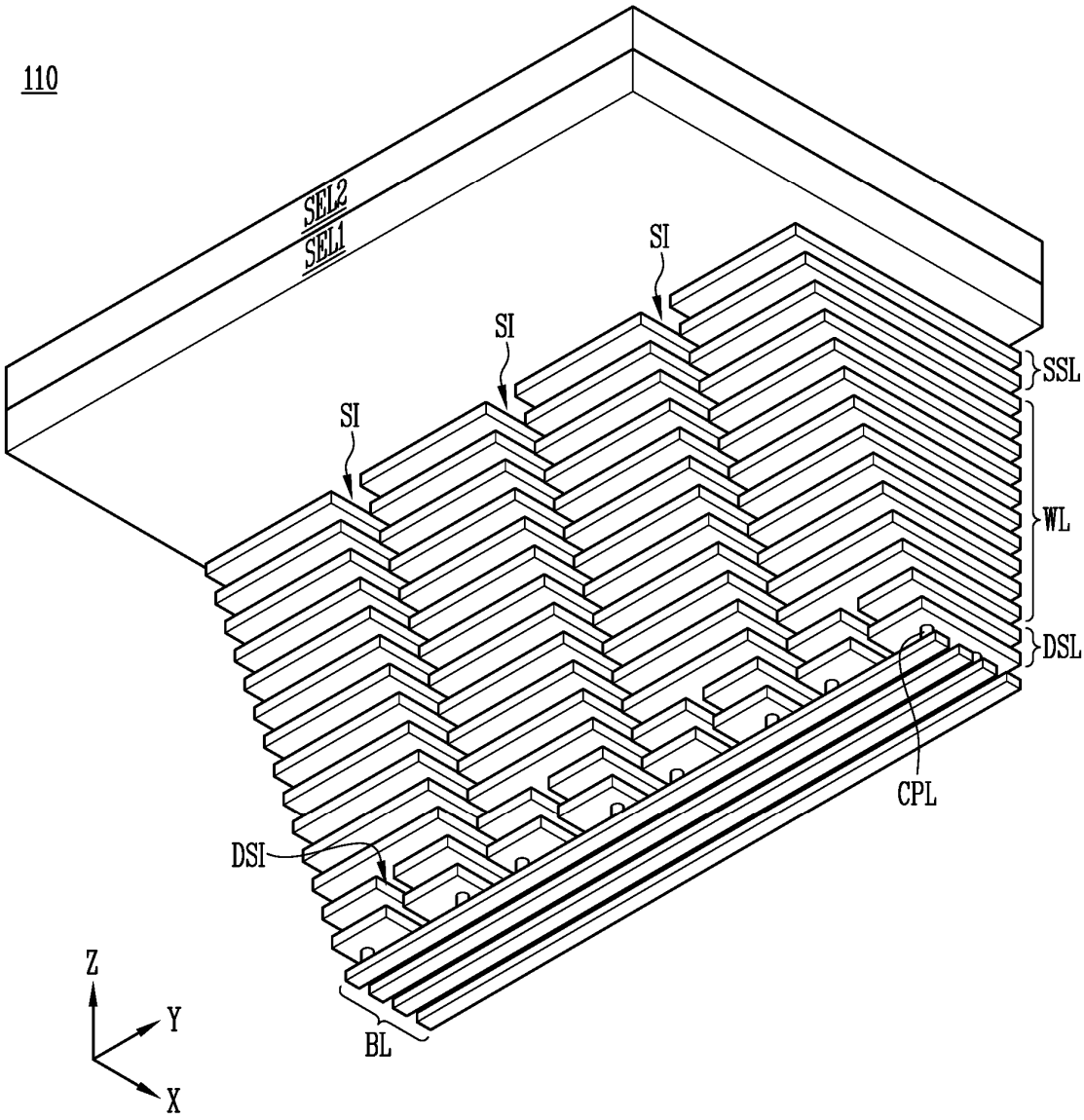


FIG. 4

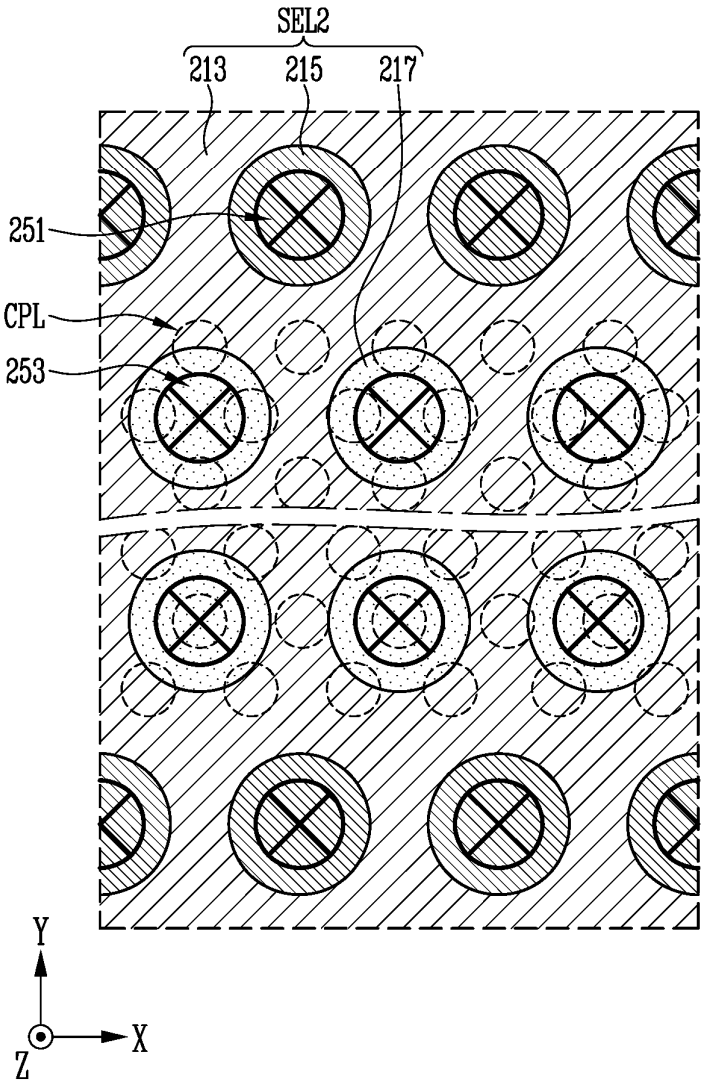


FIG. 5A

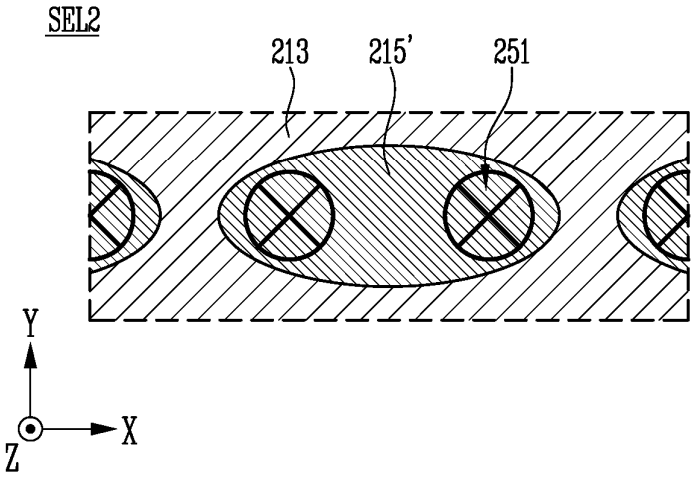


FIG. 5B

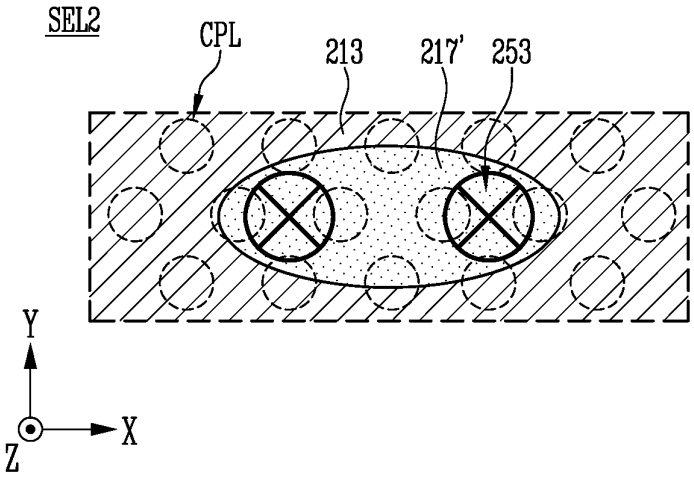


FIG. 6A

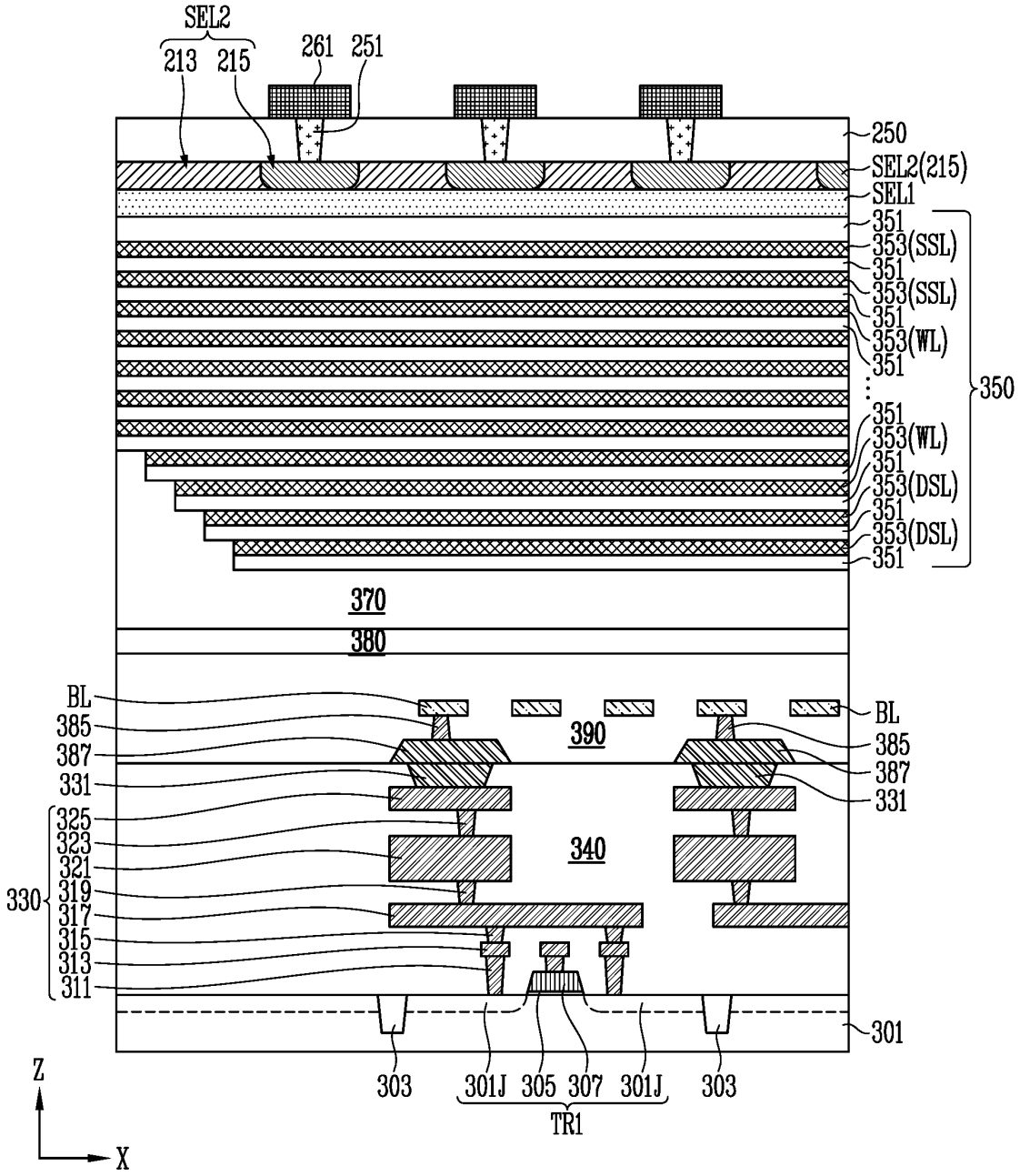

SEL2
213
215
261
251
250
SEL2(215)
SEL1
351
353(SSL)
351
353(SSL)
351
353(WL)
351
351
353(WL)
351
353(DSL)
351
353(DSL)
351
350
370
380
BL
385
387
331
325
323
321
319
317
315
313
311
330
390
340
BL
385
387
331
301
303
301J
305
307
301J
303
TR1
Z
X

FIG. 6B

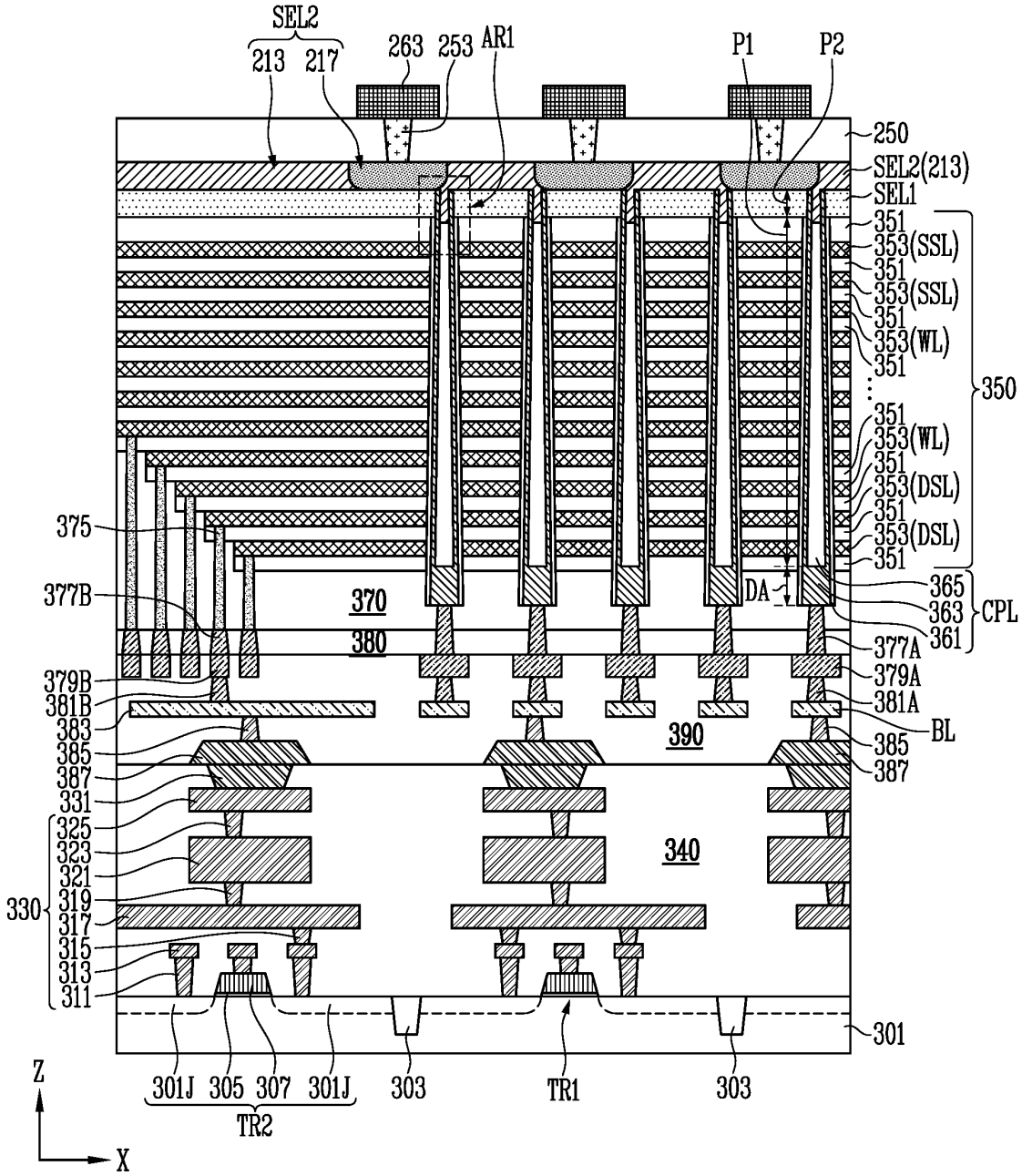

SEL2
213
217
263
253
AR1
P1
P2
250
SEL2(213)
SEL1
351
353(SSL)
351
353(SSL)
351
353(WL)
351
350
351
353(WL)
351
353(DSL)
351
353(DSL)
351
375
377B
370
380
DA
365
363
361
CPL
377A
379A
381A
BL
379B
381B
383
385
387
390
385
387
331
325
323
321
330
319
317
315
313
311
340
301
301J
305
307
301J
303
TR1
303
TR2
Z
X

FIG. 7

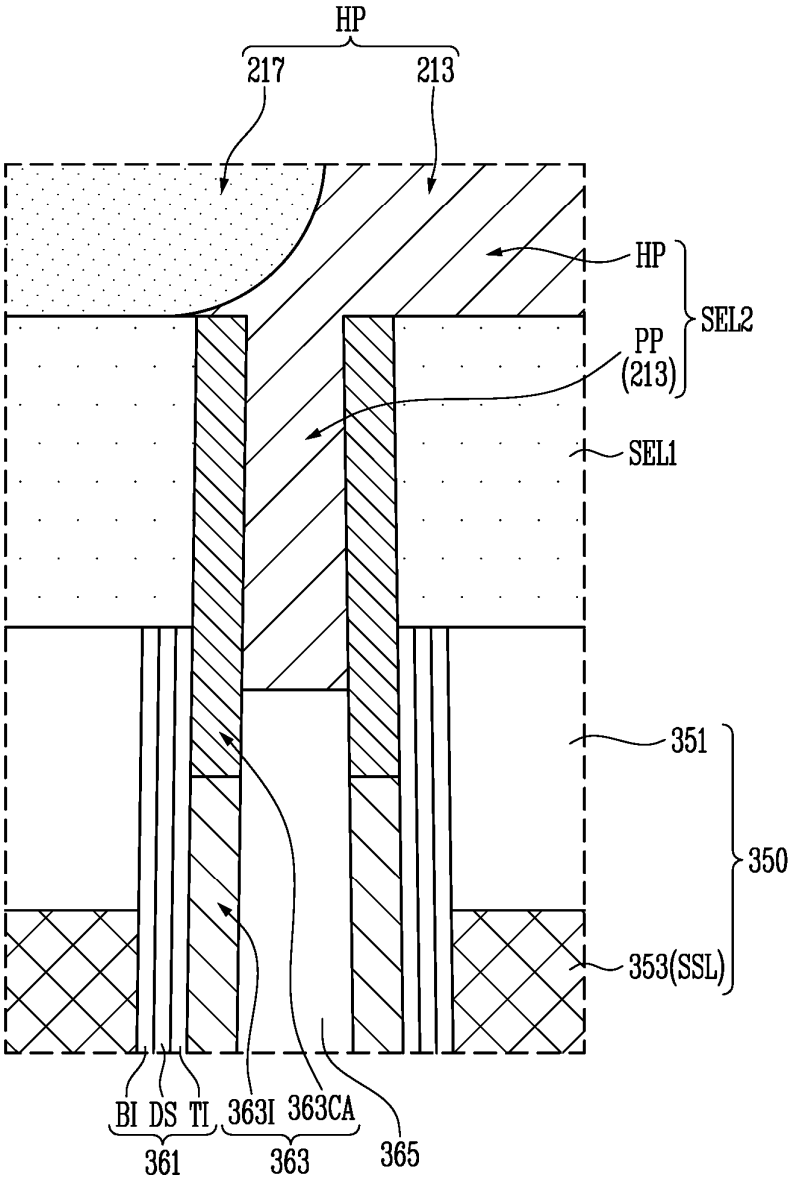

HP
217
213
HP
SEL2
PP
(213)
SEL1
351
350
353(SSL)
BI
DS
TI
363I
363CA
361
363
365

FIG. 8A

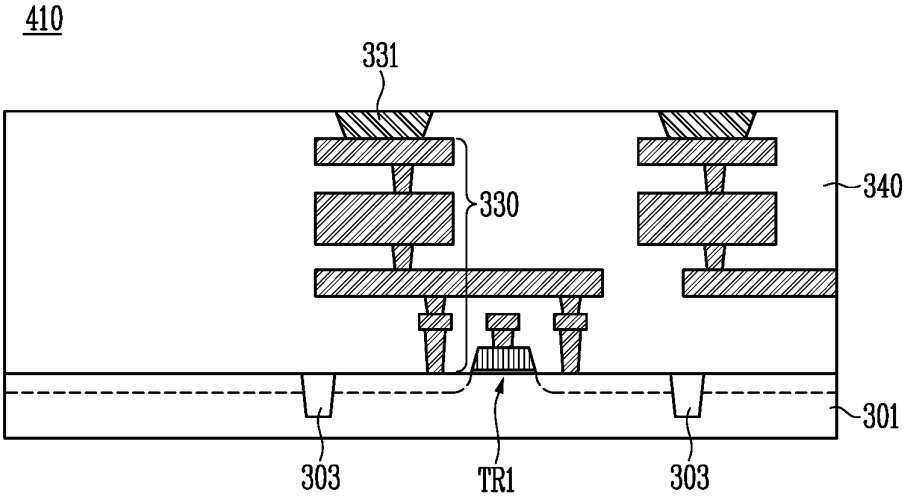

410
331
330
340
301
303
TR1
303

FIG. 8B

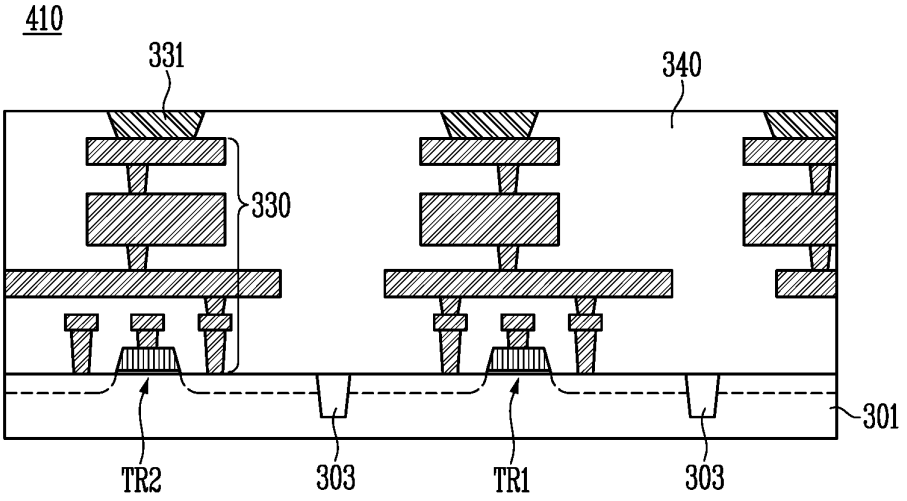

410
331
340
330
301
TR2
303
TR1
303

FIG. 9A

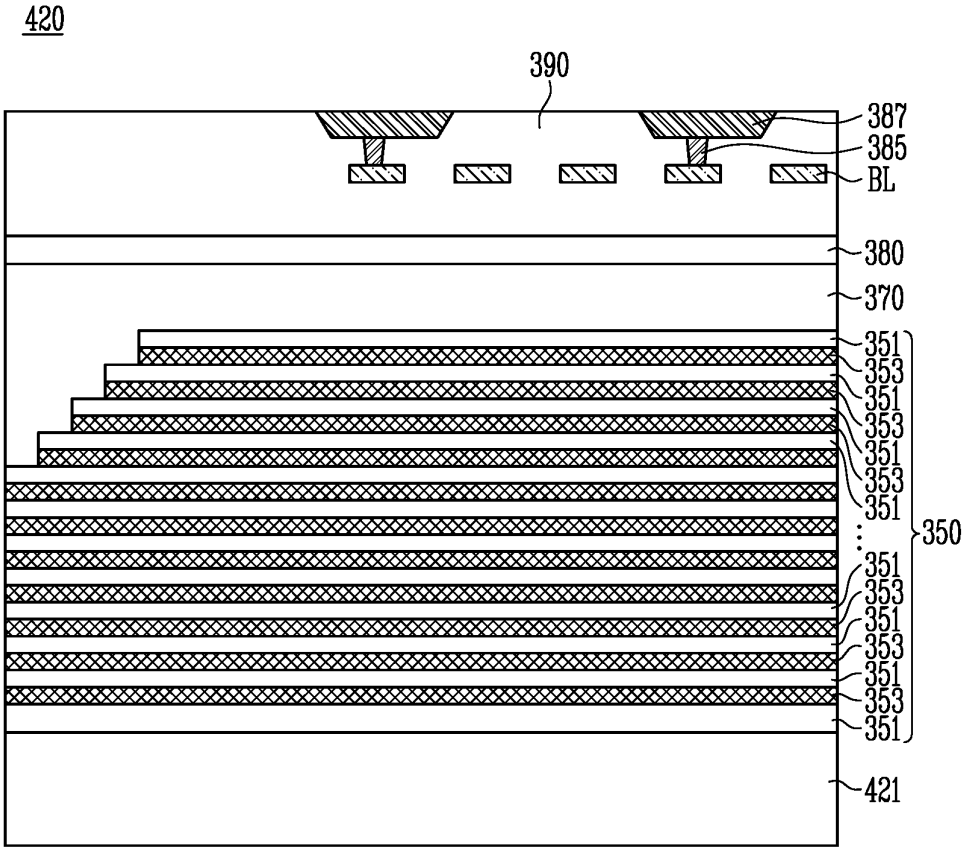

420
390
387
385
BL
380
370
351
353
351
353
351
353
351
350
351
353
351
353
351
353
351
421

FIG. 9B

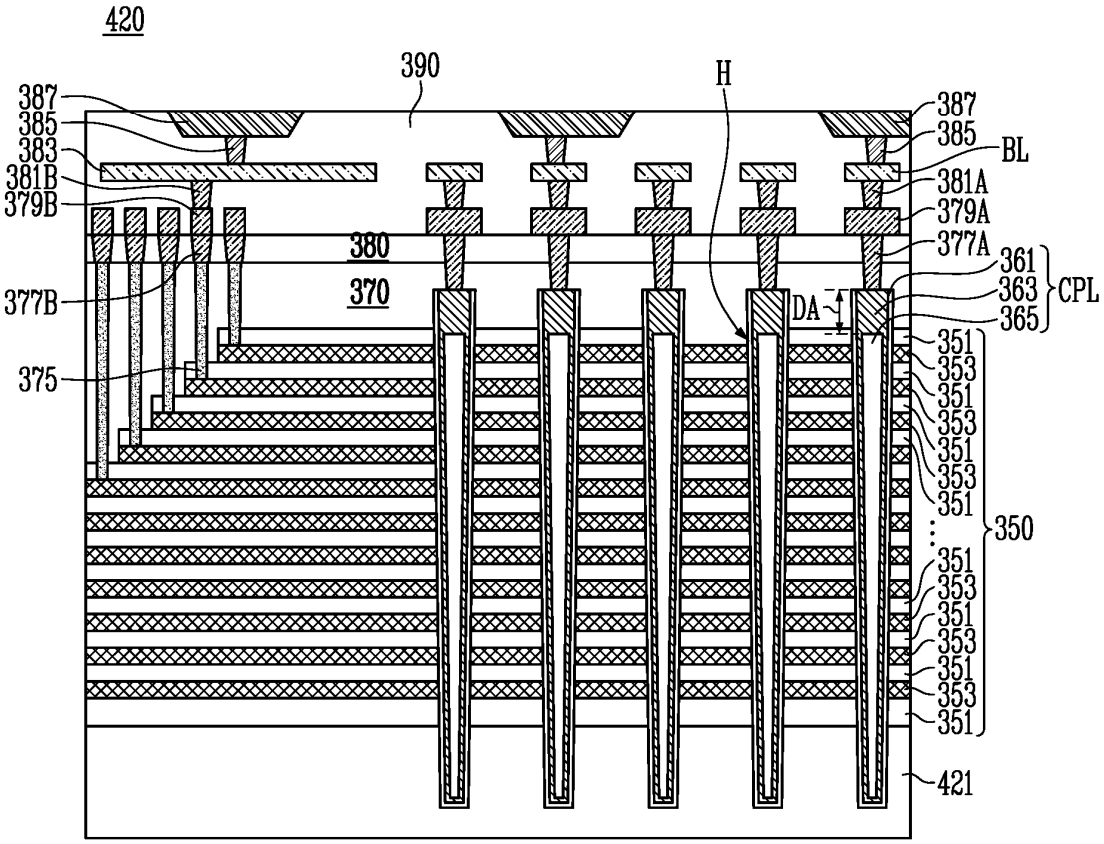

420
390
H
387
385
383
381B
379B
377B
375
380
370
387
385
BL
381A
379A
377A
361
363
365
CPL
DA
351
353
350
421

FIG. 10A

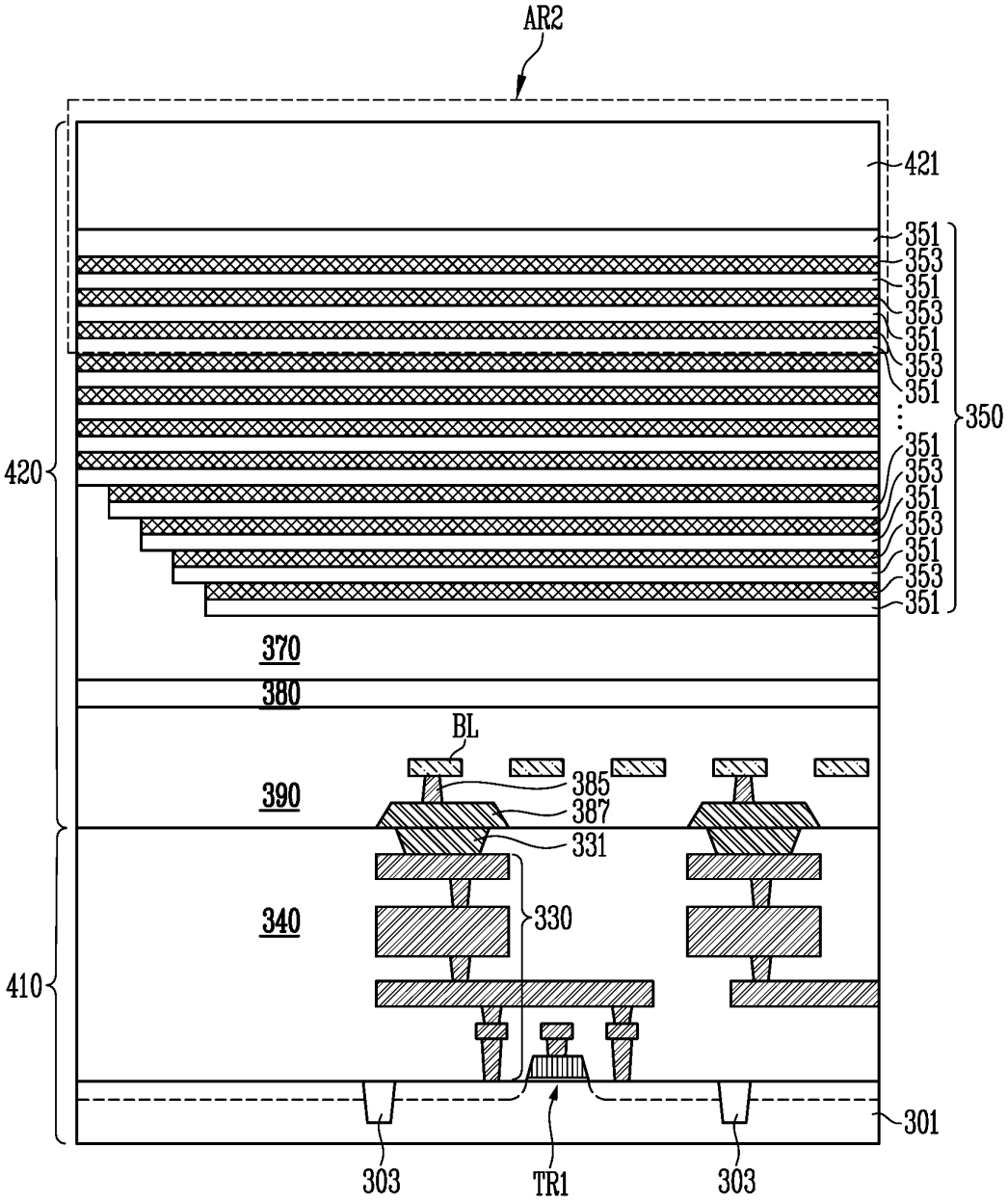

AR2
421
351
353
351
353
351
353
351
350
420
370
380
BL
385
390
387
331
340
330
410
301
303
TR1
303

FIG. 10B

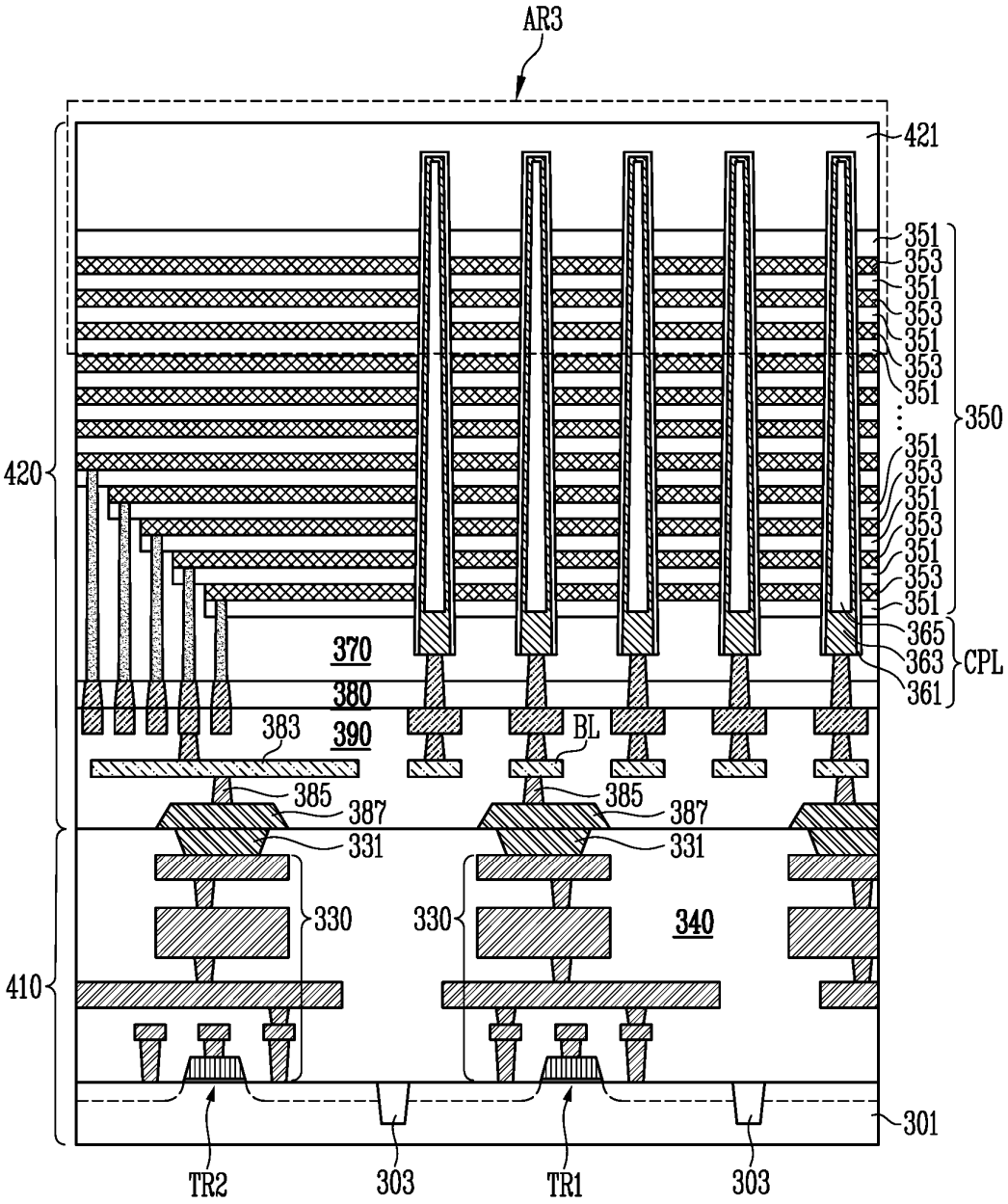

AR3
421
351
353
351
353
351
353
351
350
351
353
351
353
351
353
351
365
363
361
CPL
370
380
390
383
BL
385
387
385
387
331
331
330
330
340
420
410
301
TR2
303
TR1
303

FIG. 11A

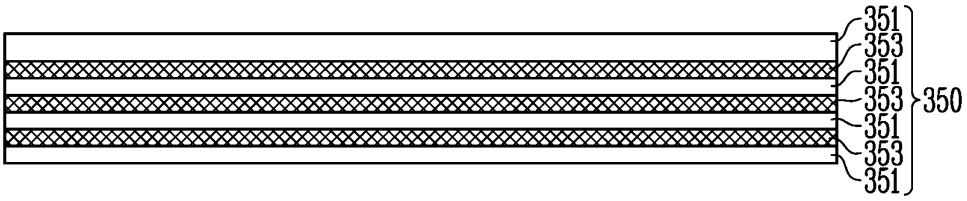


FIG. 11B

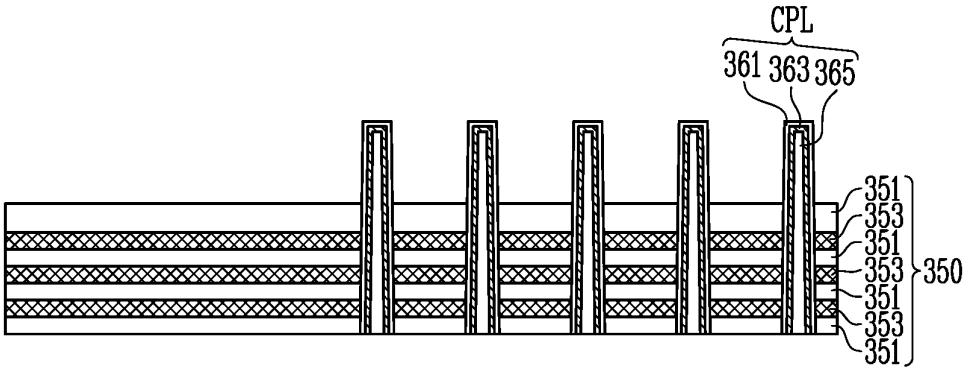


FIG. 12

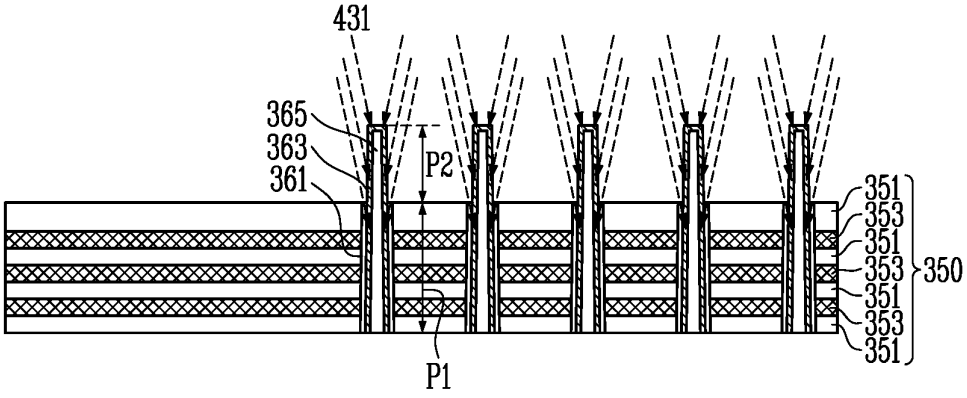


FIG. 13

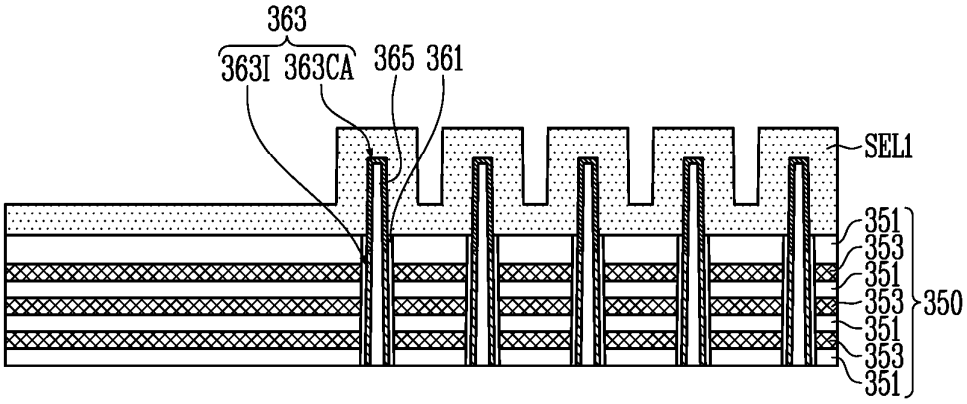

363
363I
363CA
365
361
SEL1
351
353
351
353
351
353
351
350

FIG. 14

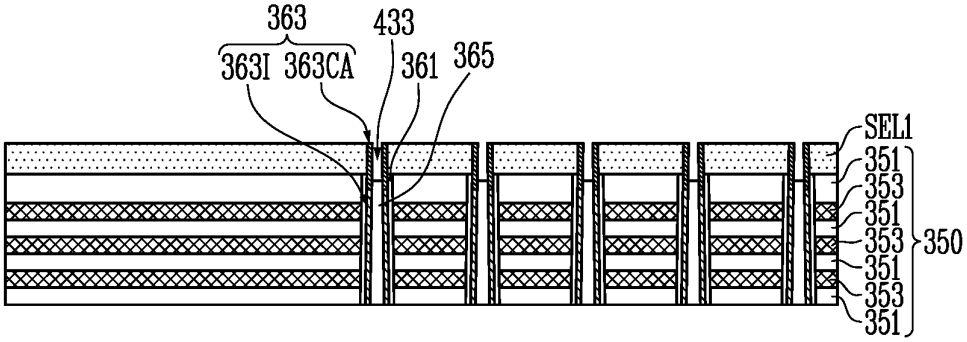

363
363I
363CA
433
361
365
SEL1
351
353
351
353
351
353
351
350

FIG. 15A

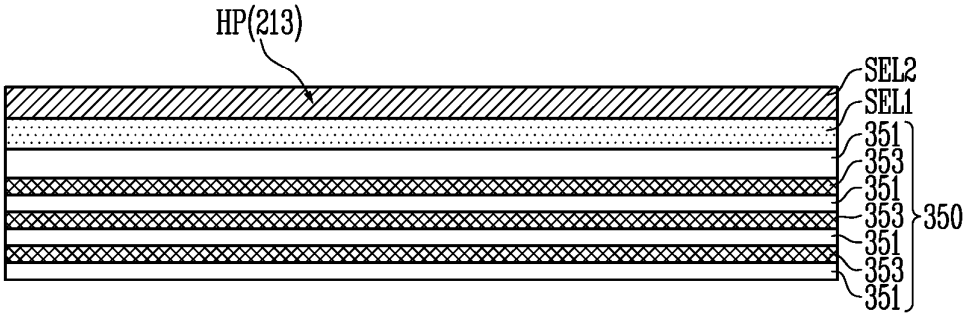


FIG. 15B

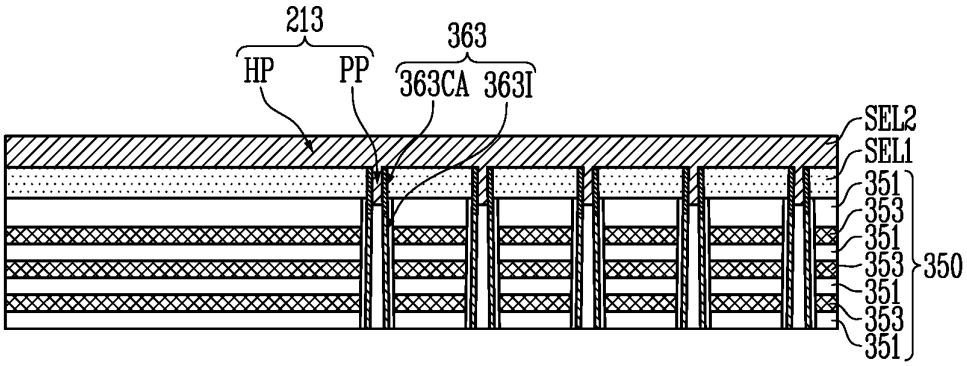


FIG. 16

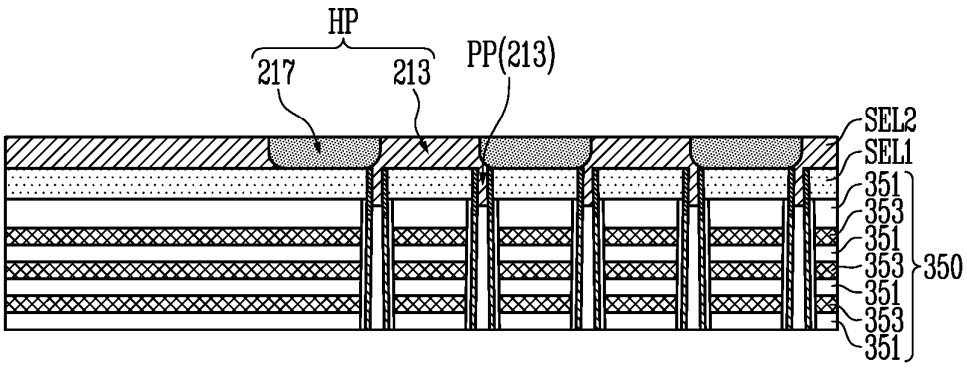

HP
217
213
PP(213)
SEL2
SEL1
351
353
351
353
351
353
351
350

FIG. 17

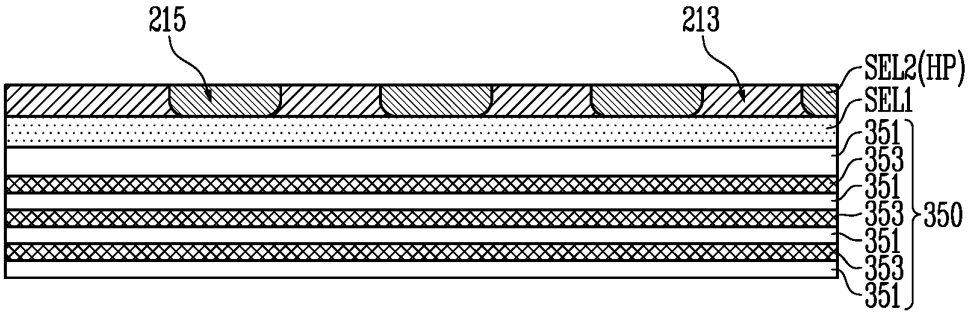

215
213
SEL2(HP)
SEL1
351
353
351
353
351
353
351
350

FIG. 18A

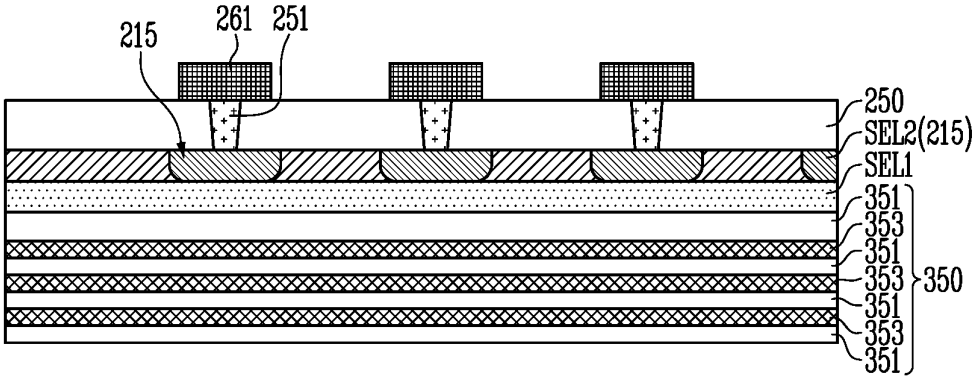


FIG. 18B

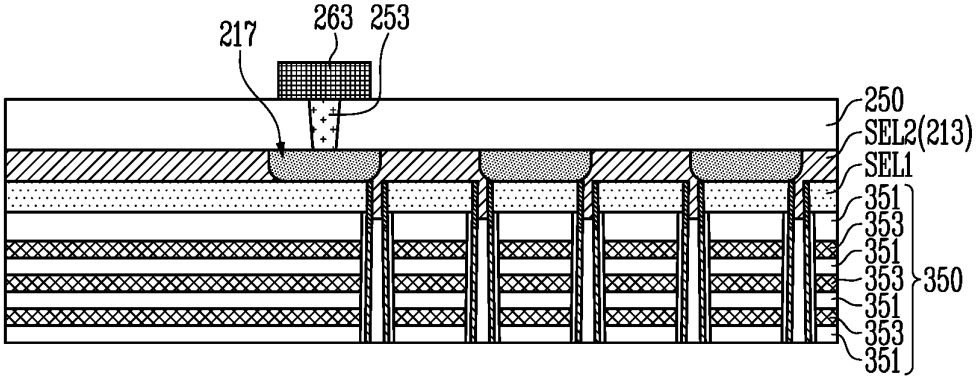


FIG. 19

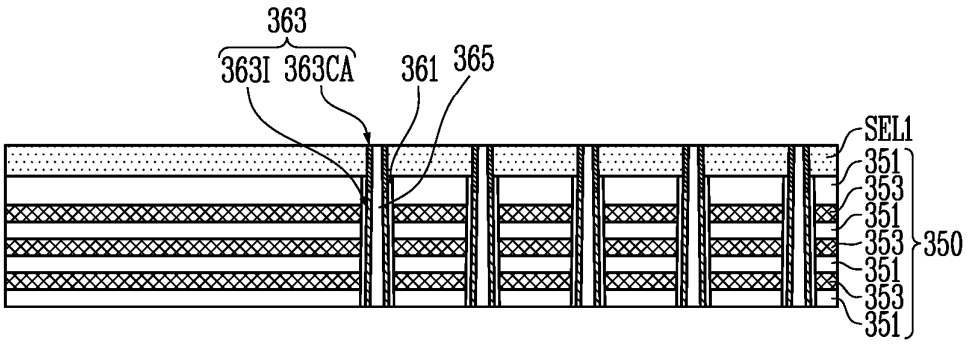

363
363I
363CA
361
365
SEL1
351
353
351
353
351
353
351
350

FIG. 20

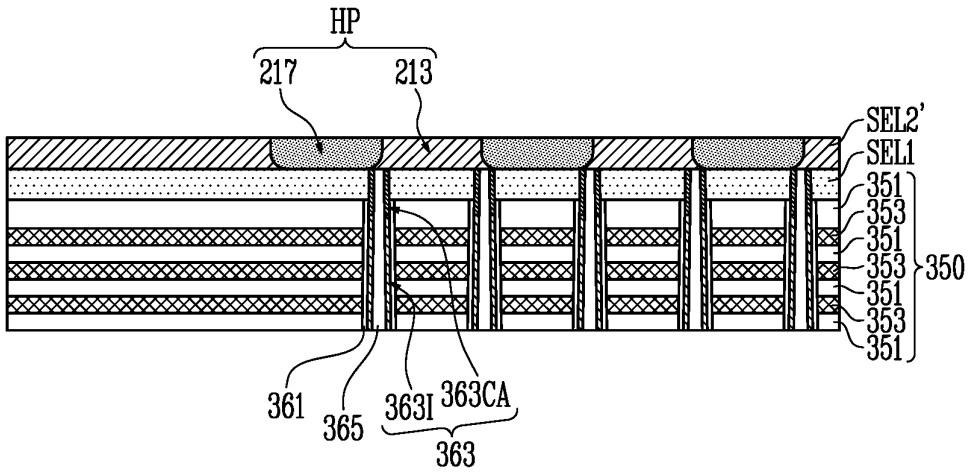

HP
217
213
SEL2'
SEL1
351
353
351
353
351
353
351
350
361
365
363I
363CA
363

FIG. 21

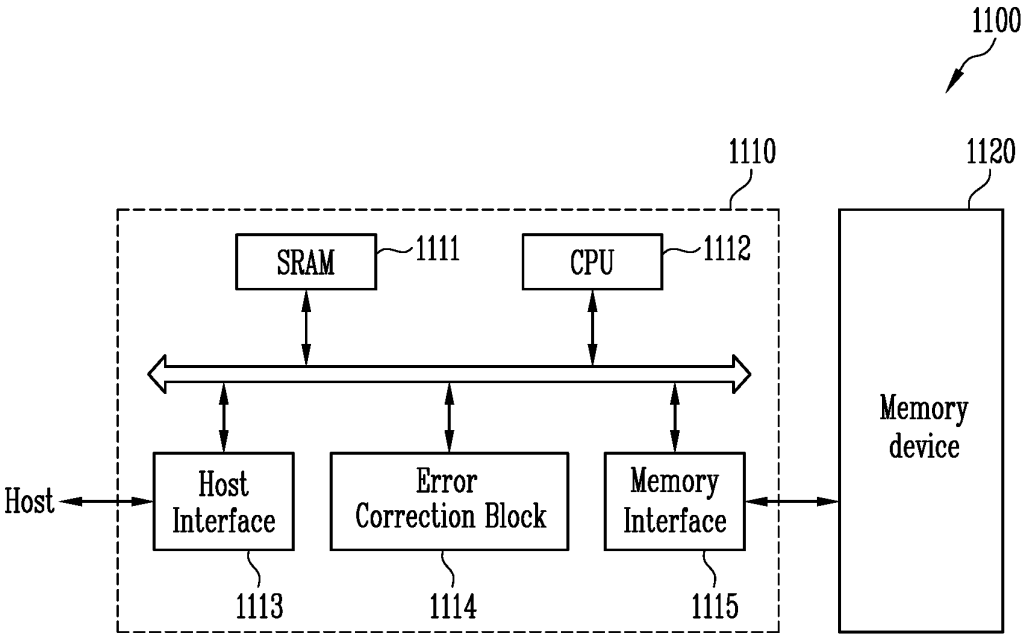
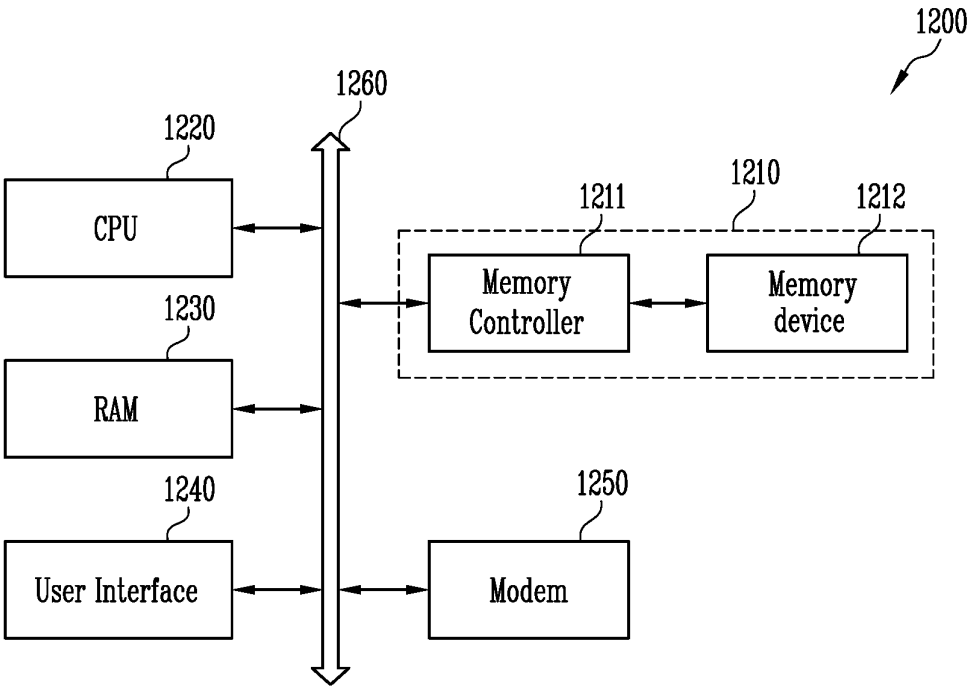

1100
1110
1120
SRAM
1111
CPU
1112
Memory device
Host
Host Interface
Error Correction Block
Memory Interface
1113
1114
1115

FIG. 22


1200
1260
1220
CPU
1210
1211
1212
Memory Controller
Memory device
1230
RAM
1240
1250
User Interface
Modem