Improved process for preparing cleaned surfaces of strained silicon

Field of the Invention

The present invention relates to cleaning layers of strained silicon (sSi) denuded by selective etching of a layer of silicon-germanium (SiGe) in contact with the sSi layer, as used in the fabrication of sSOI (strained silicon on insulator) or SGOI (silicon-germanium (SiGe) on insulator) type wafers.

Background Art

A number of techniques exist for preparing such wafers. One example of one of the most effective current techniques for fabricating sSOI or SGOI type wafers is the production of an active layer of strained silicon (sSi) or relaxed SiGe by transfer thereof onto an insulating support (for example a layer of SiO_2 on a silicon substrate) using the Smart Cut® technique to produce the desired heterostructure. Particular examples of implementations of such fabrication techniques are described in United States patent application US 2004/053477 and International patent application WO 2004/006311.

The finishing step of such wafers involves a selective etching procedure to eliminate the SiGe layer subsisting above the silicon layer after transfer thereof to the "receiver" substrate and detachment from the "donor" substrate. Selective etching is a chemical attack method which can selectively eliminate the upper layer of SiGe without attacking the next layer of strained silicon (sSi). Compositions that have been found to be capable of achieving such a "selective etch" include CH_3COOH / H_2O_2 / HF mixtures.

After the "selective etch" step, which removes the upper layer of SiGe, a cleaning step may appropriately be used in order to reduce particulate contamination and surface defects on the surface of the strained silicon layer following selective etching of the SiGe layer. The cleaning composition must thus be chosen such as to enable cleaning of the sSi surface while avoiding etching of this strained silicon layer.

This post-selective etch cleaning step generally uses compositions containing oxidants, but not containing hydrofluoric acid (HF). A known method, termed "RCA", comprises: a first step of cleaning using an "SC1" (Standard Clean 1) solution (or APM, ammonium hydroxide peroxide mixture) containing NH_4OH, H_2O_2, and deionized water, and a second cleaning step using an "SC2" (Standard Clean 2) solution (or HPM, hydrochloric peroxide mixture) containing HCl, H_2O_2, and deionized water.

An alternative treatment method proposed in United States patent application US 2006/0264008 comprises a step of cleaning the surface of the strained silicon layer with an aqueous ozone solution, rather than using the RCA cleaning procedure, following the step of selective etching of the SiGe layer.

The wafer obtained by the process steps of 1) selective etching of the SiGe layer, and 2) oxidative cleaning, may then be used in subsequent semiconductor device manufacturing processes. Generally, the oxidative cleaning step is followed by a step of rinsing with deionized water.

The wafer with an exposed sSi thus obtained may be used in MOS transistors. Workers in the semiconductor industry are in effect constantly engaged in an effort to reduce the dimensions and increase the speed of operation of integrated circuits. Other parameters being equal, the operation speed of a transistor is increased by increasing the mobility of charge carriers, both electrons and (positive) holes, and one way of achieving this is by the use of strained silicon, wherein silicon, grown on a silicon-germanium surface, is obliged to have more broadly spaced atoms than in pure silicon. A doubling of charge carrier mobility with respect to normal, relaxed silicon can be observed.

Concerning the existing technology in this area, the present inventors have found that the degree of defects as measured by SOD (sum of defects) remains higher than is desirable for the applications envisaged for the wafers obtained.

In addition, the present inventors have observed that the SiGe is not completely removed by prior art processes. Instead, although SiGe is completely removed in certain areas, other zones, in effect "islands", of SiGe persist. It has been observed that these islands may correspond to about 35% of the surface defects measured. Germanium atoms from such islands may diffuse into and contaminate the strained silicon layer. Further, these islands may disturb subsequent fabrication steps, e.g. doping steps.

There therefore remains a need in the art to produce sSi layers showing a minimum amount of surface defects and a minimum amount of residual SiGe. Any further cleaning processes other than prior art processes of 1) selective etching of the SiGe layer, and 2) oxidative cleaning, need however to be chosen so as to minimize consumption of now exposed parts of the sSi layer.

Summary of the invention

The present inventors have now surprisingly found that it is possible to achieve lower surface defects and reduced residual SiGe by a process comprising a second selective etch step, such that rinsing and drying steps are inserted between a first and a second selective etch steps.

The present invention is thus directed in a first aspect to a method of treating wafers comprising at least one surface layer of silicon-germanium (SiGe) and a layer of strained silicon (sSi) in contact with the SiGe layer, the sSi layer being exposed by etching of the SiGe layer, the method comprising the steps of:

(a) a first selective etch of the SiGe layer, optionally followed by an oxidative cleaning step;

(b) a rinsing step using deionized water;

(c) drying; and

(d) a second selective etch step.

The present invention is also directed in a second aspect to a wafer which can in particular be obtained by the method of the present invention.

Detailed Description of the Invention

In one embodiment, in the method according to the present invention, the first selective etch step (a) is carried out with an etching solution comprising a mixture of acetic acid (CH_3COOH), hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF). Generally appropriate process conditions for use with such a selective etch solution during first selective etch step (a) comprise a concentration of hydrofluoric acid (HF) of at least 0.05 % and at most 10 % by weight, about 2 % (1.5% to 2.5%) in a currently preferred embodiment.

In a first currently preferred embodiment, an acetic acid / H_2O_2 / HF mixture is used in proportions of 15/15/1 by volume, corresponding to 49 % : 49 % : 2 % by weight. In a second currently preferred embodiment, an acetic acid / H_2O_2 / HF mixture is used in proportions of 1/1/1 by volume, corresponding to 32 wt% : 50 wt% : 18 wt%.

A generally appropriate temperature during the first selective etch step is at least 20°C and at most 60°C, and a generally appropriate duration of the first selective etch step is at least 20 seconds and at most 500 seconds. In addition, a wafer rotation rate in the range 400 rpm to 2000 rpm may be appropriately used.

In an alternative embodiment according to the present invention, the first selective etch step (a) is carried out using RCA solutions, first an SC1 solution and then an SC2 solution. The present inventors have in effect observed that RCA solutions here may be used for selective etching as well as for oxidative cleaning. This procedure can also be applied for the second selective etch step (d).

In a further alternative embodiment, a mixture of acetic acid / H_2O_2 / HF / H_2SO_4, in relative proportions of 15 / 15 / 1 / 5 by volume, can be used for the first selective etch step (a). Such a mixture can also be used for the second selective etch step (d).

In one embodiment, in the method according to the present invention, the first selective etch step (a) is continued beyond the point at which measurement shows, or theoretical calculations by extrapolation predict, that SiGe has been completely removed from (at least some regions of) the now exposed sSi surface. This phase is referred to as "over-etch" (OE), but does not represent a distinct process step in the sense that the reagents used are the same as in the first selective etch step (a) – the "over-etch" is a continuation beyond the moment of end-point detection (EPD) corresponding to SiGe removal. A reflectometer measuring the intensity of reflected light may be used to detect the end point. Alternatively, if the ability of a given selective etch solution at a certain temperature to remove SiGe, as a thickness removed as a function of time, has been precisely determined by previous experiments, the end-point of the first selective etch step (a), which is the instant in time at which the over-etch starts, can be calculated with a reasonable degree of certainty. An "over-etch", which is optional in the present invention, may help to reduce possible inhomogeneity arising from etching. The duration of the "over-etch" is generally appropriately selected in the range of 0 seconds to at most 60 seconds.

In one embodiment, in the method according to the present invention, an oxidative cleaning step is carried out after the first selective etch step (a), this oxidative cleaning step using a solution of ozone (O_3) dissolved in water in a concentration in the range of 15 ppm to 50 ppm, at a temperature of 17°C to 35°C, for a period of 5 s to 300 s. A currently preferred treatment time for this oxidative cleaning step is about 15 seconds. An appropriate wafer rotation rate for this treatment with ozone lies in the range of 400 rpm to 2000 rpm.

In the case where an oxidative cleaning step is indeed carried out after the first selective etch step (a), for example using ozone, it is believed, though this should not be construed as limiting the invention, that the second selective etching step not only

removes residual "islands" of SiGe, but may also remove possible oxides of Si and Ge present on the sSi surface.

In the framework of the method according to the present invention, the deionized water (DIW) used in rinsing step (b) is of standard quality for use in micro-electronics. A generally appropriate duration of the rinsing step is of at least 5 s and at most 3 minutes. A currently preferred treatment time for this DIW rinsing step is about 15 seconds, at a temperature of 15°C to 60°C. A generally appropriate wafer rotation rate for rinsing step (b) is at least 400 rpm and at most 2000 rpm.

In one embodiment, in the method according to the present invention, the drying of step (c) is carried out using a flow of inert gas such as nitrogen or argon. The purity and pressure conditions of the gas used are appropriately chosen to have the usual parameters used by skilled practitioners in microelectronics. In an appropriate embodiment, nitrogen gas is supplied using a nozzle designed for drying the wafer after rinsing. A currently preferred drying process involves drying the wafer being treated in two scans (passes) using nitrogen gas.

In one embodiment, in the method according to the present invention, the second selective etch step (d) is carried out with an etching solution comprising a mixture of acetic acid (CH_3COOH), hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF). A generally appropriate concentration of hydrofluoric acid (HF) during the second selective etch step (d) is at least 0.05 % and at most 10 % by weight. A generally appropriate temperature during the second selective etch step (d) is at least 20°C and at most 60°C.

Concerning the duration of the second selective etch step (d), the preferred maximum duration is about 40 seconds. A currently preferred range, notably in the context of an etching solution comprising a mixture of acetic acid (CH_3COOH), hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF), is at least 5 seconds and at most 40 seconds. A further currently preferred duration of step (d) in this context is of at least 10 seconds and at most 30 seconds, more preferably at least 15 seconds and at most 25 seconds, and a duration of about 20 seconds has been found to particularly appropriate.

In one embodiment, in the method according to the present invention, the second selective etch step (d) may be directly followed by a rinsing step and then a drying step. Generally appropriate process conditions are those described above for the rinsing step (b) and the drying step (c) that follow the first selective etch step (a).

In one embodiment, in the method according to the present invention, the second selective etch step (d) is followed by a further oxidative cleaning step (e). One

appropriate process choice for this further oxidative cleaning step (e) comprises the use of a solution of ozone (O_3) dissolved in water in a concentration of at least 15 ppm and at most 50 ppm, at a temperature of at least 17°C and at most 35°C, for a period of at least 5 s and at most 300 s.

In the case where a second oxidative cleaning step is indeed carried out after the second selective etch step (d), for example using ozone, it is believed, though this should not be construed as limiting the invention, that the second oxidative cleaning may make the final surface more hydrophilic through surface oxidation and by this means inhibit contamination by particle deposition.

In one embodiment, in the method according to the present invention, the further oxidative cleaning step (e) may be followed by a rinsing step and a drying step. Generally appropriate process conditions are those described above for the rinsing step (b) and the drying step (c) that follow the first selective etch step (a).

The present invention is also directed in a second aspect to a wafer which can in particular be obtained by the method of the present invention.

A wafer according to the present invention preferably comprises at least one surface layer of strained silicon (sSi), said surface layer of sSi having a thickness of at least 5 nanometres and at most 100 nanometres, preferably between 10 nanometres and 30 nanometres, and preferably shows a sum of defects (SOD) value SOD @ 0.40 μm of at most 200 defects per wafer.

The SOD here is as determined as described in US 2006/0264008 with a detection threshold of 0.40 μm. The measurements can for example be made with an SP1-apparatus of KLA-Tencor. The measurement comprises the detection of LPD (small defects) and AP (larger defects). These different groups of defects, distinguished by size, both include topological defects (holes, craters or bumps) as well as particles (dust). SOD is a sum of LPD and AP. It is possible to discern the qualitative kind of the defects by Scanning Electron Microscope measurement, where it has been detected by the present inventors that 95% of the remaining defects (after the second etching step) are topological defects of the surface and 5% are due to particles.

The SOD values observed for wafers according to the present invention represent a considerable improvement over those observed for prior art wafers. The present inventors have namely observed that typical values of SOD @ 0.40 μ after the first, and in the conventional art methods, only selective etch step, are in the region of 4000 defects

per wafer. A reduction of SOD values by a factor of about 15 or 20 times is thus made possible by the present invention.

In a preferred embodiment, wafers according to the present invention have a diameter of about 200 millimetres or about 300 millimetres. In effect, wafers in the micro-electronics field are produced in these standard sizes. The preferred maximum of 200 defects per wafer is appropriate for both 200 mm and 300 mm wafers.

Wafers according to the present invention generally show a surface roughness of at most 1 Å rms for a scanning surface of 2 μm x 2 μm. In appropriate embodiments, the defect density is less than 0.3 particles /cm^2 for a 300 mm wafer (a consequence of the 200 defects limit) and 0.6 particles /cm^2 for the 200mm wafer.

Wafers according to the present invention generally have a strained silicon on insulator (sSOI) structure. The wafers are preferentially obtained by the SmartCut® technology as previously mentioned, whereby the stacking of sSi/SiGe is transferred from a donor substrate to a receptor Si bulk substrate by means of an oxide layer.

Examples

The following table indicates treatment conditions that were tested in the framework of the present invention. The treated wafers were obtained by the Smart Cut® technique for fabricating sSOI or SGOI type wafers, as described for example in United States patent application US 2004/053477. Wafers used were silicon bulk wafers for microelectronics use, available on the market as "silicon of microelectronic quality" with 200mm or 300mm diameter which today are the two standard sizes.

Step	Process details	Example 1	Ex.2	Ex. 3	Comparative Ex.1
Wafer diameter / mm		300	200	300	300
(a) First selective etch	Reagent identities and concentrations:	Acetic Acid / H_2O_2 / HF: (15/15/1 by volume, i.e. 49: 49:2 % by weight)	(As Ex. 1)	Acetic Acid / H_2O_2 / HF: 1/1/1 by vol. = 32:50:18 % by wt.	(As Ex. 1)
	Temperature:	25°C	25°C	30°C	26°C
	Time:	300 s	260 s	500 s	260 s
Over etch	Time:	30 s	30 s	30 s	30 s
Oxidative cleaning step	Reagent identities and concentrations:	O_3 25 ppm in DIW	(As Ex. 1)	(As Ex. 1)	(As Ex. 1)
	Temperature:	17°C	25°C	30°C	(As Ex. 1)
	Time:	20 s	25 s	100 s	(As Ex. 1)
(b) Rinsing using deionized water (DIW)	Temperature:	25°C	20°C	50°C	20°C
	Time:	10 s	20 s	100 s	10 s
(c) Drying	Drying gas	N_2	N_2	N_2	-
	Wafer rotation speed	1500 rpm	1600 rpm	2000 rpm	-
	Flow rate	20 litre/min	20 litre/min	20 litre/min	-
	Number of passes	2	2	2	-
(d) Second selective etch	Reagent identities and concentrations:	Acetic Acid / H_2O_2 / HF: (15/15/1 by volume)	(As Ex. 1)	Acetic Acid / H_2O_2 / HF: 1/1/1 by vol.)	(As Ex. 1)
	Temperature:	25°C	25°C	30°C	26°C
	Time:	20 s	10 s	25 s	10 s
(e) Post-second selective etch further oxidative cleaning step	Reagent identities and concentrations:	Same as first oxidative cleaning step in Ex.1 above, before step (b)	Same as first oxidative cleaning step in Ex.2	Same as first oxidative cleaning step in Ex.3	O_3 25 ppm in DIW
	Temperature:				20°C
	Time:				20°C
Post-second selective etch rinsing using DIW	Temperature:	25°C	20°C	50°C	20°C
	Time:	20 s	30 s	110 s	10 s
Post-second selective etch drying	Drying gas	Same conditions as in first drying step (c) in Ex.1 above	Same conditions as in first drying step (c) in Ex.2 above	Same conditions as in first drying step (c) in Ex.3 above	N_2
	Wafer rotation speed				1000 rpm
	Flow rate				20 litre/min
	Number of passes				2
Results	SOD values	150	200	250	3500

CLAIMS

1. A method of treating wafers comprising at least one surface layer of silicon-germanium (SiGe) and a layer of strained silicon (sSi) in contact with the SiGe layer, the sSi layer being exposed by etching of the SiGe layer, the method comprising the steps of:

(a) a first selective etch of the SiGe layer, optionally followed by an oxidative cleaning step;

(b) a rinsing step using deionized water;

(c) drying; and

(d) a second selective etch step.

2. A method according to claim 1, wherein the first selective etch step (a) is carried out with an etching solution comprising a mixture of acetic acid (CH_3COOH), hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF).

3. A method according to claim 2, wherein the concentration of hydrofluoric acid (HF) during the first selective etch step (a) is at least 0.05 % and at most 10 % by weight, the temperature during the first selective etch step (a) is at least 20°C and at most 60°C, and the duration of the first selective etch step (a) is at least 20 seconds and at most 500 seconds.

4. A method according to any of claims 1 to 3, wherein an oxidative cleaning step is carried out after the first selective etch step (a) using a solution of ozone (O_3) dissolved in water in a concentration of at least 15 ppm and at most 50 ppm, at a temperature of at least 17°C and at most 35°C, for a period of at least 5 s and at most 300 s.

5. A method according to any of claims 1 to 4, wherein the step (b) of rinsing with deionised water is carried out for a duration of at least 5 s and at most 3 minutes, at a temperature of 15°C to 60°C.

6. A method according to any of claims 1 to 4, wherein the drying of step (c) is carried out using a flow of inert gas such as nitrogen or argon.

7. A method according to any of claims 1 to 5, wherein the second selective etch step (d) is carried out with an etching solution comprising a mixture of acetic acid (CH_3COOH), hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF).

8. A method according to claim 7, wherein the concentration of hydrofluoric acid (HF) during the second selective etch step (d) is at least 0.05 % and at most 10 % by weight, the temperature during the second selective etch step (d) is at least 20°C and at most 60°C, and the duration of the second selective etch step (d) is at least 5 seconds and at most 40 seconds.

9. A method according to claim 7 or claim 8, in which the duration of the second selective etch step (d) is at least 10 seconds and at most 30 seconds.

10. A method according to claim 9, in which the duration of the second selective etch step (d) is at least 15 seconds and at most 25 seconds.

11. A method according to claim 10, in which the duration of the second selective etch step (d) is about 20 seconds.

12. A method according to any of claims 1 to 11, wherein the second selective etch step (d) is followed by a rinsing step and a drying step.

13. A method according to any of claims 1 to 11, wherein the second selective etch step (d) is followed by a further oxidative cleaning step (e).

14. A method according to claim 13, wherein the oxidative cleaning step (e) that follows the second selective etch step (d) is carried out using a solution of ozone (O_3) dissolved in water in a concentration of at least 15 ppm and at most 50 ppm, at a temperature of at least 17°C and at most 35°C, for a period of at least 5 s and at most 300 s.

15. A method according to claim 13 or claim 14, wherein the further oxidation step (e) is followed by a rinsing step and a drying step.

16. A wafer comprising at least one surface layer of strained silicon (sSi), said surface layer of sSi having a thickness of at least 5 nanometres and at most 100 nanometres, and a sum of defects (SOD) value SOD @ 0.40 μm of at most 200 defects per wafer.

17. A wafer according to claim 16, wherein the wafer has a diameter of about 200 millimetres or about 300 millimetres.

18. A wafer according to claim 16 or claim 17, wherein the wafer comprises a strained silicon on insulator (sSOI) structure.