

YUV VIDEO LINE DOUBLER

RCA 87,458

Doubling the number of lines, resulting in 32kHz horizontal deflection, effectively reduces the visibility of the line structure of a television picture.

The most costly parts of a line doubler are the A-to-D converters and the line memories. Fig.1 shows the block diagram of a line doubler for Y, U and V signals, embodying an inventive feature. The Y signal path is the same as an R, G or B channel.

The U and V channel uses a single A-to-D converter and a single line memory. This is achieved by multiplexing the U and V signals. Effectively the U and V signals are sampled at half the clock frequency, thus halving the bandwidth of the signal path. However, the U and V signals have a bandwidth of approximately a quarter of the bandwidth of the Y signal. The same clock signal is used for converting the Y and the multiplexed U and V signals, so that the latter are still over sampled, maintaining full bandwidth. Consecutive output samples of the converter are alternately U and V signals that are stored in the memory. At the output of the memory the data rate of U and V has doubled. U and V are demultiplexed in the digital domain rather than in the analog domain. The expense of a digital demultiplexer and a D-to-A converter, and the cost of an analog demultiplexer might well break

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even. Further, a triple D-to-A converter and a clock generator/controller are required. At the input of the A-to-D converters the signals have to be clamped to defined dc levels to avoid

signal clipping. In carrying out an inventive feature, for the U and V signals a single clamp switch could be used for both, as shown in Fig. 1.

Digital video processing requires the use of a clock signal that is locked to horizontal line frequency. For this purpose a phase locked clock generator has been used operating at 27MHz. It consists of a voltage controlled oscillator and means to compare the phase of horizontal or composite sync (CSI) and the clock signal (CLK). Since the frequencies of these are different, a divider (counter) circuit is used to make them equal. The output of the phase comparator is connected to the VCO via a low pass filter that reduces sensitivity to noise and other phase disturbances in the reference signal.

The counter and phase comparator are realized in a programmable logic device (PLD) of Fig. 4 and are functionally as shown in Fig. 2.

An 11 bit counter divides the frequency of 27MHz down to the horizontal line frequency, of 15625Hz. The duty

cycle of the most significant bit (Q10) of the counter output is about 2:1. Fig.2 also shows some waveforms of the circuit in the situation where a small phase difference is present between the input phase reference signal CSI and counter output Q10. The down going edges of composite sync signal CSI trigger, via an inverter, flipflop FF, that has output signal SYN. This flipflop is reset at the instant that counter output Q10 goes high. Since the low-to-high ratio of Q10 is 2:1, the presence



of equalising pulses in CSI, shown with broken line, will not have any influence on the output signal of the flipflop. Some combinational logic drives enable ENA of a tristate buffer connected to Q10. ENA will be active when SYN and Q10 have the same logical level. As shown in Fig.2 the circuit will output high level pulses when the phase of the sync input is advanced to Q10 and low level output pulses when the phase of SYN is lagging. High level output pulses will cause the VCO to increase its frequency, low level pulses the opposite. In this manner the oscillator will automatically adjust its frequency for minimal phase errors. In the absence of errors ENA will not be active at all. When no input sync is present CSI will be continuously high. Flipflop FF will stay in reset position and ENA will never be active, so that the oscillator will be operating at its nominal free running frequency.

The practical circuit is shown in Fig. 3. The doubling procedure is conventional. For the analog multiplexer U1 a quad analog switch with type number DG601 (Siliconix) is used. For each channel two switches are connected in parallel alternately turned on via EXOR gates U2A and U2B. The clamp switches are incorporated in the A-to-D converters. The Y signal is clamped to ground level and U and V are clamped to a level adjusted by



potentiometer R11. Demultiplexing is carried out by latches U10 and U11. They latch, respectively, the odd and the even samples that are output from the line memory. The reference voltage is present across capacitor C5.

The VCO is built up with inverter U6A and peripheral components. Vari-cap D1 allows the frequency to be varied. R24, R25, C22 and C23 represent the lowpass filter. The counter and phase comparator are implemented in PLD U7. All internal signals of the counter are phase locked to horizontal sync. Therefore all control signals for the memories, the multiplexing and the clamping can be output of the same device (U7).

The double rate horizontal sync signal is advantageously taken from the double rate Y signal. This provides a sync signal that has a fixed phase relationship to the video signals. Any phase jitter of the clock generator has minimum influence in this way.

The described circuit performs well with minimum visible defects. It uses readily available components and does not require microprocessor support. Compared to an RGB video line doubler a YUV doubler is of lower cost. However, a matrix for double rate video has to be provided. Since these are available in integrated circuits, that also incorporate contrast and brightness controls, this should not be a disadvantage.

Claims

1. A phase-lock-loop circuit, comprising:
 a controllable oscillator (53);
 a source of a synchronizing signal (Q4);
 a flip-flop (62) responsive to said synchronizing signal for generating a flip-flop output signal (SYN) at a first state when an edge (LE1/LE2) of said synchronizing signal occurs, said output signal alternating between said first state and a second state (H/L); characterized by

a decoder (101a) for applying said synchronizing signal to an output of said decoder (66c) via a signal path of said synchronizing signal that includes said flip-flop to generate a phase difference indicative signal (OUT) at said output of said decoder, said phase difference indicative signal being generated in accordance with a phase difference between said synchronizing signal and an output signal of said oscillator (CLK), such that for phase

differences that are both positive and negative, no other flip-flop is included in any signal path of said synchronizing signal between said source of synchronizing signal and said output of said decoder; and

a low-pass filter (54) responsive to said phase difference indicative signal and coupled to a control input (53a) of said oscillator for controlling said oscillator in a phase-lock-loop manner such that in steady state phase-lock operation, an edge (CE) of said oscillator output signal is aligned with said edge of said synchronizing signal.

2. An apparatus according to Claim 1 further characterized by, a counter (52) responsive to said oscillator output signal (CLK) for frequency dividing said oscillator output signal, said counter being coupled to said decoder (101a) for providing timing information of said edge (CLK) of said oscillator output signal.

3. An apparatus according to Claim 2 characterized in that said counter (52) is coupled to said flip-flop (62) for generating said flip-flop output signal at said second state (SYN=LOW).



- 30 4. A phase-lock-loop circuit according to Claim 3 characterized in that said counter (52) produces a first signal (ClkDiv) and wherein a pulse width of a pulse of said phase difference indicative signal (OUT) is determined in accordance with a length of an interval between an instant (LEt) when said flip-flop output signal (SYN) assumes said first state (SYN=HIGH) in response to said synchronizing signal (CSI) and an instant (TT1) when said first signal occurs.
- 40 5. A phase-lock-loop circuit according to Claim 4 characterized in that said counter (52) generates a second signal (CLEAR) that is time-shifted with respect to said first signal (ClkDiv), wherein said synchronizing signal (CSI) is derived from a video signal (VIDEO IN) and includes a horizontal rate signal and an equalizing pulse (EQ) between a given pair of pulses (CSI) of said horizontal rate signal and wherein in a given period of said horizontal rate signal said second signal causes said flip-flop (62) to assume said second state following the occurrence of said equalizing pulse in a manner to prevent said equalizing pulse from affecting said phase difference indicative signal (OUT).
- 45 50 55 6. A phase-lock-loop circuit according to Claim 1 characterized in that a pulse of said phase difference indicative signal (OUT) is at a first magnitude (HIGH) when said phase difference is positive and at a second magnitude (LOW) when said phase difference is negative.
7. A phase-lock-loop circuit according to Claim 1 further characterized by, a counter (52) responsive to said oscillator output signal (CLK) for generating a first signal (ClkDiv) at a lower frequency wherein said decoder (101a) includes a tri-state gate (86) that couples said first signal of said counter to an output terminal (86c) of said gate to develop a pulse of said phase error indicative signal (OUT) at said output terminal.



8. A phase-lock-loop circuit according to Claim 1 further characterized by, a counter (52) responsive to said oscillator output signal (CLK) for generating a first signal (ClkDiv) that is coupled to said decoder (101a) wherein when said synchronizing signal (CSi) phase-leads said first signal, a pulse of said phase difference indicative signal (OUT) has a leading edge in response to said flip-flop output signal (SYN) and a trailing edge in response to the occurrence of said first signal (TT1), and when said synchronizing signal phase-lags said first signal, said pulse has a leading edge (TT2) in response to the occurrence of said first signal and a trailing edge in response to said flip-flop output signal.
9. A phase-lock-loop circuit according to Claim 8 characterized in that said counter (52) generates a second signal (CLEAR) that is time-shifted with respect to said first signal for initializing said flip-flop (62) and for causing it to assume said second state (SYN=LOW) in a given period of said synchronizing signal (CSi).
10. A phase-lock-loop circuit according to Claim 8 characterized in that said flip-flop (62) is the only memory stage in any signal path between said counter (52) and said output (66c) of said decoder.
11. A phase-lock-loop circuit according to Claim 1 characterized in that said synchronizing signal (CSi) is coupled to said decoder (101a) in a manner that bypasses said flip-flop (via 67) for enabling the generation of said phase error indicative signal (OUT) in normal operation and for disabling the generation of said phase error indicative signal when said synchronizing signal is missing.
12. A phase-lock-loop circuit, comprising:
a controllable oscillator (53) for generating

an oscillatory signal (CLK);

a counter (52) responsive to said oscillatory signal for frequency dividing said oscillatory signal to generate first (ClkDiv) and second (CLEAR) signals having a time difference therebetween and that are synchronized to said oscillatory signal, each having a lower frequency than that of said oscillatory signal;

a source of a synchronizing signal (CSI); characterized by

an edge triggered flip-flop (62) responsive to said synchronizing signal for generating a flip-flop output signal (SYN) at a first state (HIGH) in accordance with a transition of said synchronizing signal, said first state being generated when a phase difference between said synchronizing signal and said first signal is positive and when said phase difference is negative, said flip-flop being responsive to said second signal for generating said flip-flop output signal at a second state (LOW) in accordance with said second signal, said flip-flop output signal alternating between said first and second states within a given period of said synchronizing signal;

a decoder (101a) for generating a signal (OUT) that is indicative of said phase difference at a first state (HIGH), when said flip-flop output signal is at said first state and said first signal (ClkDiv) is at a first state (HIGH), for generating said decoder output signal at a second state (LOW), when said flip-flop output signal is at said second state (LOW) and said first signal is at a second state (LOW) and for generating said decoder output signal at a third state (TRI-STATE) during the remainder of a given period of said synchronizing signal; and

a low-pass filter (54) responsive to said phase difference indicative signal and coupled to a control input (53a) of said oscillator for controlling said oscillator in a phase-lock-loop manner.

13. A phase-lock-loop circuit according to Claim 12 characterized in that both when said phase difference is positive and negative, only one (FALLING EDGE) of a rising edge and a falling edge of a given pulse of said synchronizing signal (CSI) affects said phase difference indicative signal (OUT) and only one (FALLING EDGE) of a rising edge and a falling edge of a given pulse of said first signal (ClkDiv) affects said phase difference indicative signal.

14. A phase-lock-loop according to Claim 13 characterized in that said edges of said synchronizing (CSI) and first (ClkDiv) signals are aligned in steady state phase-lock operation.



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15. A phase-lock-loop circuit, comprising:
- a controllable oscillator (53) for generating an oscillator output signal (CLK);
 - means (52) responsive to said oscillator output signal for frequency dividing said oscillator output signal to generate a first signal (ClkDiv) at a lower frequency than that of said oscillator output signal and that is synchronized thereto;
 - a source of a synchronizing signal (CSI) containing pulses;
 - an edge triggered flip-flop (62) responsive to said synchronizing signal for generating a flip-flop output signal (SYN) at a first state (HIGH) in accordance with an edge (LE1) of said synchronizing signal, said first state being generated when a phase difference between said synchronizing signal and said first signal is positive and when said phase difference is negative, said flip-flop output alternating between said first state and a second state (LOW); characterized by
 - a decoder (101a) responsive to said flip-flop output signal and to said first signal for generating at an output of said decoder (66c) a decoder output signal (OUT) that is indicative of said phase difference and that is independent of a duty cycle of said synchronizing signal, said decoder output signal being generated in accordance with a difference between a time (LE1) when said first state of said flip-flop output signal occurs and a time (TT1) when said first signal occurs, such that for positive and negative phase differences, no flip-flop other than said flip-flop is used to incorporate timing information from said synchronizing signal into phase difference information of said decoder output signal; and
 - a low-pass filter (54) responsive to said phase difference indicative signal and coupled to a control input (53a) of said oscillator for controlling said oscillator in a phase-lock-loop manner.

16. A phase-lock-loop circuit according to Claim 15 characterized in that in steady state phase-lock operation, an edge (CE) of said oscillator output signal (CLK) is aligned to occur substantially simultaneously with an edge (LE1) of said synchronizing signal.
17. A phase-lock-loop circuit according to Claim 15 characterized in that said first signal generating means (52) comprises a counter (52) responsive to said oscillator output signal (CLK) for frequency dividing said oscillator output signal, said counter being coupled to said decoder (101a) for providing timing information



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of said edge (CE) of said oscillator output signal.

18. A phase-lock-loop circuit according to Claim 17 characterized in that said counter (52) is coupled to said flip-flop (62) for generating said flip-flop output signal (SYN) at said second state (LOW).

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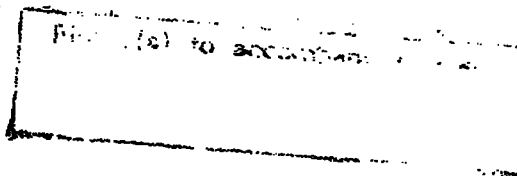
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ABSTRACT

A line-locked-clock generator circuit includes an oscillator, a counter with a 2:1 ratio output pulse connected to a tristate buffer, a reference input for providing composite sync and a control circuit. The clock generator is coupled to a line memory. Video component signals U and V are clamped using a single clamp arrangement. The clamped signal is processed through an analog-to-digital converter and applied to the line memory.

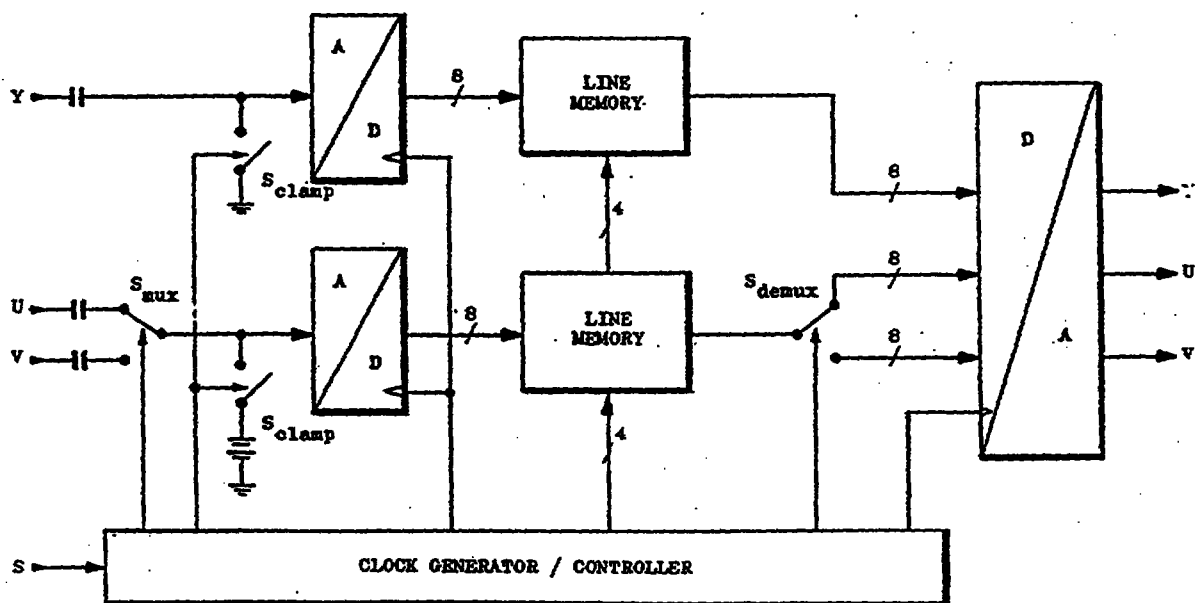


FIG.1 BLOCK DIAGRAM

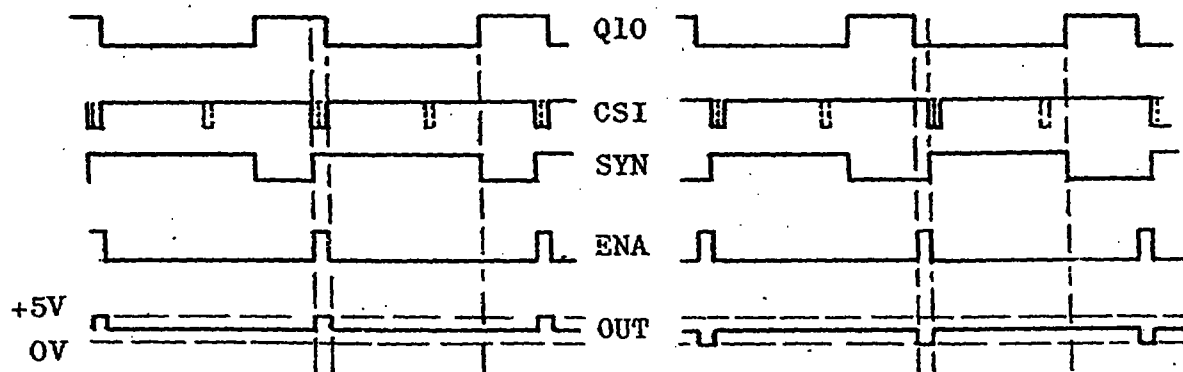
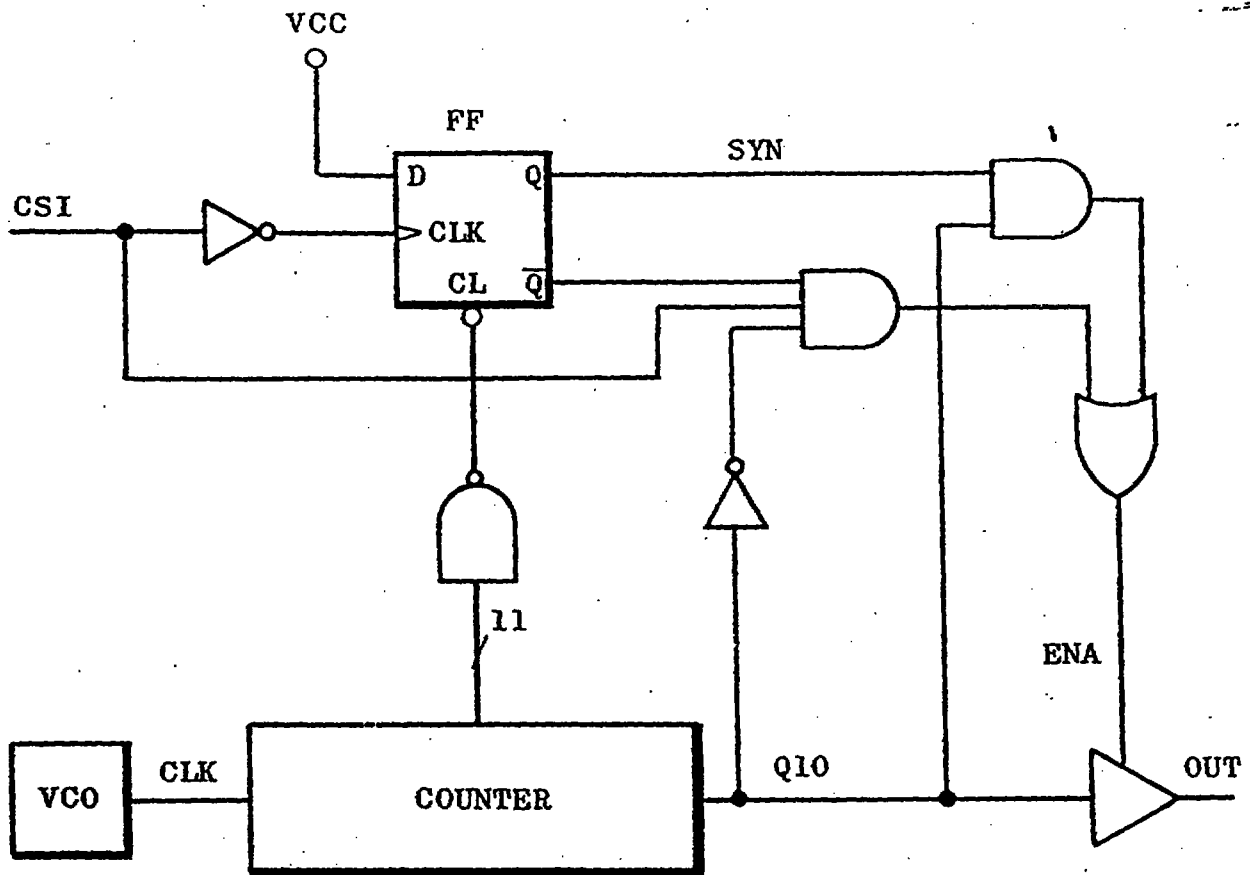
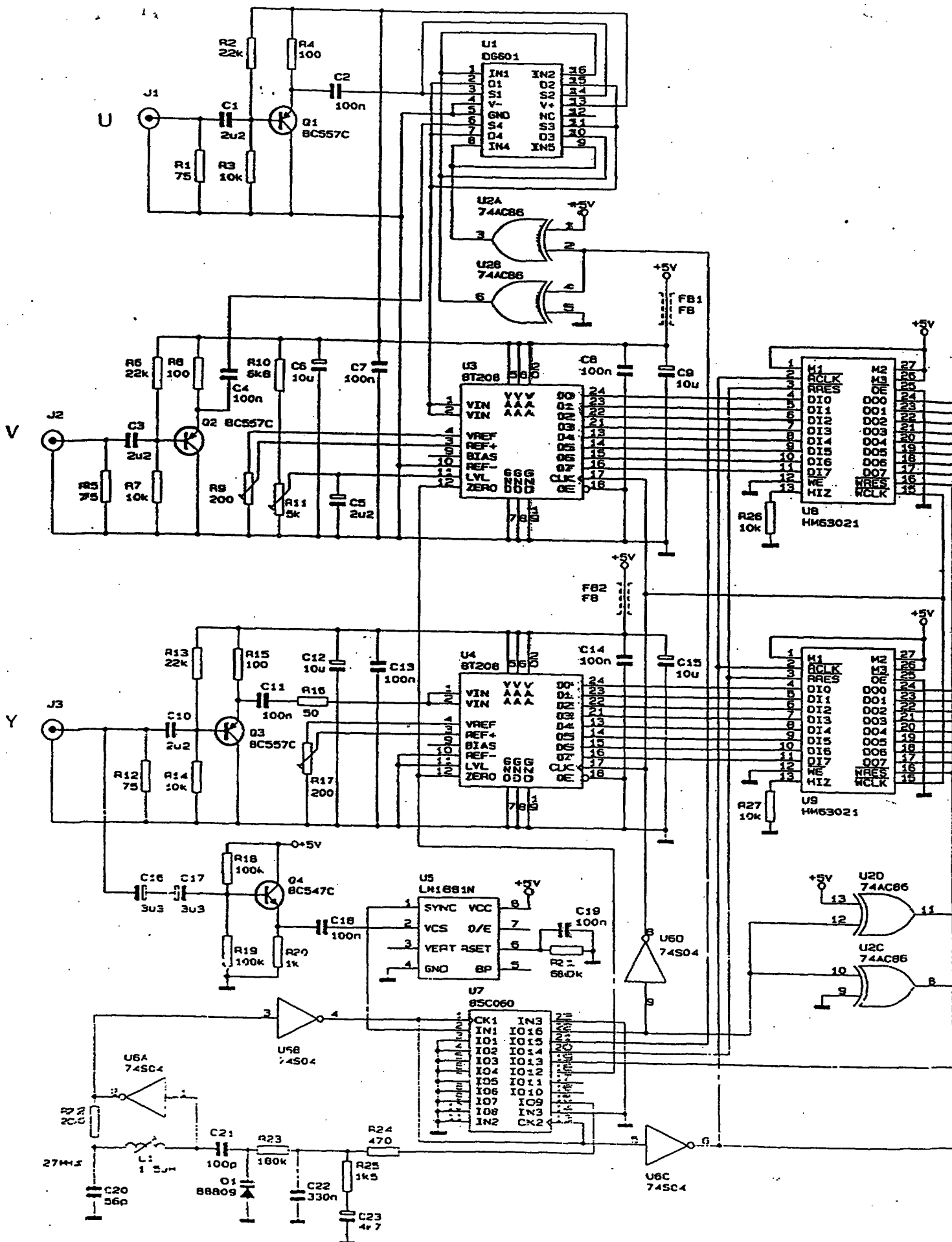


FIG.2 COUNTER / PHASE COMPARATOR



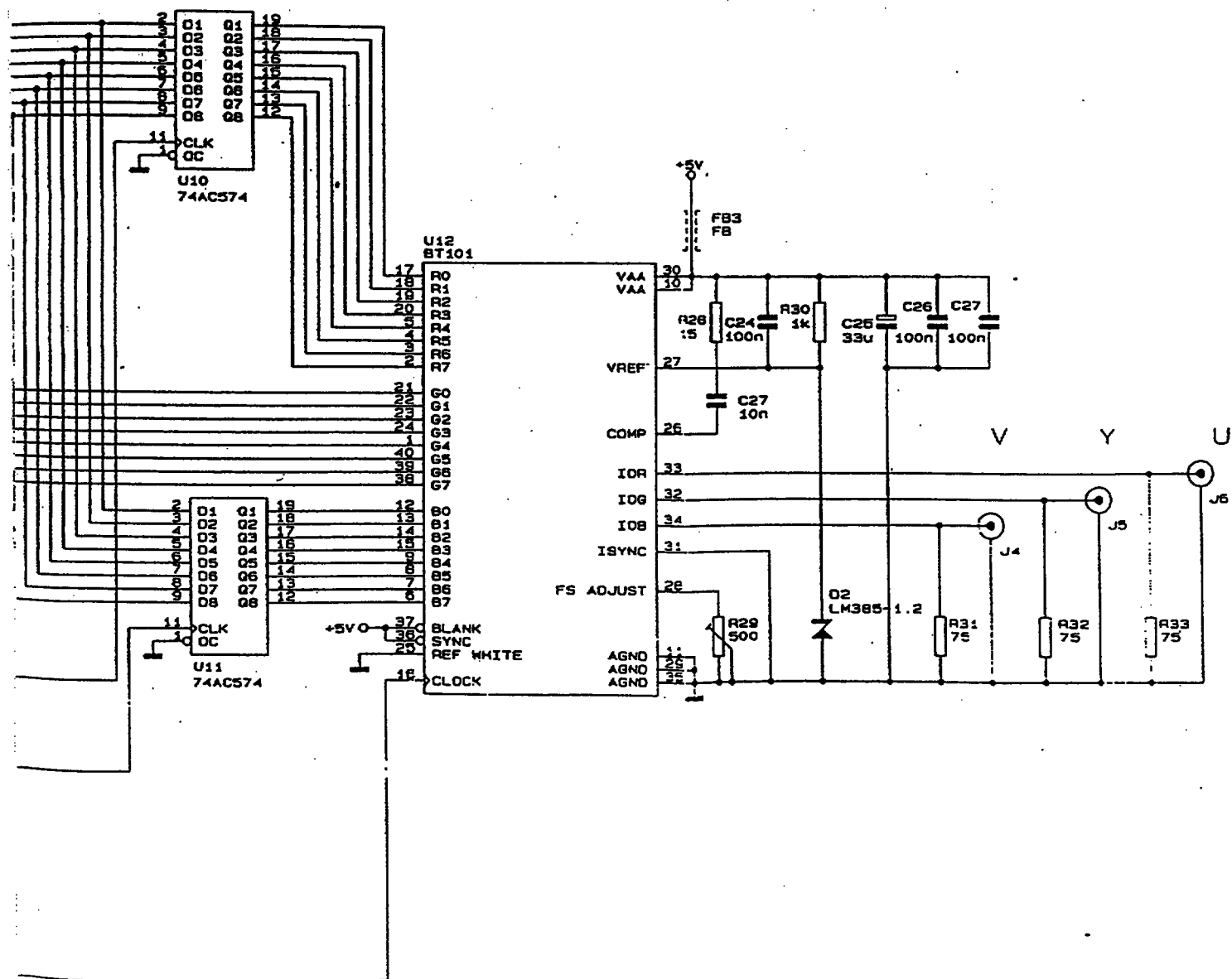


FIG.3 YUV VIDEO LINE DOUBLER

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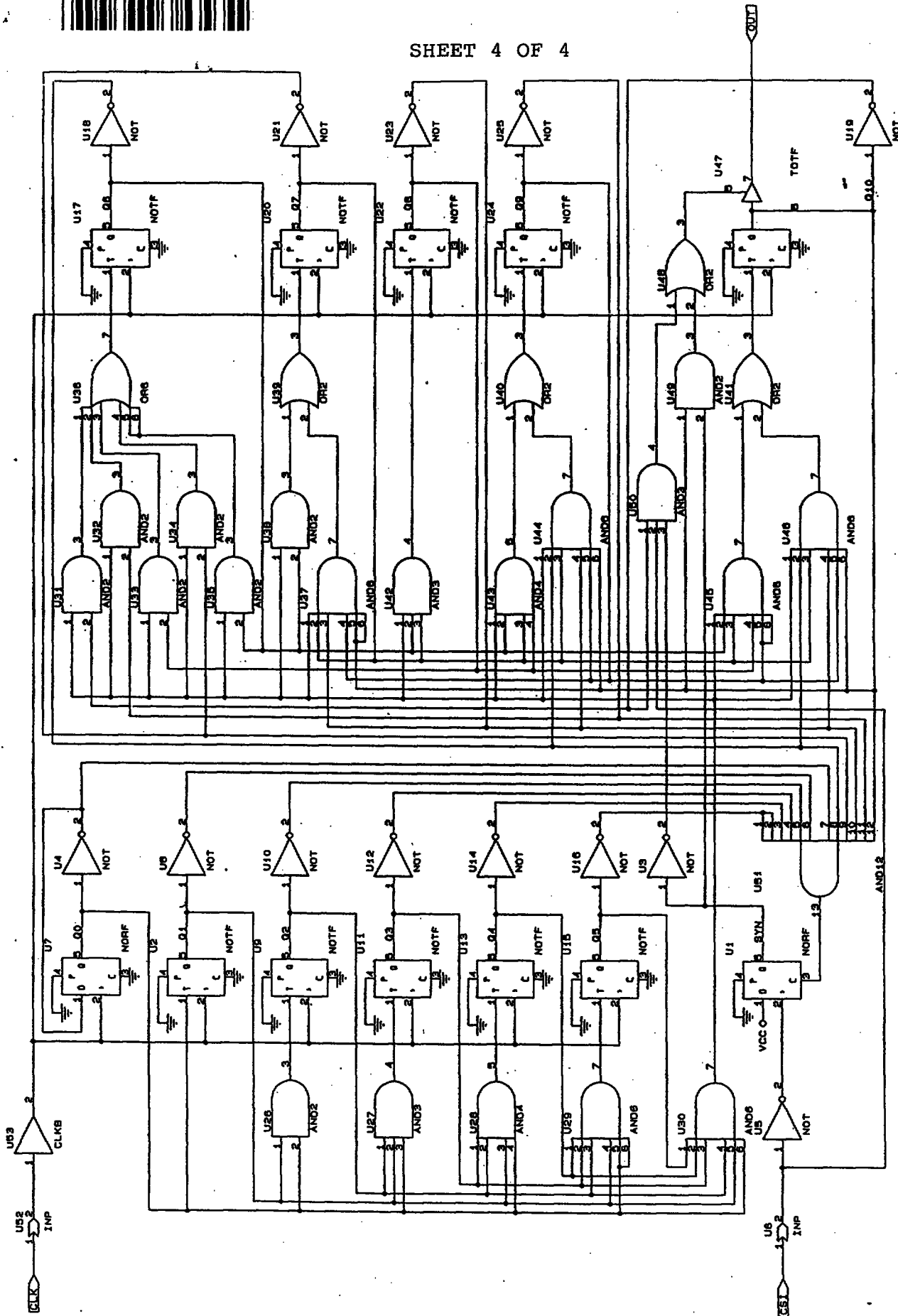


Fig.4 Internal Circuit of Programmable Logic Device

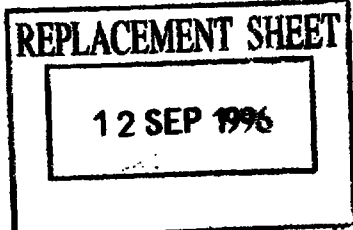
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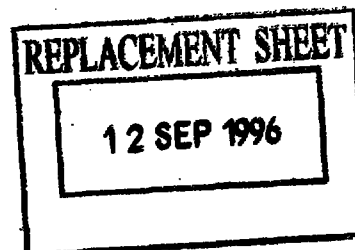
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even. Further, a triple D-to-A converter and a clock generator/controller are required. At the input of the A-to-D converters the signals have to be clamped to defined dc levels to avoid signal clipping. In carrying out an inventive feature, for the U and V signals a single clamp switch could be used for both, as shown in Fig. 1.

Digital video processing requires the use of a clock signal that is locked to horizontal line frequency. For this purpose a phase locked clock generator has been used operating at 27MHz. It consists of a voltage controlled oscillator and means to compare the phase of horizontal or composite sync (CSI) and the clock signal (CLK). Since the frequencies of these are different, a divider (counter) circuit is used to make them equal. The output of the phase comparator is connected to the VCO via a low pass filter that reduces sensitivity to noise and other phase disturbances in the reference signal.

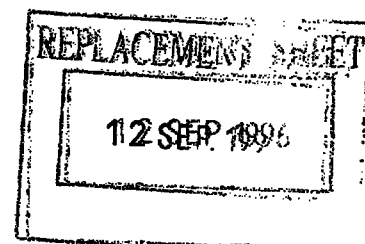
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cycle of the most significant bit (Q10) of the counter output is about 2:1. Fig.2 also shows some waveforms of the circuit in the situation where a small phase difference is present between the input phase reference signal CSI and counter output Q10. The down going edges of composite sync signal CSI trigger, via an inverter, flipflop FF, that has output signal SYN. This flip-flop is reset at the instant that counter output Q10 goes high. Since the low-to-high ratio of Q10 is 2:1, the presence



of equalising pulses in CSI, shown with broken line, will not have any influence on the output signal of the flipflop. Some combinational logic drives enable ENA of a tristate buffer connected to Q10. ENA will be active when SYN and Q10 have the same logical level. As shown in Fig.2 the circuit will output high level pulses when the phase of the sync input is advanced to Q10 and low level output pulses when the phase of SYN is lagging. High level output pulses will cause the VCO to increase its frequency, low level pulses the opposite. In this manner the oscillator will automatically adjust its frequency for minimal phase errors. In the absence of errors ENA will not be active at all. When no input sync is present CSI will be continuously high. Flipflop FF will stay in reset position and ENA will never be active, so that the oscillator will be operating at its nominal free running frequency.

The practical circuit is shown in Fig. 3. The doubling procedure is conventional. For the analog multiplexer U1 a quad analog switch with type number DG601 (Siliconix) is used. For each channel two switches are connected in parallel alternately turned on via EXOR gates U2A and U2B. The clamp switches are incorporated in the A-to-D converters. The Y signal is clamped to ground level and U and V are clamped to a level adjusted by

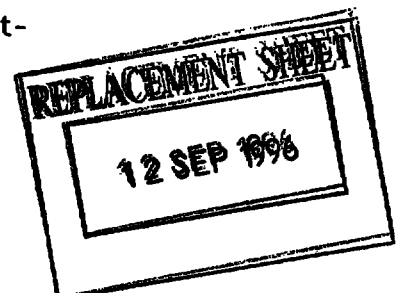


potentiometer R11. Demultiplexing is carried out by latches U10 and U11. They latch, respectively, the odd and the even samples that are output from the line memory. The reference voltage is present across capacitor C5.

The VCO is built up with inverter U6A and peripheral components. Vari-cap D1 allows the frequency to be varied. R24, R25, C22 and C23 represent the lowpass filter. The counter and phase comparator are implemented in PLD U7. All internal signals of the counter are phase locked to horizontal sync. Therefore all control signals for the memories, the multiplexing and the clamping can be output of the same device (U7).

The double rate horizontal sync signal is advantageously taken from the double rate Y signal. This provides a sync signal that has a fixed phase relationship to the video signals. Any phase jitter of the clock generator has minimum influence in this way.

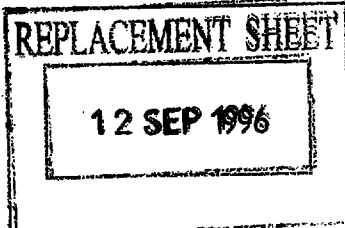
The described circuit performs well with minimum visible defects. It uses readily available components and does not require microprocessor support. Compared to an RGB video line doubler a YUV doubler is of lower cost. However, a matrix for double rate video has to be provided. Since these are available in integrated circuits, that also incorporate contrast and brightness controls, this should not be a disadvantage.





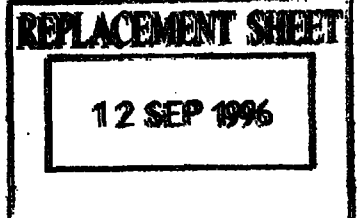
Claims

1. A phase-lock-loop circuit, comprising:
 - a controllable oscillator (53);
 - a source of a synchronizing signal (Q4);
 - a flip-flop (62) responsive to said synchronizing signal for generating a flip-flop output signal (SYN) at a first state when an edge (LE1/LE2) of said synchronizing signal occurs, said output signal alternating between said first state and a second state (H/L); characterized by
 - a decoder (101a) for applying said synchronizing signal to an output of said decoder (66c) via a signal path of said synchronizing signal that includes said flip-flop to generate a phase difference indicative signal (OUT) at said output of said decoder, said phase difference indicative signal being generated in accordance with a phase difference between said synchronizing signal and an output signal of said oscillator (CLK), such that for phase differences that are both positive and negative, no other flip-flop is included in any signal path of said synchronizing signal between said source of synchronizing signal and said output of said decoder; and
 - a low-pass filter (54) responsive to said phase difference indicative signal and coupled to a control input (53a) of said oscillator for controlling said oscillator in a phase-lock-loop manner such that in steady state phase-lock operation, an edge (CE) of said oscillator output signal is aligned with said edge of said synchronizing signal.
2. An apparatus according to Claim 1 further characterized by, a counter (52) responsive to said oscillator output signal (CLK) for frequency dividing said oscillator output signal, said counter being coupled to said decoder (101a) for providing timing information of said edge (CLK) of said oscillator output signal.
3. An apparatus according to Claim 2 characterized in that said counter (52) is coupled to said flip-flop (62) for generating said flip-flop output signal at said second state (SYN = LOW).



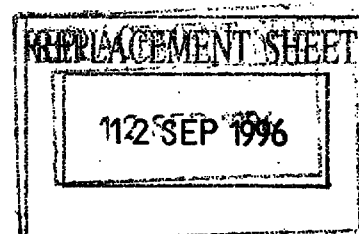


4. A phase-lock-loop circuit according to Claim 3 characterized in that said counter (52) produces a first signal (ClkDiv) and wherein a pulse width of a pulse of said phase difference indicative signal (OUT) is determined in accordance with a length of an interval between an instant (LE1) when said flip-flop output signal (SYN) assumes said first state (SYN=HIGH) in response to said synchronizing signal (CSI) and an instant (TT1) when said first signal occurs.
5. A phase-lock-loop circuit according to Claim 4 characterized in that said counter (52) generates a second signal (CLEAR) that is time-shifted with respect to said first signal (ClkDiv), wherein said synchronizing signal (CSI) is derived from a video signal (VIDEO IN) and includes a horizontal rate signal and an equalizing pulse (EQ) between a given pair of pulses (CSI) of said horizontal rate signal and wherein in a given period of said horizontal rate signal said second signal causes said flip-flop (62) to assume said second state following the occurrence of said equalizing pulse in a manner to prevent said equalizing pulse from affecting said phase difference indicative signal (OUT).
6. A phase-lock-loop circuit according to Claim 1 characterized in that a pulse of said phase difference indicative signal (OUT) is at a first magnitude (HIGH) when said phase difference is positive and at a second magnitude (LOW) when said phase difference is negative.
7. A phase-lock-loop circuit according to Claim 1 further characterized by, a counter (52) responsive to said oscillator output signal (CLK) for generating a first signal (ClkDiv) at a lower frequency wherein said decoder (101a) includes a tri-state gate (66) that couples said first signal of said counter to an output terminal (66c) of said gate to develop a pulse of said phase error indicative signal (OUT) at said output terminal.





8. A phase-lock-loop circuit according to Claim 1 further characterized by, a counter (52) responsive to said oscillator output signal (CLK) for generating a first signal (ClkDiv) that is coupled to said decoder (101a) wherein when said synchronizing signal (CSI) phase-leads said first signal, a pulse of said phase difference indicative signal (OUT) has a leading edge in response to said flip-flop output signal (SYN) and a trailing edge in response to the occurrence of said first signal (TT1), and when said synchronizing signal phase-lags said first signal, said pulse has a leading edge (TT2) in response to the occurrence of said first signal and a trailing edge in response to said flip-flop output signal.
9. A phase-lock-loop circuit according to Claim 8 characterized in that said counter (52) generates a second signal (CLEAR) that is time-shifted with respect to said first signal for initializing said flip-flop (62) and for causing it to assume said second state (SYN=LOW) in a given period of said synchronizing signal (CSI).
10. A phase-lock-loop circuit according to Claim 8 characterized in that said flip-flop (62) is the only memory stage in any signal path between said counter (52) and said output (65c) of said decoder.
11. A phase-lock-loop circuit according to Claim 1 characterized in that said synchronizing signal (CSI) is coupled to said decoder (101a) in a manner that bypasses said flip-flop (via 67) for enabling the generation of said phase error indicative signal (OUT) in normal operation and for disabling the generation of said phase error indicative signal when said synchronizing signal is missing.
12. A phase-lock-loop circuit, comprising:
 - a controllable oscillator (53) for generating an oscillatory signal (CLK);
 - a counter (52) responsive to said oscillatory signal for frequency dividing said oscillatory signal to generate first (ClkDiv) and second (CLEAR) signals having a time difference therebetween and that are synchronized to said oscillatory signal, each having a lower frequency than that of said oscillatory signal;





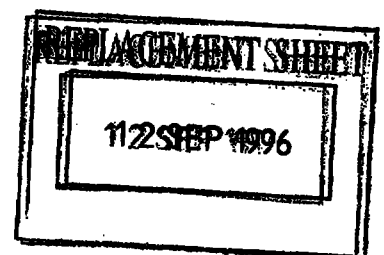
a source of a synchronizing signal (CSI);
characterized by

an edge triggered flip-flop (62) responsive to said synchronizing signal for generating a flip-flop output signal (SYN) at a first state (HIGH) in accordance with a transition of said synchronizing signal, said first state being generated when a phase difference between said synchronizing signal and said first signal is positive and when said phase difference is negative, said flip-flop being responsive to said second signal for generating said flip-flop output signal at a second state (LOW) in accordance with said second signal, said flip-flop output signal alternating between said first and second states within a given period of said synchronizing signal;

a decoder (101a) for generating a signal (OUT) that is indicative of said phase difference at a first state (HIGH), when said flip-flop output signal is at said first state and said first signal (ClkDiv) is at a first state (HIGH), for generating said decoder output signal at a second state (LOW), when said flip-flop output signal is at said second state (LOW) and said first signal is at a second state (LOW) and for generating said decoder output signal at a third state (TRI-STATE) during the remainder of a given period of said synchronizing signal; and

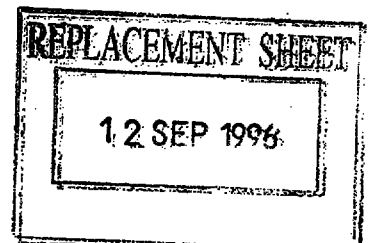
a low-pass filter (54) responsive to said phase difference indicative signal and coupled to a control input (53a) of said oscillator for controlling said oscillator in a phase-lock-loop manner.

13. A phase-lock-loop circuit according to Claim 12 characterized in that both when said phase difference is positive and negative, only one (FALLING EDGE) of a rising edge and a falling edge of a given pulse of said synchronizing signal (CSI) affects said phase difference indicative signal (OUT) and only one (FALLING EDGE) of a rising edge and a falling edge of a given pulse of said first signal (ClkDiv) affects said phase difference indicative signal.
14. A phase-lock-loop according to Claim 13 characterized in that said edges of said synchronizing (CSI) and first (ClkDiv) signals are aligned in steady state phase-lock operation.





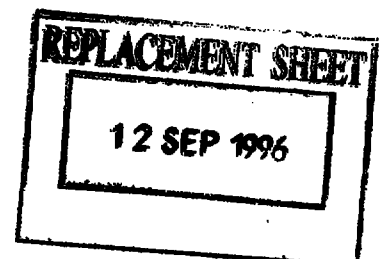
15. A phase-lock-loop circuit, comprising:
- a controllable oscillator (53) for generating an oscillator output signal (CLK);
 - means (52) responsive to said oscillator output signal for frequency dividing said oscillator output signal to generate a first signal (CikDiv) at a lower frequency than that of said oscillator output signal and that is synchronized thereto;
 - a source of a synchronizing signal (CSI) containing pulses;
 - an edge triggered flip-flop (62) responsive to said synchronizing signal for generating a flip-flop output signal (SYN) at a first state (HIGH) in accordance with an edge (LE1) of said synchronizing signal, said first state being generated when a phase difference between said synchronizing signal and said first signal is positive and when said phase difference is negative, said flip-flop output alternating between said first state and a second state (LOW); characterized by
 - a decoder (101a) responsive to said flip-flop output signal and to said first signal for generating at an output of said decoder (68c) a decoder output signal (OUT) that is indicative of said phase difference and that is independent of a duty cycle of said synchronizing signal, said decoder output signal being generated in accordance with a difference between a time (LE1) when said first state of said flip-flop output signal occurs and a time (TT1) when said first signal occurs, such that for positive and negative phase differences, no flip-flop other than said flip-flop is used to incorporate timing information from said synchronizing signal into phase difference information of said decoder output signal; and
 - a low-pass filter (54) responsive to said phase difference indicative signal and coupled to a control input (53a) of said oscillator for controlling said oscillator in a phase-lock-loop manner.
16. A phase-lock-loop circuit according to Claim 15 characterized in that in steady state phase-lock operation, an edge (CE) of said oscillator output signal (CLK) is aligned to occur substantially simultaneously with an edge (LE1) of said synchronizing signal.





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17. A phase-lock-loop circuit according to Claim 15 characterized in that said first signal generating means (52) comprises a counter (52) responsive to said oscillator output signal (CLK) for frequency dividing said oscillator output signal, said counter being coupled to said decoder (101a) for providing timing information of said edge (CE) of said oscillator output signal.
18. A phase-lock-loop circuit according to Claim 17 characterized in that said counter (52) is coupled to said flip-flop (62) for generating said flip-flop output signal (SYN) at said second state (LOW).

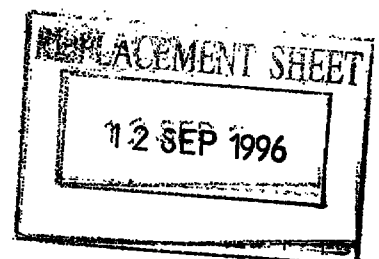


YUV VIDEO LINE DOUBLER

ABSTRACT

A line-locked-clock generator circuit includes an oscillator, a counter with a 2:1 ratio output pulse connected to a tristate buffer, a reference input for providing composite sync and a control circuit. The clock generator is coupled to a line memory. Video component signals U and V are clamped using a single clamp arrangement. The clamped signal is processed through an analog-to-digital converter and applied to the line memory.

FIG 3



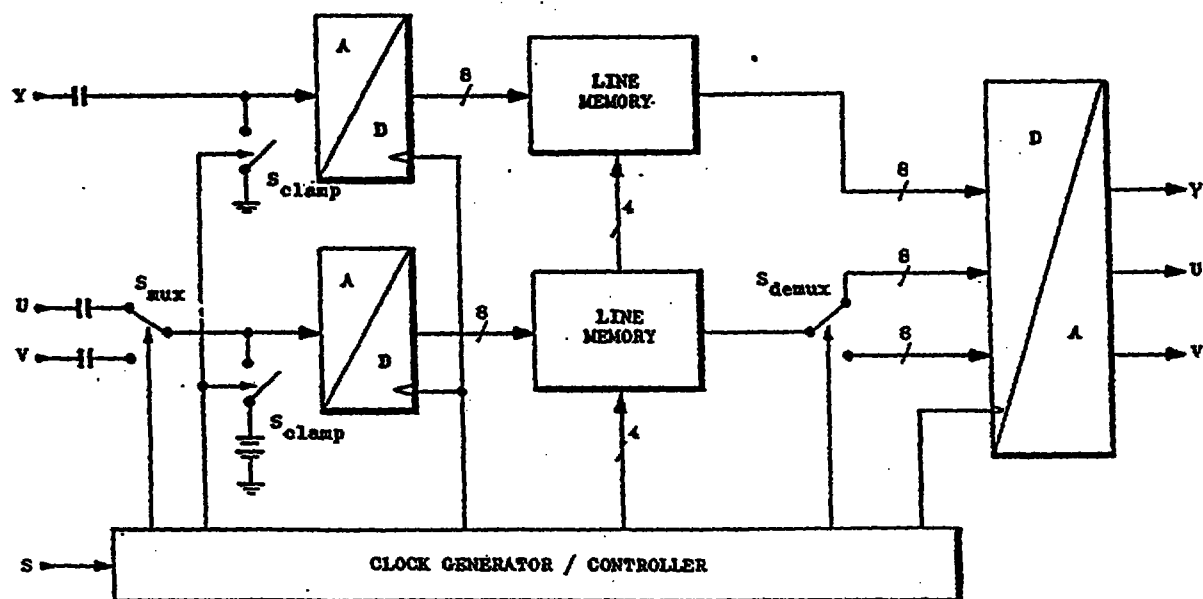
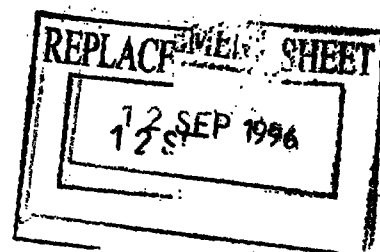


FIG.1 BLOCK DIAGRAM



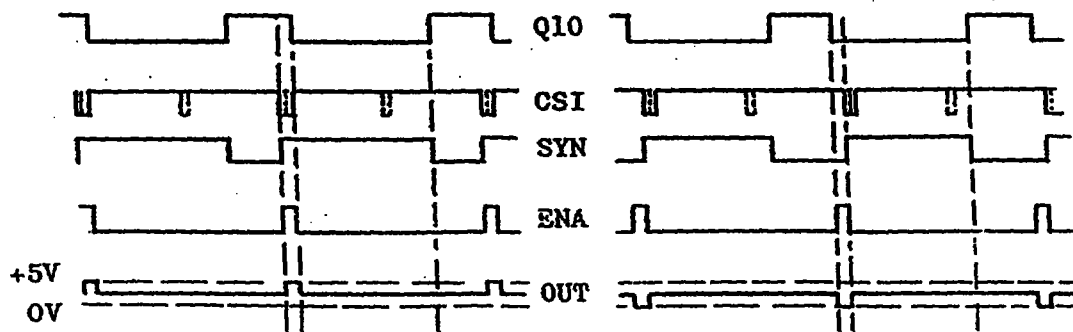
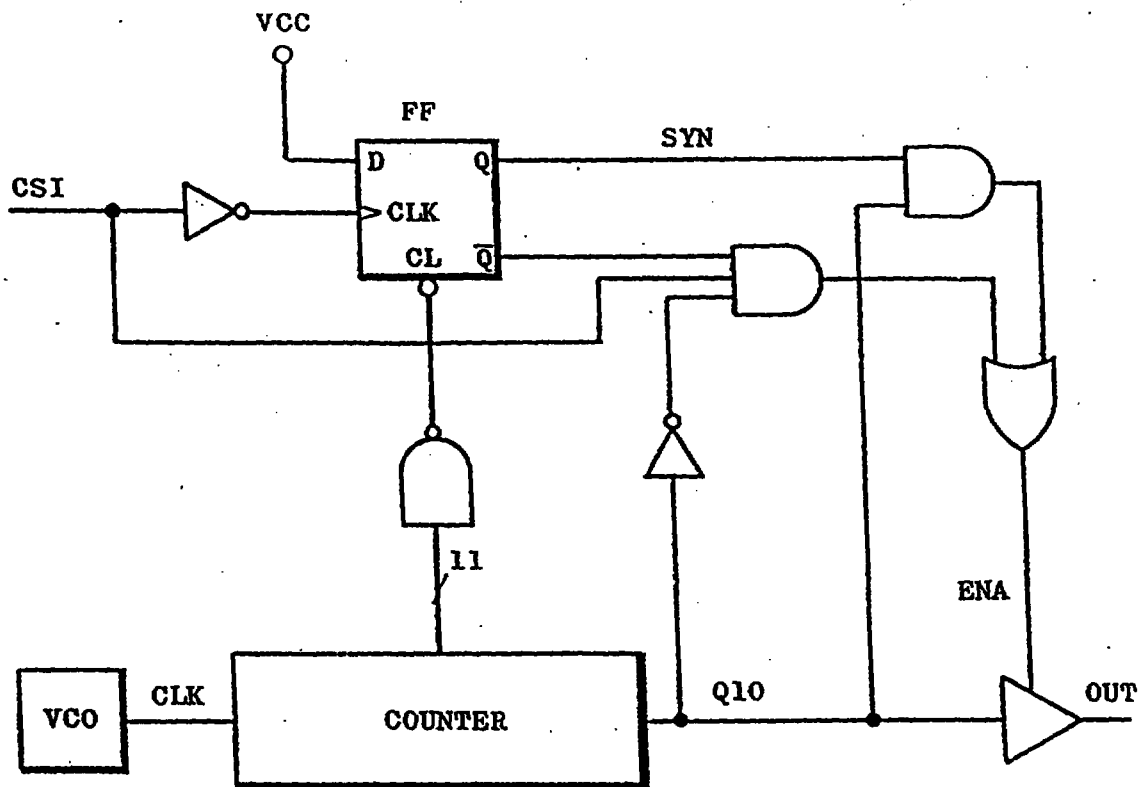


FIG.2 COUNTER / PHASE COMPARATOR

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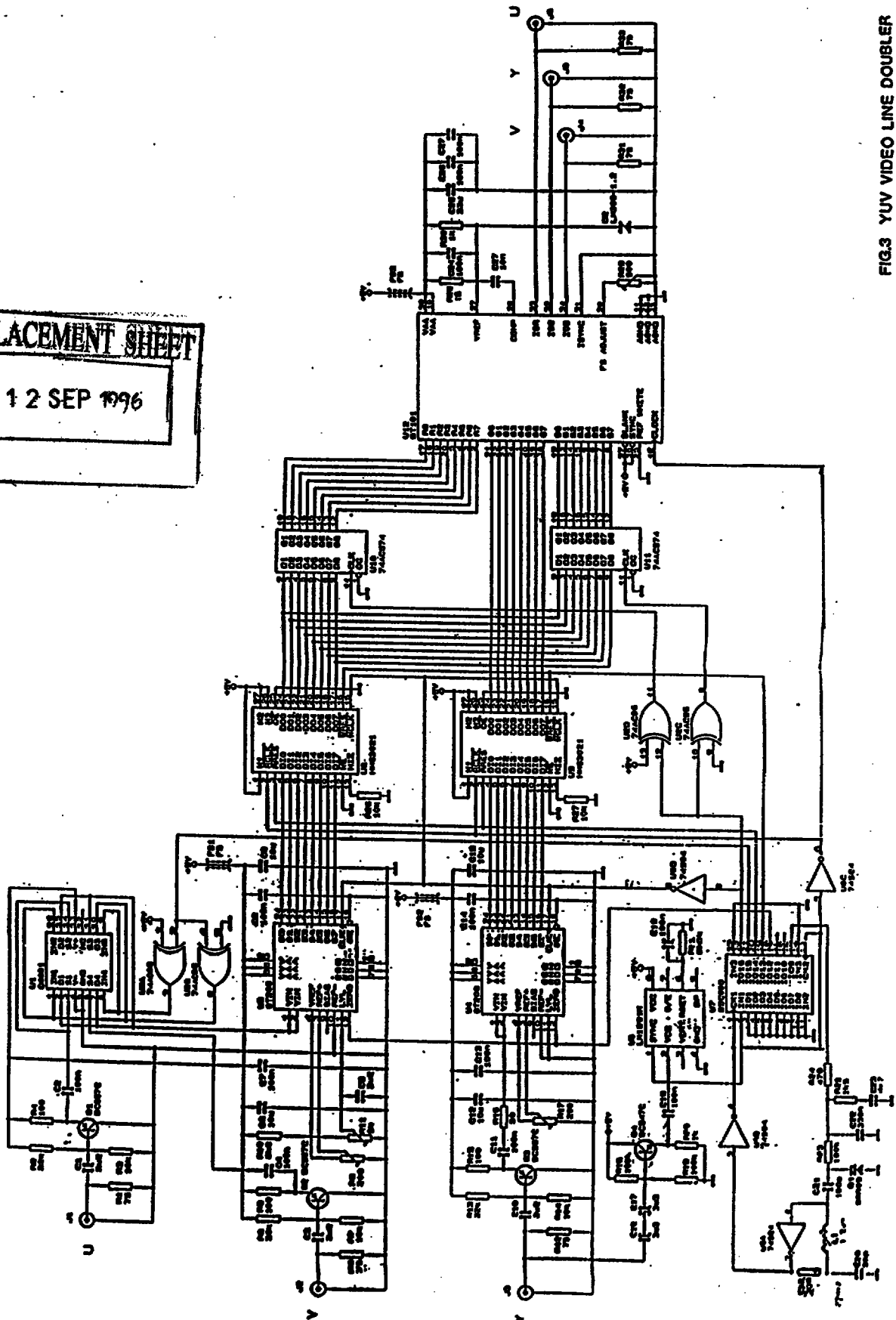


FIG.3 YUV VIDEO LINE DOUBLER

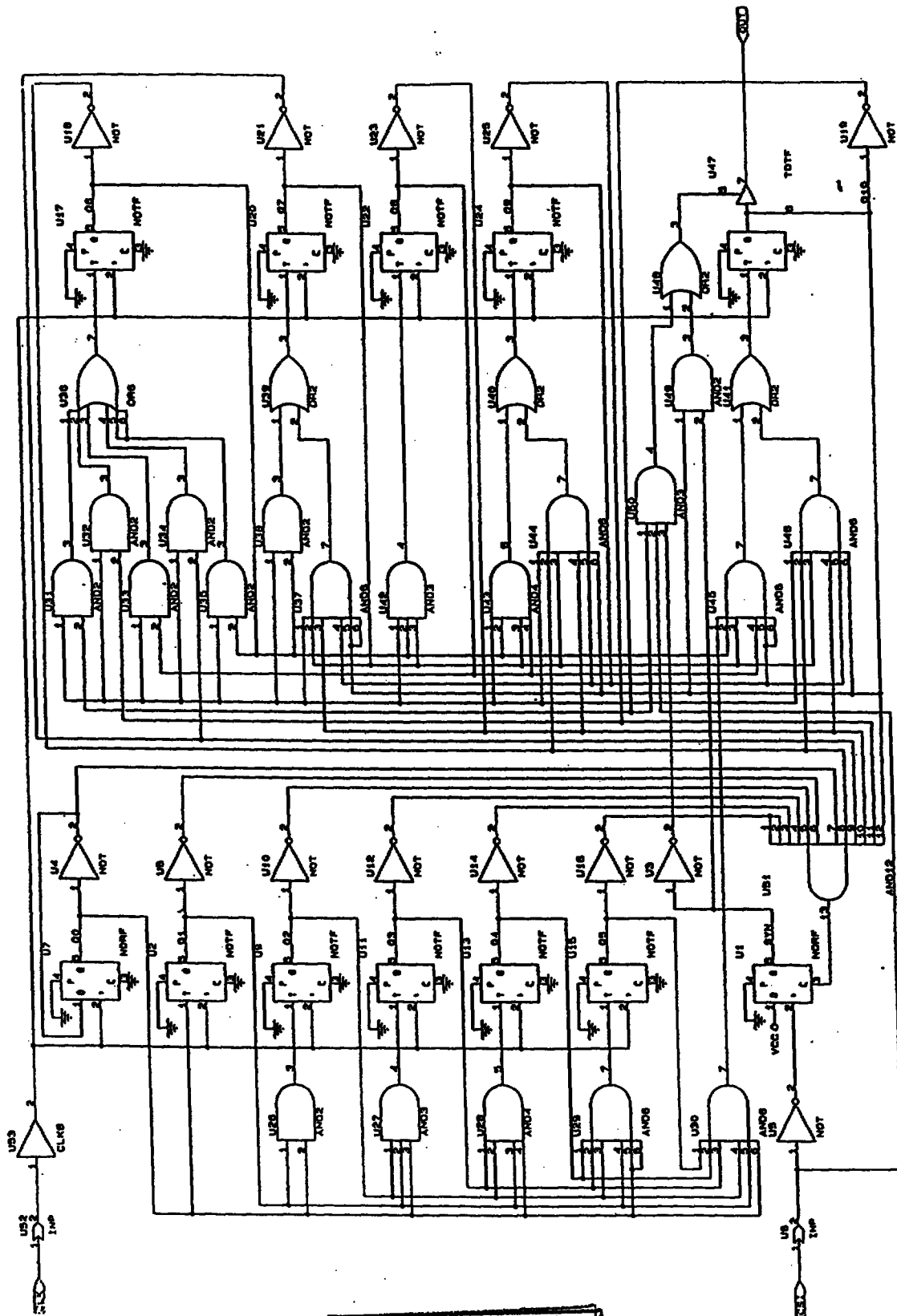
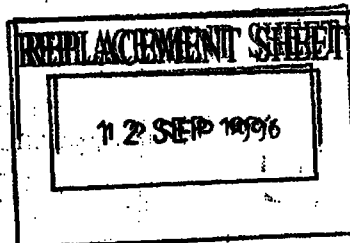


Fig.4 Internal circuit of Programmable Logic Device



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