WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a substrate comprising a first active pattern, the first active pattern comprising a first source/drain region, a second source/drain region and a third source/drain region, wherein the first source/drain region is between the second source/drain region and the third source/drain region;

a gate electrode crossing the first active pattern, extending in a first direction, and crossing a region between the first and second source/drain regions;

a bit line crossing the first active pattern and extending in a second direction, the bit line being electrically connected to the first source/drain region;

a spacer on a side surface of the bit line;

a first contact coupled to the second source/drain region and spaced apart from the bit line with the spacer interposed therebetween;

a landing pad on the first contact;

a data storing element on the landing pad; and

a second contact coupled to the third source/drain region,

wherein the second source/drain region has a top surface, an upper side surface, and a curved top surface that extends from the top surface to the upper side surface,

wherein the first contact is in contact with the curved top surface and the upper side surface,

wherein the second contact is in contact with a curved top surface and an upper side surface of the third source/drain region,

wherein a lowermost level of the curved top surface of the second source/drain region is at a first level,

wherein a lowermost level of the curved top surface of the third source/drain region is at a second level,

wherein a lowermost level of the first contact is at a third level,

wherein a lowermost level of the second contact is at a fourth level, and

wherein a difference between the first level and the second level is larger than a difference between the third level and the fourth level.

2. The semiconductor memory device of claim 1, wherein the first contact

comprises:

a lower portion in contact with the curved top surface; and

a vertically-extended portion protruding from the lower portion toward a bottom of the substrate along the upper side surface.

3. The semiconductor memory device of claim 2, further comprising a device isolation layer that is in a first trench defining the first active pattern,

wherein the vertically-extended portion extends into an upper portion of the device isolation layer.

4. The semiconductor memory device of claim 3,

wherein the substrate further comprises a second active pattern,

wherein each of the first and second active patterns has a longitudinal axis parallel to a third direction,

wherein the first and second active patterns are adjacent to each other in the third direction,

wherein the device isolation layer is in a second trench between the first and second active patterns, and

wherein the second trench is deeper than the first trench.

5. The semiconductor memory device of any one of claims 2 to 4,

wherein an upper portion of the first contact has a first side surface and a second side surface that are opposite to each other in the first direction,

wherein the second side surface is in contact with the spacer, and

wherein the lower portion of the first contact has a profile that is gradually spaced apart from a vertical imaginary line that vertically extends from the first side surface, in the first direction as a distance from the bottom of the substrate decreases.

6. The semiconductor memory device of any one of claims 1 to 5,

wherein the curved top surface has an average slope defining a first angle, and

wherein the first angle ranges from 40° to 80°.

7. The semiconductor memory device of claim 6,

wherein the upper side surface has a slope defining a second angle, and

wherein the second angle is greater than the first angle.

8. The semiconductor memory device of claim 1, wherein a width of a lower portion of the first contact in the first direction decreases with decreasing distance from a bottom of the substrate.

9. The semiconductor memory device of any one of claims 1 to 8, further comprising a conductive pattern between the bit line and the first active pattern,

wherein the conductive pattern is coupled to the first source/drain region of the first active pattern, and

wherein a bottom surface of the conductive pattern in contact with the first source/drain region is higher than a lowermost level of the first contact.

10. A semiconductor memory device comprising:

a substrate having a first active pattern, a second active pattern, and a third active pattern that are sequentially arranged in a first direction;

a bit line crossing the second active pattern and extending in a second direction, the bit line being electrically connected to the second active pattern;

a first contact coupled to the first active pattern;

a second contact coupled to the third active pattern;

landing pads on the first and second contacts, respectively; and

data storing elements on the landing pads, respectively,

wherein the first contact is in contact with a curved top surface of the first active pattern,

wherein the second contact is in contact with a curved top surface of the third active pattern,

wherein a lowermost level of the curved top surface of the first active pattern is at a first level,

wherein a lowermost level of the curved top surface of the third active pattern is at a second level,

wherein a lowermost level of the first contact is at a third level,

wherein a lowermost level of the second contact is at a fourth level, and

wherein a difference between the first level and the second level is larger than a difference between the third level and the fourth level.

11. The semiconductor memory device of claim 10, further comprising a gate electrode crossing the first to third active patterns and extending in the first direction.

12. The semiconductor memory device of claim 10 or claim 11, wherein the first contact comprises:

a lower portion in contact with the curved top surface of the first active pattern; and

a vertically-extended portion protruding from the lower portion toward a bottom of the substrate along an upper side surface of the first active pattern.

13. The semiconductor memory device of claim 12, further comprising a device isolation layer that is in a trench between the first and second active patterns,

wherein the vertically-extended portion extends into an upper portion of the device isolation layer.

14. The semiconductor memory device of any one of claims 10 to 13,

wherein the curved top surface of the first active pattern has an average slope defining a first angle,

wherein the curved top surface of the third active pattern has an average slope defining a second angle, and

wherein the second angle is smaller than the first angle.

15. A semiconductor memory device comprising:

a substrate including an active pattern, the active pattern having a longitudinal axis parallel to a first direction and comprising a first source/drain region and a pair of second source/drain regions that are spaced apart from each other in the first direction with the first source/drain region interposed therebetween;

a device isolation layer on the substrate, in a first trench defining the active pattern;

a pair of gate electrodes crossing the active pattern and extending in a second direction, each of the pair of gate electrodes being in a second trench between the first source/drain region and a first one of the pair of second source/drain regions;

a gate dielectric layer interposed between each of the pair of gate electrodes and the active pattern;

a gate capping layer on each of the pair of gate electrodes, in the second trench;

an insulating layer on the substrate;

a line structure on the insulating layer to cross the active pattern and extend in a third direction, the line structure comprising:

a conductive pattern that penetrates the insulating layer and is coupled to the first source/drain region;

a bit line on the conductive pattern; and

a barrier pattern between the bit line and the conductive pattern;

a pair of spacers on opposite side surfaces of the line structure, respectively;

a first contact and a second contact that are in contact with the first one and a second one of the pair of second source/drain regions, respectively, the first and second contacts being spaced apart from the line structure by the pair of spacers;

landing pads on the first and second contacts, respectively;

first electrodes on the landing pads, respectively;

a second electrode on the first electrodes; and

a dielectric layer interposed between the first electrodes and the second electrode,

wherein a bottom surface of the conductive pattern in contact with the first source/drain region is at a level higher than a lowermost level of the first contact,

wherein the first contact is in contact with a first curved top surface of the first one of the pair of second source/drain regions,

wherein the second contact is in contact with a second curved top surface of the second one of the pair of second source/drain regions,

wherein a lowermost level of the first curved top surface is at a first level,

wherein a lowermost level of the second curved top surface is at a second level,

wherein a lowermost level of the first contact is at a third level,

wherein a lowermost level of the second contact is at a fourth level, and

wherein a difference between the first level and the second level is larger than a difference between the third level and the fourth level.

16. The semiconductor memory device of claim 15,

wherein the first one of the pair of second source/drain regions that is in contact with

the first contact has a flat top surface, an upper side surface, and the first curved top surface that extends from the flat top surface to the upper side surface, and

wherein the first contact is in contact with the first curved top surface and the upper side surface.

17. The semiconductor memory device of claim 16, wherein the first contact comprises:

a lower portion in contact with the first curved top surface; and

a vertically-extended portion protruding from the lower portion into an upper portion of the device isolation layer along the upper side surface.

18. The semiconductor memory device of claim 15,

wherein the first curved top surface has an average slope defining a first angle,

wherein the second curved top surface has an average slope defining a second angle, and

wherein the second angle is smaller than the first angle.