

IC SOCKET

TECHNICAL FIELD

The present invention relates to an IC socket with which a
5 semiconductor integrated circuit (which will be referred to as
"IC" hereinafter) is to be electrically contacted, and more
particularly, to an IC socket suitable for use, for example, with
an IC testing apparatus (commonly called IC tester) for testing
ICs.

BACKGROUND ART

As shown in Fig. 6, a conventional IC socket 1 comprises
an electrically insulating resin block 2 having a plurality of
spaced apart through-holes 2A vertically formed therethrough in
15 which round elongated conductors 3a, 3b, 3c called "probe
contact" are mounted by press-fitting, for example (hereinafter
each of the round elongated conductors will be referred to as
probe contact). Each of the probe contacts has contacts 3A and
3B mounted at its opposite ends, the contacts 3A and 3B being
20 movable in the axial direction of the probe contact. The upper
contact 3A as viewed in the drawing is to be brought into contact
with the corresponding terminal of an IC 4 under test (which will
be referred to as "DUT" hereinafter). In this example, the DUT
4 is a ball grid array type IC (an IC having a number of ball-like
25 terminals (bumps) formed on the bottom surface of the IC
package; which will be referred to as BGA-IC hereinafter), so
that the end face of the contact 3A is bowl-like concavely shaped
so as to maintain stable contact with the ball terminal 4A of the

DUT 4. The lower contact 3B has a conically convex shaped tip so as to maintain stable contact with a land 6 formed on the surface of a socket board 5.

5 The socket board 5 is a printed board for mounting an IC socket thereon, and it typically comprises a multi-layer printed board having a predetermined number of lands (conductor pads) 6 formed on the top and bottom surfaces (upper and lower surfaces as viewed in the drawing) thereof. Each pair of
10 opposed upper and lower lands 6 positioned on the top and bottom surfaces are electrically connected with each other by a corresponding one of through-hole conductors 7a, 7b, 7c formed in the respective through-holes. That portion of the socket board 5 on which the IC socket 1 is not mounted has likewise a predetermined number of lands formed on the top and bottom
15 surfaces (upper and lower surfaces as viewed in the drawing) thereof (only the lands formed on the bottom surface are designated by 10a, 10b, 10c in the drawing), and each pair of opposed upper and lower lands positioned on the top and bottom surfaces are electrically connected with each other by a
20 corresponding one of through-hole conductors 8a, 8b, 8c formed in the respective through-holes.

When the IC socket 1 is placed on the top surface of the socket board 5 constructed as described above, the lands 6 of the top surface of the socket board come into contact with the
25 contacts 3B of the corresponding probe contacts of the IC socket 1. These lands 6 are connected, via the through-hole conductors 7a, 7b, 7c, the internal conductor layers (wiring patterns) 9a, 9b, 9c in the socket board and the through-hole conductors 8a, 8b,

8c, with the connector terminals (lands) 10a, 10b, 10c for connection with an external circuit or apparatus, respectively, whereby the IC socket 1 is connected with the external circuit or apparatus.

5 Within the socket board 5, three, in this example, conductor layers (wiring patterns) 9a, 9b, 9c are formed in three layers electrically insulated from each other. The uppermost conductor layer 9a is a ground (also denoted as GND for short) pattern for providing a common potential to a DUT 4 and is
10 electrically connected with the through-hole conductors 7a and 8a. The intermediate conductor layer 9b is a power source pattern for providing an electric power to the DUT 4 and is electrically connected with the through-hole conductors 7b and 8b. The lowermost conductor layer 9c is a signaling pattern for
15 applying test signals to the DUT 4 and detecting response signals from the DUT 4 and is electrically connected with the through-hole conductors 7c and 8c.

 It is thus to be understood that in the illustrated example, the through-hole conductors 7a and 8a constitute a grounding
20 through-hole conductor, the through-hole conductors 7b and 8b constitute a power source through-hole conductor, and the through-hole conductors 7c and 8c constitute a signaling through-hole conductor. Likewise, the probe contact 3a of the IC socket 1 constitutes a grounding probe contact, the probe
25 contact 3b constitutes a power source probe contact, and the probe contact 3c constitutes a signaling probe contact.

 The signaling land 10c electrically connected with the signaling pattern 9c and the grounding land 10a electrically

connected with the grounding pattern 9a are connected through the core and the shield of a cable 11, and the power source land 10b electrically connected with the power source pattern 9b is connected through a wiring 13, respectively, to a performance
5 board 12 and then through the wiring in the performance board 12 and further through probe contact pins 15 to the tester head 14 of an IC tester.

The DUT 4 and the IC socket 1 have a plurality of balls 4A and probe contacts 3 to be contacted with the balls formed
10 thereon as required, respectively, in order to increase the current capacity to the GND bus (current capacity flowing into or from a point of common potential) as well as to reduce the impedance of the GND path.

In the conventional IC socket 1, since the inductances of
15 the probe contacts 3a, 3b, 3c themselves are inserted serially into the connecting line to the DUT 4, there is a disadvantage that an impedance mismatching undesirably occurs thereby. Such impedance mismatching will distort a signal waveform at high rate or speed resulting in lowering of accuracy in measurements
20 as well as distorting a power source waveform, thereby causing power source noises.

DISCLOSURE OF THE INVENTION

It is an object of the present invention to provide an IC
25 socket which has overcome the foregoing problems incidental to the conventional IC socket.

It is another object of the present invention to provide an IC socket which is configured to avoid the occurrence of any

impedance mismatching.

It is yet another object of the present invention to provide an IC socket which is configured to produce capacitances for bypassing power source noises between a ground conductor layer and a power source conductor layer both of which are formed in a multi-layer printed board to suppress the distortion of power source waveforms and the generation of power source noises.

In order to accomplish the foregoing objects, in a first aspect of the present invention, there is provided an IC socket comprising: a multi-layer printed board having at least two conductor layers including a ground conductor layer and a power source conductor layer laminated one on another at a predetermined spacing and having a plurality of through-holes vertically formed therethrough; through-hole conductors formed in all of the through-holes of the multi-layer printed board, and including a ground through-hole conductor electrically connected with the ground conductor layer, a power source through-hole conductor electrically connected with the power source conductor layer, and a signaling through-hole conductor connected with none of the conductor layers; and probe contacts attached to the respective through-hole conductors and adapted to be electrically contacted with terminals of an IC under test, the IC socket being constructed such that a capacitance is produced, with the material of the multi-layer printed board as a dielectric, between the ground conductor layer and the power source conductor layer so as to bypass power source noises.

In a preferred embodiment, a plurality of the ground through-hole conductor are formed, and at least one of these

ground through-hole conductors has none of the probe contacts attached thereto.

In addition, distances of gaps between the signaling through-hole conductor and the ground conductor layer, and
5 between the signaling through-hole conductor and the power source conductor layer are set such that the characteristic impedance of the transmission line formed by electrostatic capacitances across the gaps and a parasitic inductance of the probe contact is equal to a predetermined value.

10 In the case that the IC under test is a BGA-IC (Ball Grid Array type Integrated Circuit), each of the probe contacts is formed at one end on the side of the IC under test with a contact to be contacted with the corresponding ball-like terminal of the BGA-IC and at the opposite end with a pin contact to be
15 contacted with the corresponding land formed on the surface of a socket board on which the IC socket is to be placed.

Further, the aforesaid multi-layer printed board has at least four conductor layers embedded therein including ground conductor layers and power source conductor layers alternately
20 laminated one on another at predetermined spacings, whereby capacitances are produced, with the material of the multi-layer printed board as a dielectric, between each pair of the adjacent two ground conductor layer and power source conductor layer.

In a second aspect of the present invention, the aforesaid
25 multi-layer printed board has at least four conductor layers embedded therein including ground conductor layers and power source conductor layers alternately laminated one on another at predetermined spacings, and an interstitial via hole or a via hole

for electrically interconnecting two ground conductor layers or two power source conductor layers is formed around the aforesaid signaling through-hole conductor.

5 In a preferred embodiment, two ground conductor layers and two power source conductor layers are alternately laminated one on another at predetermined spacings, and an interstitial via hole or a via hole for electrically interconnecting two ground conductor layers or two power source conductor layers is formed around the aforesaid signaling through-hole conductor.

10 In addition, a plurality of the ground through-hole conductor are formed, and at least one of these ground through-hole conductors has none of the probe contacts attached thereto.

Moreover, distances of gaps between the signaling through-hole conductor and the ground conductor layers, and
15 between the signaling through-hole conductor and the power source conductor layers are set such that the characteristic impedance of the transmission line formed by the sum of electrostatic capacitances across these gaps plus an electrostatic capacitance produced between the signaling through-hole
20 conductor and the interstitial via hole or via hole, and a parasitic inductance of the probe contact is equal to a predetermined value.

In the case that the IC under test is a BGA-IC, each of the probe contacts is formed at one end on the side of the IC under test with a contact to be contacted with the corresponding ball-
25 like terminal of the BGA-IC and at the opposite end with a pin contact to be contacted with the corresponding land formed on the surface of a socket board on which the IC socket is to be placed.

Further, the aforesaid multi-layer printed board has at least four conductor layers embedded therein including ground conductor layers and power source conductor layers alternately laminated one on another at predetermined spacings, whereby capacitances are produced, with the material of the multi-layer printed board as a dielectric, between each pair of the adjacent two ground conductor layer and power source conductor layer.

In a third aspect of the present invention, an IC socket is provided which comprises: a multi-layer printed board having a ground conductor layer, a power source conductor layer and a signaling conductor layer laminated one on another at predetermined spacings and having a plurality of through-holes vertically formed therethrough; through-hole conductors formed in all of the through-holes of the multi-layer printed board, and including a ground through-hole conductor electrically connected with the ground conductor layer, a power source through-hole conductor electrically connected with the power source conductor layer, and a signaling through-hole conductor connected with the signaling conductor layer; tubular sockets attached to the respective through-hole conductors; and probe contacts fitted in the respective tubular sockets and adapted to be electrically contacted with terminals of an IC under test, the IC socket being constructed such that a capacitance is produced, with the material of the multi-layer printed board as a dielectric, between the ground conductor layer and the power source conductor layer so as to bypass power source noises.

In a preferred embodiment, a plurality of the ground through-hole conductor are formed, and at least one of these

ground through-hole conductors has none of the probe contacts attached thereto.

In addition, distances of gaps between the signaling through-hole conductor and the ground conductor layer, and
5 between the signaling through-hole conductor and the power source conductor layer are set such that the characteristic impedance of the transmission line formed by electrostatic capacitances across these gaps and a parasitic inductance of the probe contact is equal to a predetermined value.

10 In the case that the IC under test is a BGA-IC, each of the aforesaid probe contacts is formed at one end on the side of the IC under test with a contact to be contacted with the corresponding ball-like terminal of the BGA-IC, and the multi-layer printed board has external connecting lands formed on at
15 least one side surface thereof, the lands being electrically connected with the ground conductor layer, the power source conductor layer and the signaling conductor layer, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Fig. 1 is a sectional view illustrating in principle the configuration and electrical connections of a first embodiment of the IC socket according to the present invention;

Fig. 2 is a circuit diagram showing electrical connections between power source conductor layers and ground conductor
25 layers of the IC socket shown in Fig. 1;

Fig. 3 is an electrical equivalent circuit diagram of the signaling probe contact 3c and its peripheral components of the IC socket shown in Fig. 1;

Fig. 4 is a sectional view illustrating in principle the configuration and electrical connections of a second embodiment of the IC socket according to the present invention;

Fig. 5 is a sectional view illustrating in principle the configuration and electrical connections of a third embodiment of the IC socket according to the present invention; and

Fig. 6 is a sectional view illustrating in principle the configuration and electrical connections of a conventional IC socket and its peripheral devices.

BEST MODE FOR CARRYING OUT THE INVENTION

Several embodiments of the present invention will now be described in details with reference to Figs. 1 to 5. Further, those parts and/or components in these drawings corresponding to those of Fig. 6 are indicated by the same reference characters and will not be discussed again unless required.

Fig. 1 is a sectional view illustrating in principle the configuration and electrical connections of the first embodiment of the IC socket according to the present invention. In this embodiment as is the case with the conventional IC socket shown in Fig. 6, it is assumed that the IC 4 under test (DUT) which is to be put into contact with the contacts 3A on the top of the IC socket 1 is a ball grid array type IC (BGA-IC).

In this embodiment, the IC socket 1 comprises a multi-layer printed board 20 having at least four conductor layers (wiring patterns) including ground conductor layers (wiring patterns) and power source conductor layers (wiring patterns) alternately laminated one on another at predetermined spacings,

and having a plurality of through-holes vertically formed therethrough; through-hole conductors 21a, 21a', 21b, 21c formed in a plurality of the through-hole, respectively, of the multi-layer printed board 20; and probe contacts 3a, 3b, 3c
5 attached to the respective through-hole conductors (21a, 21b, 21c in this embodiment) other than at least one (21a' in this embodiment) of those through-hole conductors as by press-fitting and adapted to be electrically contacted with terminals of the DUT 4. The ground conductor layers 23 and 25 (which will
10 be referred to as "ground pattern" or "GND pattern" hereinafter) are electrically connected with the through-hole conductors 21a and 21a', respectively, while the power source conductor layers 22 and 24 (which will be referred to as "power source pattern" hereinafter) are electrically connected with the through-hole
15 conductors 21b, respectively. It is thus to be understood that the through-hole conductors 21a and 21a' comprise ground through-hole conductors and that the probe contacts 3a attached to these ground through-hole conductors 21a, 21a' comprise ground probe contacts. Similarly, the through-hole conductor 21b
20 comprises a power source through-hole conductor 21b and the probe contact 3b attached to this power source through-hole conductor 21b comprises a power source probe contact. The through-hole conductor 21c comprises a signaling through-hole conductor and the probe contacts 3c attached to this signaling
25 through-hole conductor 21b comprises a signaling probe contact.

Like the conventional IC socket, the contacts 3A and 3B mounted at the opposite ends of each of the probe contacts are movable axially of the probe contact. In addition, since the DUT

4 is a BGA-IC, the end face of each of the upper contacts 3A to be brought into contact with the corresponding terminals (balls 4A) of the DUT 4 is bowl-like concavely shaped while each of the lower contacts 3B to be contacted with lands formed on the surface of a socket board 5 has a conically convex shaped tip. In the case that the DUT 4 is an IC other than the BGA-IC, it is needless to say that the upper contacts 3A are formed so as to have a shape adapted to securedly come into contact with the corresponding terminals of an IC under test. Further, it is to be noted here that the socket board 5 is similar in construction to that of the conventional IC socket shown in Fig. 6, and will not be further described here.

In the IC socket 1 constructed as mentioned above, a capacitor CA is formed with the material of the printed board 20 as a dielectric between the GND pattern 23 to which the ground through-hole conductors 21a, 21a' are connected and the power source pattern 22 to which the power source through-hole conductor 21b is connected, and likewise a capacitor CB is formed with the material of the printed board 20 as a dielectric between the GND pattern 25 to which the ground through-hole conductors 21a, 21a' are connected and the power source pattern 24 to which the power source through-hole conductor 21b is connected. These capacitors CA and CB have the function of bypassing power source noises. It should be noted that as the case may be, external capacitors (not shown) may be connected in parallel with the capacitors CA and CB, respectively.

The through-hole conductor 21a' with no probe contacts fitted therein is connected in parallel with the GND through-hole

conductors 21a with the probe contacts 3a fitted therein through the GND patterns 23, 25 to thereby reduce the serial impedance of the GND path. In some instances, however, the through-hole conductor 21a' may be omitted.

5 Fig. 2 shows a schematic diagram of electrical connections between the power source patterns 22, 24 and the ground patterns 23, 25 of the IC socket 1 shown in Fig. 1. As shown in Fig. 2, a plurality of GND through-hole conductors 21a with the probe contacts 3a fitted therein and a plurality of GND through-hole conductor 21a' with no probe contacts 3a fitted therein are
10 connected in parallel with one another through the GND patterns 23, 25, respectively. As a result, the current capacity flowing into or from a point of common potential, that is, the current capacity to the GND bus is increased, and at the same time the
15 serial impedance of the GND path is suppressed to a small value, whereby the problem of impedance mismatching is eliminated.

 In addition, the parasitic inductances L_a , L_b , L_c of the power source probe contact 3b and the above capacitors (electrostatic capacitances) 3A, CB together constitute a low-
20 pass filter (LPF), the width of the pass band of which may be set to be sufficiently broad, and hence, even if the power source current/voltage of a DUT 4 should change stepwise, waveform distortions such as overshoots and/or undershoots of the current/voltage waveforms which may occur at the rise and/or
25 fall thereof are suppressed to an insignificant level, and accordingly, the resulting noise components are suppressed to an insignificant level. Besides, external noises may also be kept low by this low-pass filter.

Further, in Fig. 2, L_d , L_e , L_f show parasitic inductances of the GND probe contacts 3a, respectively, and L_g shows parasitic inductances of the GND through-hole conductors 21a'.

Fig. 3 is an electrical equivalent circuit diagram of the signaling probe contact 3c and its peripheral components of the IC socket 1 shown in Fig. 1. The capacitors CA, CB are considerably large relative to the signal frequency so that the power source patterns 22, 24 are short-circuited through the capacitors 3A, CB to the GND patterns 23, 25, respectively. The distances of gaps d_1 to d_4 between the signaling through-hole conductor 21c and the GND patterns 23, 25 and between the signaling through-hole conductor 21c and the power source patterns 22, 24 are set such that the characteristic impedance Z_0 of the transmission line formed by the electrostatic capacitances C_1 to C_4 corresponding to the gaps respectively and the parasitic inductances L_1 to L_5 of the signaling probe contact 21c is equal to a predetermined value (50 Ω , for example). That is, it is represented by the following equation:

$$Z_0 = \sqrt{\frac{L_1 + L_2/2}{C_1}} \approx \sqrt{\frac{L_2/2 + L_3/2}{C_2}} \approx \sqrt{\frac{L_3/2 + L_4/2}{C_3}} \approx \sqrt{\frac{L_4/2 + L_5}{C_4}} \dots \dots (1)$$

In this manner, the characteristic impedance Z_0 of the signaling probe contact 3c is set to the predetermined value, and

the impedance matching of the signaling probe contact 3c with respect to the DUT 4 and the socket board 5 may be achieved. As a result, the conventional waveform distortions due to the parasitic inductances are suppressed. In other words, any waveform distortions due to the impedance mismatching are suppressed.

The second embodiment of the IC socket according to the present invention is shown in Fig. 4. In this embodiment, the IC socket 1 serves as a conventional socket board 5 as well as an IC socket. This IC socket 1 employs, as a multi-layer printed board of the IC socket 1, a multi-layer printed board 20' having three conductor layers, a GND pattern 9a, a power source pattern 9b and a signaling pattern 9c formed in a manner electrically insulated from one another. The multi-layer printed board 20' has a predetermined number of through-holes vertically formed therethrough in which through-hole conductors 21a, 21a', 21b, 21c are formed. Further, tubular sockets 30a, 30b, 30c are attached to the respective through-hole conductors (21a, 21b, 21c in this embodiment) other than at least one (21a' in this embodiment) of those through-hole conductors as by press-fitting. Fitted in these tubular sockets 30a, 30b, 30c are probe contacts 3a, 3b, 3c which are adapted to be electrically contacted with terminals (balls 4A) of the DUT 4, respectively.

The through-hole conductors 21a and 21a' are electrically connected with the GND pattern 9a, respectively, the power source through-hole conductor 21b is electrically connected with the power source pattern 9b, and the signaling probe contact 21c is electrically connected with the signaling pattern

9c. In this manner, the probe contacts 3a are electrically connected with the GND pattern 9a through the tubular sockets 30a, the probe contact 3b is electrically connected with the power source through-hole conductor 21b through the tubular socket 30b, and the probe contact 3a, 3b, 3c is electrically connected with the signaling through-hole conductor 21c through the tubular socket 30c. As a result, a capacitor C is formed with the material of the printed board 20' as a dielectric between the GND pattern 9a and the power source pattern 9b to thereby bypass power source noises. It is thus to be appreciated that as is the case with the first embodiment described above, the second embodiment may also provide the advantages of not only preventing occurrences of the waveform distortions of the power source and the power source noises, but also avoiding the occurrence of impedance mismatching. It should be noted that an external capacitor may be connected in parallel with the capacitor C as required.

Fig. 5 is a sectional view illustrating in principle the configuration and electrical connections of the third embodiment of the IC socket according to the present invention. In this embodiment, in the first embodiment described above, a plurality of interstitial via holes or via holes 31 for electrically interconnecting the GND patterns 23 and 25 are formed at predetermined angular intervals around the signaling probe contact 3c for the purpose of providing for increasing the electrostatic capacitances between the signaling through-hole conductor 21c and the ground patterns 23, 25 without substantially reducing the distances d_2 and d_4 of the gaps

between the through-hole conductor 21c and the GND patterns 23, 25.

Usually, the IC socket 1 is provided with a number of signaling probe contacts 3c, so that a plurality of interstitial via holes or via holes 31 each for electrically interconnecting the corresponding GND patterns 23 and 25 are formed around each of all of the signaling probe contacts 3c. Of course, however, in some instances, such interstitial via holes or via holes 31 for electrically interconnecting the GND patterns 23 and 25 may need be formed around only a predetermined number of rather than all of the signaling probe contacts 3c. It should also be noted that the interstitial via holes or via holes 31 may be provided so as to electrically interconnecting the power source patterns 22 and 24 rather than the GND patterns 23 and 25 and may provide the similar effects. In this case as well, a plurality of interstitial via holes or via holes 31 each for electrically interconnecting the corresponding power source patterns 22 and 24 may be formed at predetermined angular intervals around every signaling probe contact 3c or alternatively, such interstitial via holes or via holes 31 may be formed around only a predetermined number of rather than all of the signaling probe contacts 3c.

Since it will be apparent to one skilled in the art that the configuration of this third embodiment may provide the functional advantages equivalent to those obtained by the first embodiment, further detailed explanation is omitted. With the configuration of the first embodiment, however, the required electrostatic capacitances C_1 to C_4 could not be obtained unless

the gap distances d_2 , d_4 between the signaling through-hole conductor 21c and the ground patterns 23, 25 or the gap distances d_1 , d_3 between the signaling through-hole conductor 21c and the power source patterns 22, 24 were extremely reduced, in other words, unless the ground patterns 23, 25 or the power source patterns 22, 24 were located very close to the signaling through-hole conductor 21c. Consequently, the first embodiment would require very high precision of the operations or works of forming the GND patterns 23, 25 or the power source patterns 22, 24. In contrast, the configuration of the third embodiment provides increased electrostatic capacitances between the signaling probe contacts 3c and the via holes 31 in parallel to these probe contacts 3c so that it is not required to decrease the gap distances d_2 , d_4 between the signaling through-hole conductor 21c and the ground patterns 23, 25 or the gap distances d_1 , d_3 between the signaling through-hole conductor 21c and the power source patterns 22, 24. It is thus to be appreciated that the third embodiment provides the additional advantage of improving the manufacturing operation or working efficiency.

As will be appreciated from the foregoing discussion, the IC socket according to the present invention employs a multi-layer printed board having conductor layers comprising a GND pattern, a power source pattern and a signaling pattern laminated one on another at predetermined spacings by which a capacitor for bypassing power source noises is formed between the GND pattern and the power source pattern, and a low-pass filter (LPF) is constituted by this capacitor and parasitic inductances of the

power source probe contact, the band width of which may be set to be sufficiently broad. Accordingly, there are obtained advantages that occurrences of waveform distortions in the power source and the power source noises due to the parasitic inductances of the power source probe contact can be suppressed.

In addition, since the gap distances between the signaling through-hole conductors and the GND patterns, and between the signaling through-hole conductors and the power source patterns are set such that the characteristic impedance of the transmission line formed by the electrostatic capacitances across these gaps or the sum of these electrostatic capacitances plus the electrostatic capacitances brought by the via holes, and the parasitic inductances of the signaling probe contacts is equal to a predetermined value, an advantage is obtained that impedance matching with respect to the DUT and others can be achieved so that waveform distortions of a signal may be suppressed, leading to enhancement of the measuring accuracy.

Further, it will be readily understood that the present invention can be applied not only to IC sockets used in an IC tester but also to IC sockets in various types of apparatuses and devices, with which ICs are to be electrically contacted whereby similar functional effects can be obtained.

While the present invention has been described with regard to the embodiments shown by way of example, it will be apparent to those skilled in the art that various modifications, alterations, changes, and/or minor improvements of the embodiments can be made without departing from the spirit and the technical scope of the present invention. Accordingly, it

should be understood that the present invention is not limited to the embodiments shown and described above, and is intended to encompass all such various modifications, alterations, changes, and/or minor improvements falling within the scope of the
5 invention defined by the appended claims.



WHAT IS CLAIMED IS:

1. An IC socket comprising:

a multi-layer printed board having at least two conductor layers including a ground conductor layer and a power source conductor layer laminated one on another at a predetermined spacing and having a plurality of through-holes vertically formed therethrough;

through-hole conductors formed in all of said through-holes of said multi-layer printed board, said through-hole conductors including a ground through-hole conductor electrically connected with said ground conductor layer, a power source through-hole conductor electrically connected with said power source conductor layer, and a signaling through-hole conductor connected with none of said conductor layers; and

probe contacts attached to said respective through-hole conductors and adapted to be electrically contacted with terminals of an IC under test,

said IC socket being constructed such that a capacitance is produced, with the material of said multi-layer printed board as a dielectric, between said ground conductor layer and said power source conductor layer so as to bypass power source noises.

2. The IC socket as set forth in claim 1, wherein a plurality of said ground through-hole conductor are formed.

3. The IC socket as set forth in claim 1, wherein said multi-layer printed board is formed with a plurality of said



grounding through-hole conductor, at least one of which has none of said probe contacts attached thereto.

4. The IC socket as set forth in any one of claims 1 to 3, wherein distances of gaps between said signaling through-hole conductor and said ground conductor layer, and between said signaling through-hole conductor and said power source conductor layer are set such that the characteristic impedance of the transmission line formed by electrostatic capacitances across said gaps and a parasitic inductance of the probe contact is equal to a predetermined value.

5. The IC socket as set forth in any one of claims 1 to 3, wherein said IC under test is a BGA-IC (Ball Grid Array type Integrated Circuit), each of said probe contacts is formed at one end on the side of said IC under test with a contact to be contacted with the corresponding ball-like terminal of said BGA-IC and at the opposite end with a pin contact to be contacted with the corresponding land formed on the surface of a socket board on which said IC socket is to be placed.

6. The IC socket as set forth in any one of claims 1 to 3, wherein said multi-layer printed board has at least four conductor layers embedded therein including ground conductor layers and power source conductor layers alternately laminated one on another at predetermined spacings, whereby capacitances are produced, with the material of said multi-layer printed board as a dielectric, between each pair of said adjacent two ground



conductor layer and power source conductor layer.

7. The IC socket as set forth in any one of claims 1 to 3, wherein said multi-layer printed board has at least four conductor layers embedded therein including ground conductor layers and power source conductor layers alternately laminated one on another at predetermined spacings, and an interstitial via hole or a via hole for electrically interconnecting two ground conductor layers or two power source conductor layers is formed around said signaling through-hole conductor.

8. The IC socket as set forth in claim 7, wherein distances of gaps between said signaling through-hole conductor and said ground conductor layers, and between said signaling through-hole conductor and said power source conductor layers are set such that the characteristic impedance of the transmission line formed by the sum of electrostatic capacitances across these gaps plus an electrostatic capacitance produced between said signaling through-hole conductor and said interstitial via hole or via hole, and a parasitic inductance of the probe contact is equal to a predetermined value.

9. An IC socket comprising:

a multi-layer printed board having a ground conductor layer, a power source conductor layer and a signaling conductor layer laminated one on another at predetermined spacings and having a plurality of through-holes vertically formed therethrough;



through-hole conductors formed in all of said through-holes of said multi-layer printed board, said through-hole conductors including a ground through-hole conductor electrically connected with said ground conductor layer, a power source through-hole conductor electrically connected with said power source conductor layer, and a signaling through-hole conductor connected with said signaling conductor layer;

tubular sockets attached to said respective through-hole conductors; and

probe contacts fitted in said respective tubular sockets and adapted to be electrically contacted with terminals of an IC under test,

said IC socket being constructed such that a capacitance is produced, with the material of said multi-layer printed board as a dielectric, between said ground conductor layer and said power source conductor layer so as to bypass power source noises.

10. The IC socket as set forth in claim 9, wherein a plurality of said ground through-hole conductor are formed.

11. The IC socket as set forth in claim 9, wherein said multi-layer printed board is formed with a plurality of said ground through-hole conductor, at least one of which has none of said probe contacts attached thereto.

12. The IC socket as set forth in any one of claims 9 to 11, wherein distances of gaps between said signaling through-hole conductor and said ground conductor layer, and between said



signaling through-hole conductor and said power source conductor layer are set such that the characteristic impedance of the transmission line formed by electrostatic capacitances across these gaps and a parasitic inductance of said probe contact is equal to a predetermined value.

13. The IC socket as set forth in any one of claims 9 to 11, wherein said IC under test is a BGA-IC, each of said probe contacts is formed at one end on the side of said IC under test with a contact to be contacted with the corresponding ball-like terminal of said BGA-IC, and said multi-layer printed board has external connecting lands formed on at least one side surface thereof, said lands being electrically connected with said ground conductor layer, said power source conductor layer and said signaling conductor layer, respectively.