

DEVICE FOR COMPARING DATA IN A CONTENT-ADDRESSABLE
MEMORY ON SeOI

FIELD OF THE INVENTION

The field of the invention is that of semiconductor devices, and more particularly that of content-addressable memories produced on a semiconductor-on-insulator substrate (SeOI substrate).

5 The invention relates more specifically to a device for comparing data in a content-addressable memory, to a method for controlling such a comparison device and to a content-addressable memory.

BACKGROUND OF THE INVENTION

10 The content-addressable memory (CAM) is a type of computer memory used in certain very high speed search applications.

Unlike standard computer memories (of the random access memory RAM type, in particular) for which the user application supplies a memory address and the RAM returns the data stored at that address, a CAM
15 memory is designed so that the user application supplies a data word and the CAM searches throughout its memory to determine whether this word is stored therein. If the word is found, the CAM returns a list of one or more addresses where the word has been found.

Because a CAM memory is designed to search throughout its memory
20 in a single operation by performing multiple operations in parallel, this memory is faster than RAM in all search applications. However, unlike the RAM which has simple storage cells (the single function of a RAM is to store data), the CAM must also handle the comparison function. Each individual memory cell must thus have its own comparison circuit to detect a match
25 between the bit stored in the cell and a proposed input bit. The physical size of a CAM cell (particularly in terms of surface units occupied) is therefore greater than that of a RAM cell.

Figure 1 shows a conventional NOR-type CAM cell. Such a cell comprises ten transistors and typically occupies approximately 300 surface
30 units (300 F²).

A CAM memory of this type is said to be binary in that it uses the systematic search for data containing only 1s and 0s. Also known is a ternary

CAM memory allowing for a third state of correspondence called "X" or "any" for one or more bits in the stored data word, so that flexibility can be added to the search.

Figure 2 shows a conventional NOR-type ternary CAM cell. This cell
5 consists of 16 transistors and typically occupies 500 surface units.

It will have been understood that a conventional CAM cell thus occupies a large surface area. That said, there is a recurrent need in the field of application of the invention for miniaturization of the semiconductor devices. Moreover, merely because of the large number of transistors and the need to
10 supply a power supply line in the CAM memory array, a conventional CAM memory has the drawback of consuming a lot of power.

BRIEF DESCRIPTION OF THE INVENTION

The aim of the invention is to remedy the abovementioned drawbacks,
15 and, to this end, it proposes, according to a first aspect, a device for comparing data in a content-addressable memory, comprising:

- a memory cell formed by a first transistor storing a data bit and a second transistor storing the complement of the data bit, the transistors being produced on a semiconductor-on-insulator substrate and each of the
20 transistors having a front control gate and a back control gate that can be controlled to block the transistor;
- a comparison circuit configured to:
 - o operate the first and second transistors in read mode by applying to the front control gate of each of the transistors a nominal read voltage while controlling the back control gate of each of the transistors, one
25 with the proposed bit, the other with the complement of the proposed bit to block the passing transistor among said transistors if the proposed bit and the stored bit correspond; and
 - o detect the presence or absence of current on a source line linked to the source of each of the transistors to indicate whether the proposed
30 bit and the stored bit are identical or not.

Some preferred, but nonlimiting, aspects of this device are as follows:

- the comparison circuit is configured to supply the back control gate of the first transistor with the complement of a proposed bit and to supply the back control gate of the second transistor with the proposed bit;
- 5 – the semiconductor-on-insulator substrate comprises a thin film of semiconductive material separated from a base substrate by an insulating layer, and the back control gate of a transistor is arranged in the base substrate under the insulating layer facing the channel of said transistor;
- the back control gate of each of the transistors is isolated in the base
10 substrate by a well of opposite bias;
- the back control gate of each of the transistors has a working function;
- the comparison circuit is also configured to perform a ternary operation during which the proposed bit is disregarded;
- during a ternary operation, the comparison circuit operates the first and
15 the second transistors in read mode while controlling the back control gate of each of the transistors with one and the same voltage chosen so as to block the normally passing transistor;
- it also comprises a circuit for controlling the memory cell configured to operate the transistors in read, programming and erase modes by controlling
20 the back control gate of each of the transistors with one and the same voltage chosen so that the passing transistor is not blocked;
- the control circuit is also configured to operate the transistors in a holding mode by controlling the back control gate of each of the transistors with one and the same voltage chosen so that the passing transistor is
25 blocked;
- the device comprises two parallel back gate lines, each of the back gate lines being linked to the back control gate of one of the transistors;
- a word line links the front control gates of the transistors, the word line being perpendicular to the back gate lines;

- the transistors are floating gate FET transistors, and the back control gate of a transistor is arranged in the base substrate, being separated from the channel of said transistor by the insulating layer;

- the transistors are floating channel FET transistors, and the back control gate of a transistor is arranged in the base substrate, being separated from the channel of said transistor by the insulating layer.

According to another aspect, the invention relates to a content-addressable memory cell comprising a first transistor designed to store a data bit and a second transistor designed to store the complement of the data bit, the transistors being produced on a semiconductor-on-insulator substrate and each of the transistors having a source, a drain, a front control gate and a back control gate that can be controlled to block the transistor, in which cell a source line is linked to the source of each of the transistors, a back gate line is associated with the back control gate of each of the transistors, the back gate lines being parallel with one another and perpendicular to the source line.

A word line parallel to the source line can also be linked to the front control gate of each of the transistors.

According to yet another aspect, the invention relates to a memory array comprising a plurality of memory cells according to the invention.

According to yet another aspect, the invention relates to a method of comparing data in a content-addressable memory, the memory comprising a memory cell formed by a first transistor storing a data bit and a second transistor storing the complement of the data bit, the transistors being produced on a semiconductor-on-insulator substrate and each of the transistors having a front control gate and a back control gate that can be controlled to block the transistor, the method comprising steps consisting in:

- operating the first and second transistors in read mode by applying to the front control gate of each of the transistors a nominal read voltage, while controlling the back control gate of each of the transistors, one with the proposed bit, the other with the complement of a proposed bit,

to block the passing transistor among said transistors if the proposed bit and the stored bit correspond;

- detecting the presence or absence of current on a source line linked to the source of each of the transistors to indicate whether the proposed bit and the stored bit are identical or not.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, aims and advantages of the present invention will become more apparent from reading the following detailed description of preferred embodiments thereof, given as nonlimiting examples, and with reference to the appended drawings in which:

- Figures 1 and 2, already discussed previously, represent conventional NOR-type CAM cells, respectively binary and ternary, in which the access transistors are not shown in the interests of clarity;
- Figure 3 is a diagram representing one possible embodiment of a CAM memory cell with two transistors according to the invention;
- Figure 4 shows a preferential topology of a CAM memory array according to the invention;
- Figure 5 shows an equivalent diagram of a CAM memory cell according to the invention;
- Figures 6-8 illustrate a comparison operation between a proposed 4-bit word and a word stored in 4 CAM memory cells according to the invention, in the respective cases of a match between the proposed word and the stored word, a non-match between the proposed word and the stored word and a non-search for a match for one of the bits of the proposed word.
- Figures 9a and 9b represent two possible embodiments of a flash-type transistor that can be used in a CAM memory according to the invention;
- Figures 10a-10e represent various possible embodiments of a back control gate.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates, according to a first aspect, to a device for comparing data in a content-addressable memory comprising a memory cell storing a data bit BIT and a comparison circuit configured to detect whether a proposed bit DATA is identical to the stored bit BIT.

Referring to Figure 3, one possible embodiment of a memory cell is shown, used in a device for comparing data according to the first aspect of the invention.

The memory cell comprises two transistors: a first transistor T1 stores the data bit BIT and the second transistor T2 stores the complement of the data bit BITb. One of the transistors is thus normally passing (the one storing the logic "0" value), whereas the other is normally blocked (the one storing the logic "1" value).

The transistors are produced on a semiconductor-on-insulator substrate and each of the transistors has a front control gate CG and a back control gate BG1, BG2 that can be controlled to block the transistor.

The semiconductor-on-insulator substrate comprises a thin film of semiconductive material separated from a base substrate by an insulating layer. The semiconductor-on-insulator substrate is, for example, a silicon-on-insulator SOI substrate.

According to a preferred embodiment, the insulating layer is a buried oxide layer (BOX). The insulating layer is, for example, made of SiO₂.

Each transistor T1, T2 has a source region S, a drain region D and a channel C extending between the source region and the drain region.

The front control gate CG extends in a manner conventionally known per se on the surface of the substrate, above the channel C. In the context of the invention, the back control gate BG1, BG2 of a transistor is arranged in the base substrate under the insulating layer BOX facing the channel of said transistor. The back control gate is typically produced by dopant implantation under the insulating layer.

The drain D and source S regions are preferentially in contact with the insulating layer BOX so that the transistor is fully depleted.

The source S can thus be shared between two adjacent memory cells (see the two adjacent cells C1 and C2 in Figure 4). Such sharing makes it possible to reduce the surface area occupied by a memory cell.

It will be understood that the invention is not limited to a fully depleted memory cell but also extends to a memory cell on partially depleted SeOI. In a manner known conventionally per se, it is then necessary to isolate the cells along a line of the memory array in order to isolate the channels of adjacent cells from one another. This is conventionally done by the use of lateral isolating trenches (using the STI - Shallow Trench Isolation - technique) extending depthwise from the surface of the substrate to the BOX.

According to a preferential embodiment of the invention, the memory cell is formed by two floating gate flash transistors.

According to a first variant represented in Figure 9a, the flash transistors are planar: the floating gate 12 is arranged on the surface of the thin film of the SeOI substrate and is insulated from the channel C which extends in the thin film via a gate dielectric layer 13. The front control gate 10 is formed above the floating gate 12 while being insulated therefrom by an inter-gate dielectric layer 11.

According to a second variant represented in Figure 9b, the flash transistors are of the recessed floating gate type: the floating gate 22 is formed in a trench made in the channel C, and insulated from the channel via a gate dielectric layer 23 arranged on the walls of the trench. The front control gate 20 is formed on the surface of the substrate while being insulated from the floating gate 22 by an inter-gate dielectric layer 21.

The invention is not, however, limited to the use of flash transistors, but also extends to the use of DRAM on SeOI with floating gate transistors. According to a preferential variant, the front control gate of the DRAM transistors is recessed in the floating channel so as to increase its apparent

length, while being insulated from the channel by a gate dielectric layer. RCAT (Recess Channel Array Transistor) type transistors are thus defined.

On the left of Figure 3 there is a plan view of a CAM cell with two transistors T1, T2 (in this case, of flash type with recessed floating gate) according to the invention with the various access or control lines in the various regions of the transistors: source line SL linking the source regions S of each of the transistors, bit lines BL1, BL2 for addressing the drain region of each of the transistors, word line WL linking the front control gate of each of the transistors, back gate lines BG1, BG2 for addressing the back control gate of each of the transistors.

On the right of Figure 3 there is a cross-sectional view along the axis AA' of the transistor T1 illustrating the arrangement of the various source S, drain D and channel C regions of the front control gate CG and of the back control gate BG1 and of the various access lines BL1, WL, SL.

The active regions of the two transistors are arranged along two parallel strips. A word line WL is linked to the front control gate CG of each of the transistors, while a source line SL is linked to the source S of each of the two transistors.

The word line WL and the source line SL are perpendicular to the active region strips, while the drain of each transistor is addressed by a bit line BL1, BL2.

The back control gates BG1, BG2 are parallel to the bit lines. They are thus perpendicular to the source line SL which makes it possible to compare in parallel all the bits of one and the same proposed word (the source line is in fact common to all the bits of a stored word). They are also thus perpendicular to the word line WL which makes it possible to compare simultaneously the proposed word with several stored words on different rows (selective comparison by selection of a row via the corresponding word line WL).

The data comparison device according to the first aspect also comprises a comparison circuit (not represented) configured to operate the

first and second transistors in read mode by applying to the front control gate of the transistors a nominal read voltage, while controlling the back control gate of each of the transistors, one with a proposed bit DATA, the other with the complement DATA_b of the proposed bit so as to block the passing transistor among said transistors if the proposed bit and the stored bit match.

Thus, the back control gate of the normally passing transistor (the one storing the logic "1" value) is acted upon to block it in read mode if BIT and DATA match, and leave it passing if BIT and DATA do not match.

A transistor whose channel has an N-type conductivity and a back control gate of P conductivity (the back control gate is then said to have a working function) has a very high threshold voltage. This threshold voltage can be reduced by applying a positive voltage to the back control gate.

A transistor whose channel has an N-type conductivity and a back control gate of N conductivity (the back control gate is then said to be without working function) has a nominal threshold voltage that can be reduced by applying a positive voltage to the back control gate.

This variation of the threshold voltage of the transistor via the back control gate can be formulated according to $V_{th} = V_{t0} - \alpha \cdot V_{BG}$, in which V_{th} represents the threshold voltage of the transistor, V_{BG} the voltage applied to the back gate, V_{t0} the nominal threshold voltage (which may be offset by the working function depending on whether an N- or P-type back control gate is used), and α a coefficient linked to the geometry of the transistor.

The coefficient α can notably be modelled according to $\alpha = \frac{3 \cdot t_{ox1}}{t_{Si} + 3 \cdot t_{ox2}}$,

in which t_{ox1} designates the thickness of the gate dielectric layer separating the front control gate from the channel, t_{ox2} designates the thickness of the insulating layer separating the back control gate from the channel and t_{Si} designates the thickness of the thin film.

As an example, the thickness of the gate dielectric layer t_{ox1} is of the order of 15 Å or less for current or future technologies, the thickness of the

thin film t_{Si} is of the order of 25 Å or less, and the thickness of the insulating layer t_{ox2} is of the order of 50 Å or more.

It will be noted that, with a greater insulating layer thickness, it may be difficult to completely block a transistor via its back control gate. But it does, however, remain possible to detect its residual current so that the principle behind the invention can also be applied in such a situation.

In the context of the invention, a choice will preferentially be made to act with the working function so as to reduce the thickness, doping and other constraints on the transistor.

A choice is thus made to apply a zero voltage to the back control gate of a normally passing transistor in order to block it (the back control gate is then OFF). The threshold voltage of the transistor is effectively then very high.

The application of a positive voltage to the control gate of a transistor (the back control gate is then ON) reduces the threshold voltage of the transistor, so that a normally passing transistor will not be blocked by the back control gate.

This means that the complement DATA_b of the proposed bit must be applied to the back control gate of the first transistor storing the data bit BIT, and the proposed bit DATA must be applied to the back control gate of the second transistor storing the complement BIT_b of the data bit.

Thus, if BIT = 1, the back control gate of the first transistor is:

- OFF if BIT and DATA match, so that this transistor is then blocked and delivers no current,
- ON if BIT and DATA do not match, so that this transistor remains passing and delivers current.

It will be understood that the invention is not limited to the use of the working function, but extends to the case without working function. The invention is not moreover limited to the use of a zero or positive back control gate voltage but also extends to the use of a zero or negative back control gate voltage.

Various possible embodiments of a back control gate are detailed with reference to Figures 10a–10e. It will be noted that, in these figures, only the part that extends below the insulating layer is represented. Generally, the back control gate is formed by dopant implantation under the insulating layer.

5 According to a first embodiment represented in Figures 10c and 10e, the back control gate BG extends under the entire width of the cell.

 According to another embodiment represented in Figures 10a, 10b and 10d, the back control gate BG is located so as to extend only facing the floating channel (DRAM case) or the floating gate (Flash case).

10 As represented in Figure 10a, the back control gate BG is insulated from the base substrate 1 by a well W of opposite bias (N-type well for a P+ back control gate with working function for an N-type transistor).

 The well voltage is chosen so that the parasitic diode created by the electrical node between the back control gate and the well is always
15 reversed, the diode isolating the back control gate from the well and from anything that it might contain (other back control gates in particular).

 In the case where the back control gate extends under the entire width of the cell, it is also necessary to provide lateral insulating regions 20
20 extending depthwise into the base substrate 1 so as to insulate the back control gate from the base substrate. In Figure 10c, the lateral insulating regions 20 are buried under the insulating layer BOX. In Figure 10e, the lateral insulating regions 20 extend from the surface, through the insulating layer BOX.

 Such lateral insulating regions 20 can also be provided when the back
25 control gate is localized by thus contributing to the insulation of the wells. In particular, it may in this case be necessary to produce wells only for a single back control gate bias (for example N- well for insulating P+ back control gate whereas an N+ back control gate would be arranged directly in the P-biased base substrate). In Figure 10b, the lateral insulating regions 20 are
30 buried under the insulating layer BOX. In Figure 10d, the lateral insulating regions 20 extend from the surface through the insulating layer BOX.

According to a variant embodiment not represented, a second insulating layer, arranged in the base substrate below the insulating layer BOX, can contribute, wholly or partly, to the insulation of a back control gate from the base substrate.

5 Returning to the description of the data comparison device according to the first aspect of the invention, the comparison circuit is also configured to detect the presence or the absence of current on the source line SL linked to the source of each of the transistors to indicate whether the proposed bit DATA and the data bit BIT are identical or not. More specifically, the absence
10 of current signifies a match between BIT and DATA (the passing transistor has indeed been blocked so that the cell with two transistors supplies no current to the source line), whereas the presence of current signifies that DATA is different from BIT (the passing transistor has not been blocked and the cell is supplying current to the source line).

15 It will be noted that, for the conventional CAM memories of Figures 1 and 2, a specific line (generally designated "match line") is provided to supply the result of the comparison. This line is different from earth. It also requires the production of interconnects, which is made possible by the relatively large size of the cell (10 or 16 transistors).

20 In the context of the invention, the source line (generally used as earth for the cells) is used as "match line".

This makes it possible to avoid having to produce interconnects, while the cell comprises only two transistors and therefore has a minimal footprint.

25 Moreover, the source line is parallel to the word line, and therefore common to all the bits of a stored word. It is thus possible to make a comparison between one (or more) stored word(s) and a proposed word, in parallel, over all the bits of the word.

30 Given that the electrical function of the source line in the cell is primarily to form the earth, the voltage of the source line is 0V (or as close as possible) in all circumstances to ensure correct operation of the cells. On the other hand, it is possible to measure the presence or the absence of current in this

line, the current being able to flow at any voltage, provided that the line has a relatively low impedance.

The presence of current on the source line may be due to any bit of the word, which corresponds to a difference between the stored word and the proposed word in the comparison. Only a perfect match of all the bits will induce an absence of current in the source line.

Figure 4 represents a preferential topology of a CAM memory array according to the invention. In this figure, the dotted lines identify adjacent CAM memory cells C1 and C2 as described previously. It will be noted that, advantageously, the source line SL is common to the two adjacent cells C1 and C2 along an active region strip (the cell C1 being addressed by the word line WL1, the cell C2 being addressed by the word line WL2). The selective activation of WL1 or WL2 thus makes it possible to compare a proposed bit with one or other of the bits stored in the cells C1 and C2.

On the right of Figure 5 is an equivalent circuit diagram of the CAM cell according to the invention.

In as much as each transistor has two control gates (a front control gate and a back control gate), each transistor functions as two transistors in series. The cell thus works like a cell with four transistors. The interest in using transistors that have a back control gate is that the latter are much smaller than two transistors in series.

Referring to Figure 6, this shows an exemplary comparison of a proposed word (comprising four bits: 0100) with a word stored in four CAM cells according to the invention arranged on one and the same line of a memory array such that the transistors of these cells share the same word line WL and the same source line SL.

When the proposed bit (DATA3-DATA2-DATA1-DATA0) is identical to the stored bit (BIT3-BIT2-BIT1-BIT0), no current flows on the source line SL.

Taking the example of the proposed bit DATA0=0, the first transistor of the cell stores BIT0=0, while the second transistor of the cell stores the complementary bit BIT0b=1. In normal read operation (via the application of

a nominal read voltage VDD to the word line WL, and a voltage of around VDD/2 to the bit line BL1, BL2 of each of the first and second transistors), the first transistor is blocked, while the second is passing. In the case of action with the working function, the comparison circuit according to the invention is
 5 configured to perform this normal read operation while applying the DATA_b value to the back control gate of the first transistor and the DATA value to the back control gate of the second transistor. The second transistor is then blocked by its back control gate (the latter is OFF because controlled by DATA₀=0). It follows from this that this cell delivers nothing to the source line
 10 SL.

If a perfect match is observed between all the bits of the proposed word and the stored bits, no current flows on the source line. It will be noted that there is no constraint on the width (number of bits) of the proposed word.

Referring to Figure 7, this shows the same exemplary comparison of a
 15 proposed word of 4 bits 0100. In this Figure 6, there is no match between the bit DATA₂=0 of the proposed word and the stored bit BIT₂=1.

Taking the example of the proposed bit DATA₂=0, the first transistor of the cell stores BIT₂=1, while the second transistor of the cell stores the complementary bit BIT_{2b}=0. In normal read operation, the first transistor is
 20 passing, while the second is blocked. The comparison circuit according to the invention is configured to perform this normal read operation while applying the DATA_b value to the back control gate of the first transistor and the DATA value to the back control gate of the second transistor. The first transistor then remains passing (its back control gate is ON because controlled with
 25 DATA_{2b}=1). This cell then delivers current to the source line SL. The presence of the current, which may be due to any bit of the word, thus corresponds to a difference between the proposed word and the stored word.

Referring to Figure 8, this shows a ternary comparison corresponding to a "don't care" situation on proposed bit DATA₁. For such a ternary
 30 comparison, the back control gates of the corresponding CAM cell (storing BIT₁) are forced to OFF, so that the passing transistor becomes blocked and

no current is then delivered to the source line. The comparison on the bit BIT1 has thus been blocked. Such a ternary comparison corresponds, for example, to a search on words that are incomplete or contain faults.

5 As a variant, the two transistors can be controlled for each to store a "0". The comparison on the bit is then blocked, no current being able to be delivered on the source line by this pair of transistors. Such a variant corresponds, for example, to a search in a database that may contain "spelling errors".

10 A comparison operation between a proposed bit and the bit stored in the CAM cell according to the invention has been described above.

The read, programming, erase and hold operations of this cell are described hereinbelow.

15 These operations run in a manner known conventionally per se with regard to the voltages to be applied to the front control gate and to the drain of each transistor.

With respect to the read, programming and erase modes, a control circuit also controls the back control gate of each of the transistors with one and the same voltage chosen such that the passing transistor is not blocked. In the example described here, the back control gate of each of the two
20 transistors is thus ON during these operations.

Although not mandatory, different operation can be provided for the hold mode, the control circuit then being configured to control the back control gate of each of the transistors with one and the same voltage chosen such that the passing transistor is blocked. In the example described here,
25 the back control gate of each of the two transistors would thus be OFF so as to reduce the power consumption during this hold operation.

A truth table for a CAM cell according to the invention is thus as follows.

DATA	DATA _b	BIT	BIT _b	MODE	
X	X	1	1	Prohibited (this mode is technically possible, but it is avoided because it would systematically create a non-match result in the comparison modes)	
1	1	-	-	Read, programming, erase	
0	0	-	-	Hold	
0	0	X	X	Comparison	Ternary "don't care"
X	X	0	0		Ternary "don't care"
0	1	0	1		Match
1	0	0	1		Non-match
0	1	1	0		Non-match
1	0	1	0		Match

It will have been understood that the invention is not limited to the comparison device according to its first aspect, but also extends to a content-addressable memory cell, to a method for comparing data in a content-addressable memory implementing the principles described hereinabove, and to a content-addressable memory comprising a plurality of cells with two transistors according to the invention arranged in lines and columns.

The invention offers the following particular advantages.

- Firstly, by limiting to two the number of transistors needed to fulfil the comparison function, the surface area occupied by the CAM cell is considerably reduced. Depending on the technological process used, the CAM cell of the invention occupies around 8 F² in memory process, at least 30 F² in logic process (to be compared with 300 F² for the conventional binary CAM cell, and with 500 F² for the conventional ternary CAM cell).
- Moreover, in the context of the invention, the same cell can be used to perform a binary comparison or a ternary comparison.
- The comparison speed is similar to that of the conventional cells.

- The CAM memory according to the invention does not need any power supply line so that neither leaks nor power losses are observed in the memory array.
 - The comparison is selected via the word line, which is not possible with the conventional cells. It is therefore possible to choose simply the number of words compared simultaneously without being constrained by the architecture of the memory circuit (size of the arrays in particular).
 - The CAM cell according to the invention operates at low power.
 - The CAM memory is relatively easy to design: it in effect comprises only long rectilinear regions for all the layers, the contacts being established according to regular arrays.
 - When the CAM cell according to the invention uses flash transistors, the initial programming is relatively slow compared to a CAM cell with SRAM transistors. However, the CAM cell according to the invention consumes less and has smaller dimensions. The CAM cell can also be used only for information that is infrequently addressed.
- When the CAM cell according to the invention uses DRAM transistors, a periodic refresh of the content is needed, but the programming is significantly faster than with flash transistors. This variant embodiment can advantageously be used to produce the memory buffers (usually called Caches L1, L2, L3) of a microprocessor.

CLAIMS

1. Device for comparing data in a content-addressable memory, comprising:
 - 5 - a memory cell formed by a first transistor (T1) storing a data bit (BIT) and a second transistor (T2) storing the complement of the data bit (BITb), the transistors being produced on a semiconductor-on-insulator substrate and each of the transistors having a front control gate (CG) and a back control gate (BG1, BG2) that can be controlled to block the transistor;
 - 10 - a comparison circuit configured to:
 - o operate the first and second transistors in read mode by applying to the front control gate of each of the transistors a nominal read voltage while controlling the back control gate of each of the transistors, one with the proposed bit (DATA), the other with the complement of the
15 proposed bit (DATAb) to block the passing transistor among said transistors if the proposed bit (DATA) and the stored bit (BIT) correspond; and
 - o detect the presence or absence of current on a source line (SL) linked to the source of each of the transistors to indicate whether the
20 proposed bit (DATA) and the stored bit (BIT) are identical or not.
2. Device according to Claim 1, in which the comparison circuit is configured to supply the back control gate (BG1) of the first transistor with the complement of a proposed bit (DATAb) and to supply the back control gate
25 (BG2) of the second transistor with the proposed bit (DATA).
3. Device according to one of the preceding claims, in which the semiconductor-on-insulator substrate comprises a thin film of semiconductive material separated from a base substrate by an insulating layer, and the back
30 control gate of a transistor is arranged in the base substrate under the insulating layer facing the channel of said transistor.

4. Device according to one of the preceding claims, in which the back control gate of each of the transistors is isolated in the base substrate by a well of opposite bias.
- 5 5. Device according to one of the preceding claims, in which the back control gate of each of the transistors has a working function.
6. Device according to one of the preceding claims, in which the comparison circuit is also configured to perform a ternary operation during which the
10 proposed bit is disregarded.
7. Device according to Claim 6, in which, during a ternary operation, the comparison circuit operates the first and the second transistors in read mode while controlling the back control gate of each of the transistors with one and
15 the same voltage chosen so as to block the normally passing transistor.
8. Device according to one of the preceding claims, also comprising a circuit for controlling the memory cell configured to operate the transistors in read, programming and erase modes by controlling the back control gate of each
20 of the transistors with one and the same voltage chosen so that the passing transistor is not blocked.
9. Device according to one of the preceding claims, also comprising a circuit for controlling the memory cell configured to operate the transistors in a
25 holding mode by controlling the back control gate of each of the transistors with one and the same voltage chosen so that the passing transistor is blocked.
10. Device according to one of the preceding claims, comprising two
30 parallel back gate lines, each of the back gate lines being linked to the back control gate of one of the transistors.

11. Device according to Claim 10, in which a word line links the front control gates of the transistors, the word line being perpendicular to the back gate lines.
- 5 12. Device according to one of Claims 1 to 11, in which the transistors are floating gate FET transistors, the semiconductor-on-insulator substrate comprises a thin film of semiconductive material separated from a base substrate by an insulating layer, and the back control gate of a transistor is arranged in the base substrate, being separated from the channel of said
10 transistor by the insulating layer.
13. Device according to one of Claims 1 to 11, in which the transistors are floating channel FET transistors, the semiconductor-on-insulator substrate comprises a thin film of semiconductive material separated from a base
15 substrate by an insulating layer, and the back control gate of a transistor is arranged in the base substrate, being separated from the channel of said transistor by the insulating layer.
14. Content-addressable memory cell comprising a first transistor (T1)
20 designed to store a data bit (BIT) and a second transistor (T2) designed to store the complement of the data bit (BITb), the transistors being produced on a semiconductor-on-insulator substrate and each of the transistors having a source, a drain, a front control gate (CG) and a back control gate (BG1, BG2) that can be controlled to block the transistor, in which cell a source line
25 (SL) is linked to the source of each of the transistors, a back gate line (BG1, BG2) is associated with the back control gate of each of the transistors, the back gate lines being parallel with one another and perpendicular to the source line.

15. Cell according to Claim 14, in which a word line (WL) is linked to the front control gate of each of the transistors, the word line being parallel to the source line.

5 16. Content-addressable memory comprising a plurality of memory cells according to one of Claims 14 or 15 arranged in lines and in columns.

17. Method of comparing data in a content-addressable memory, the memory comprising a memory cell formed by a first transistor storing a data bit (BIT) and a second transistor storing the complement of the data bit (BITb), the transistors being produced on a semiconductor-on-insulator substrate and each of the transistors having a front control gate and a back control gate that can be controlled to block the transistor, the method comprising steps consisting in:

- 15 – operating the first and second transistors in read mode by applying to the front control gate of each of the transistors a nominal read voltage, while controlling the back control gate of each of the transistors, one with the proposed bit (DATA), the other with the complement of a proposed bit (DATAb), to block the passing transistor among said
- 20 transistors if the proposed bit (DATA) and the stored bit (BIT) correspond;
- detecting the presence or absence of current on a source line linked to the source of each of the transistors to indicate whether the proposed bit (DATA) and the stored bit (BIT) are identical or not.

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