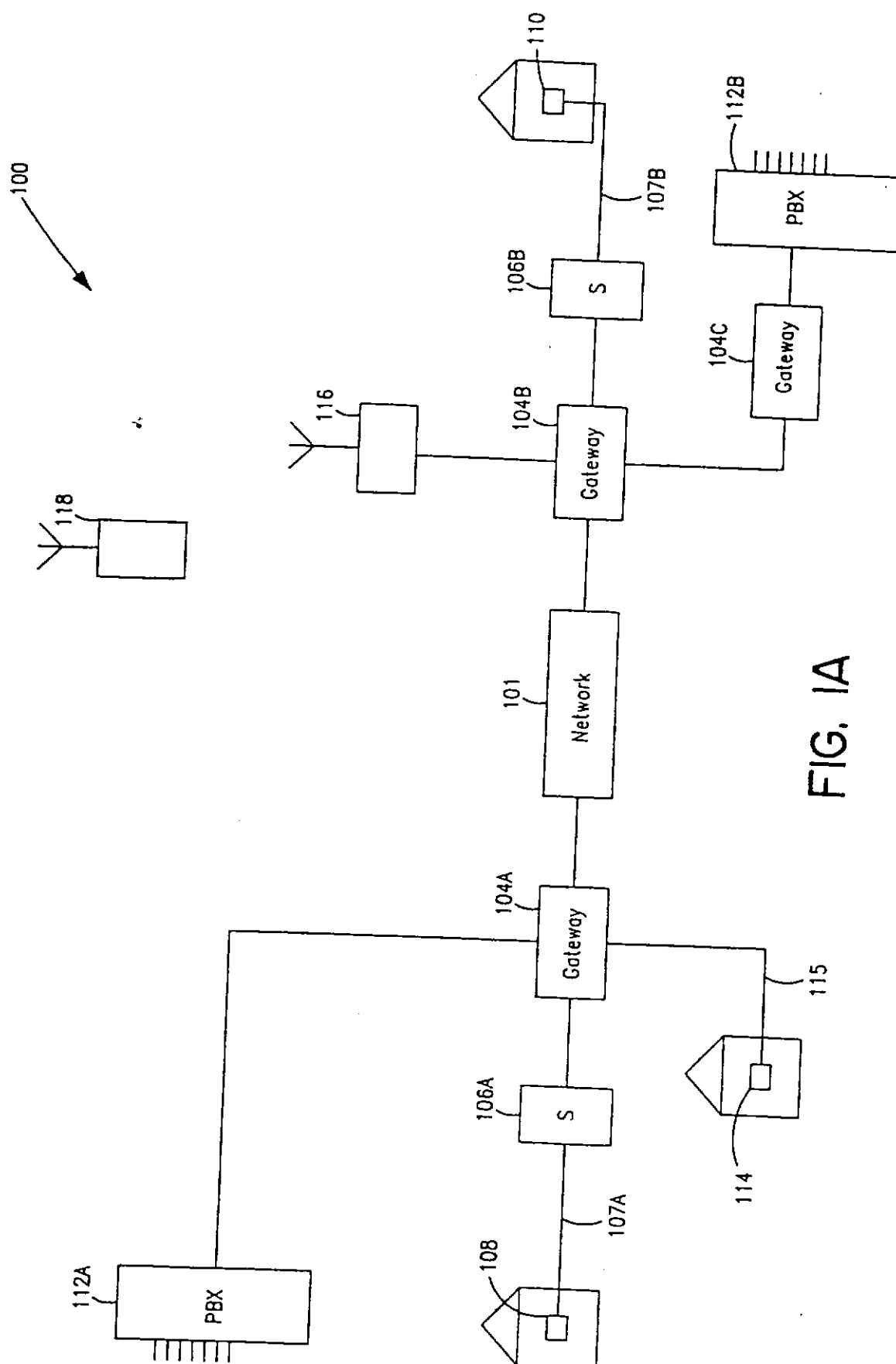




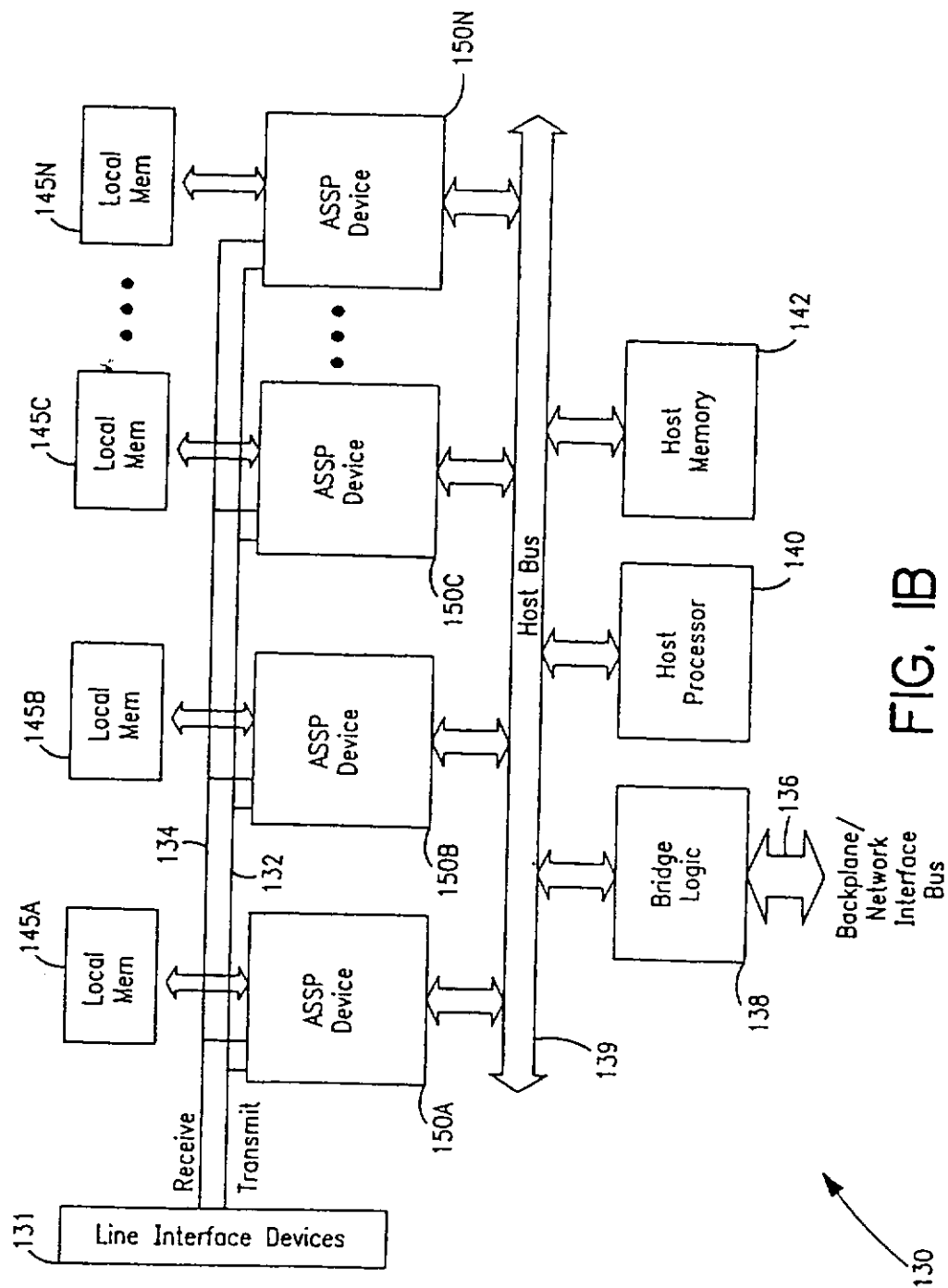


FIG. 1B

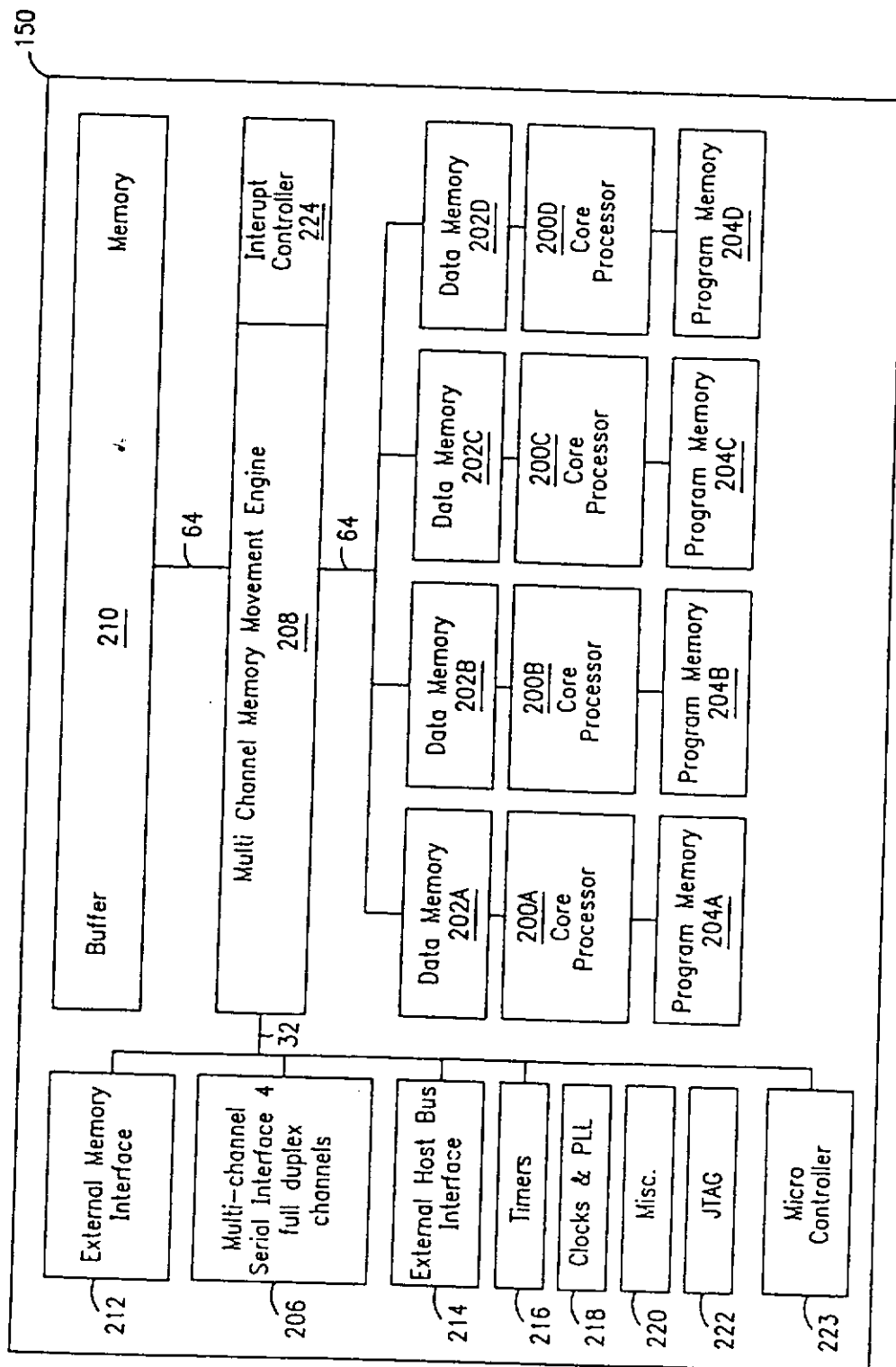


FIG. 2

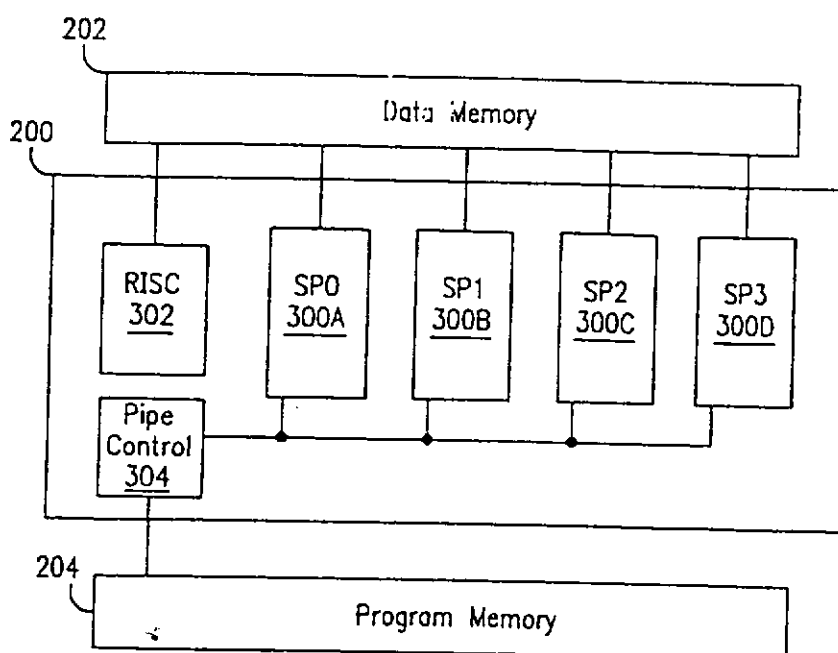


FIG. 3

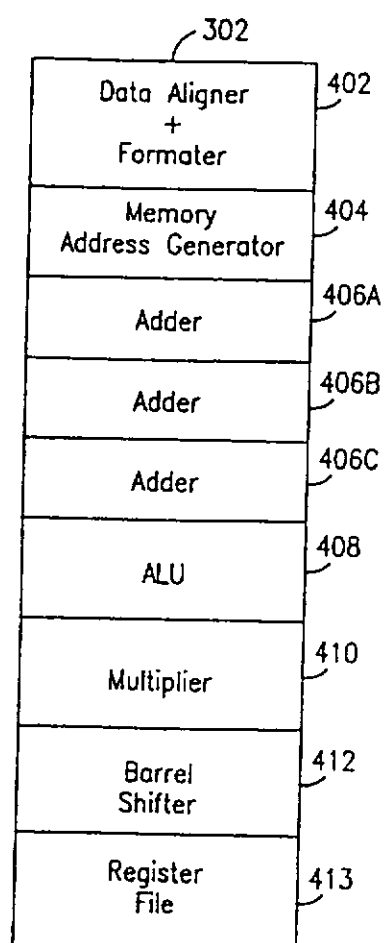


FIG. 4

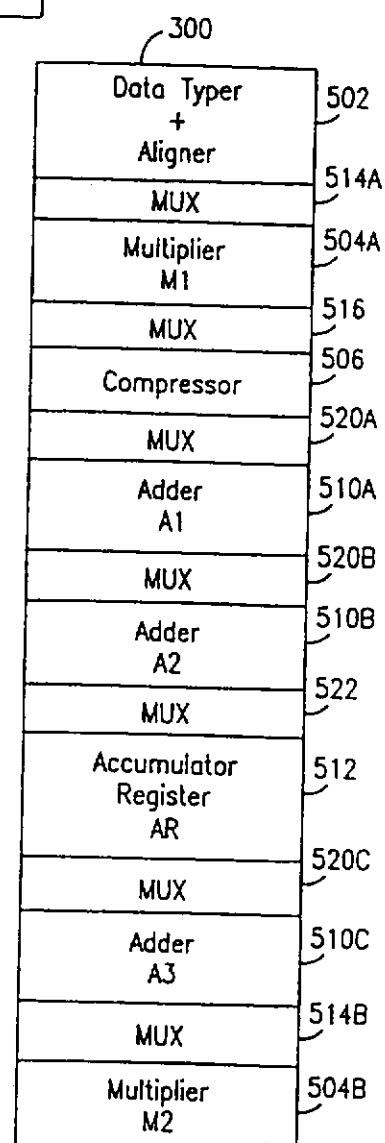


FIG. 5A

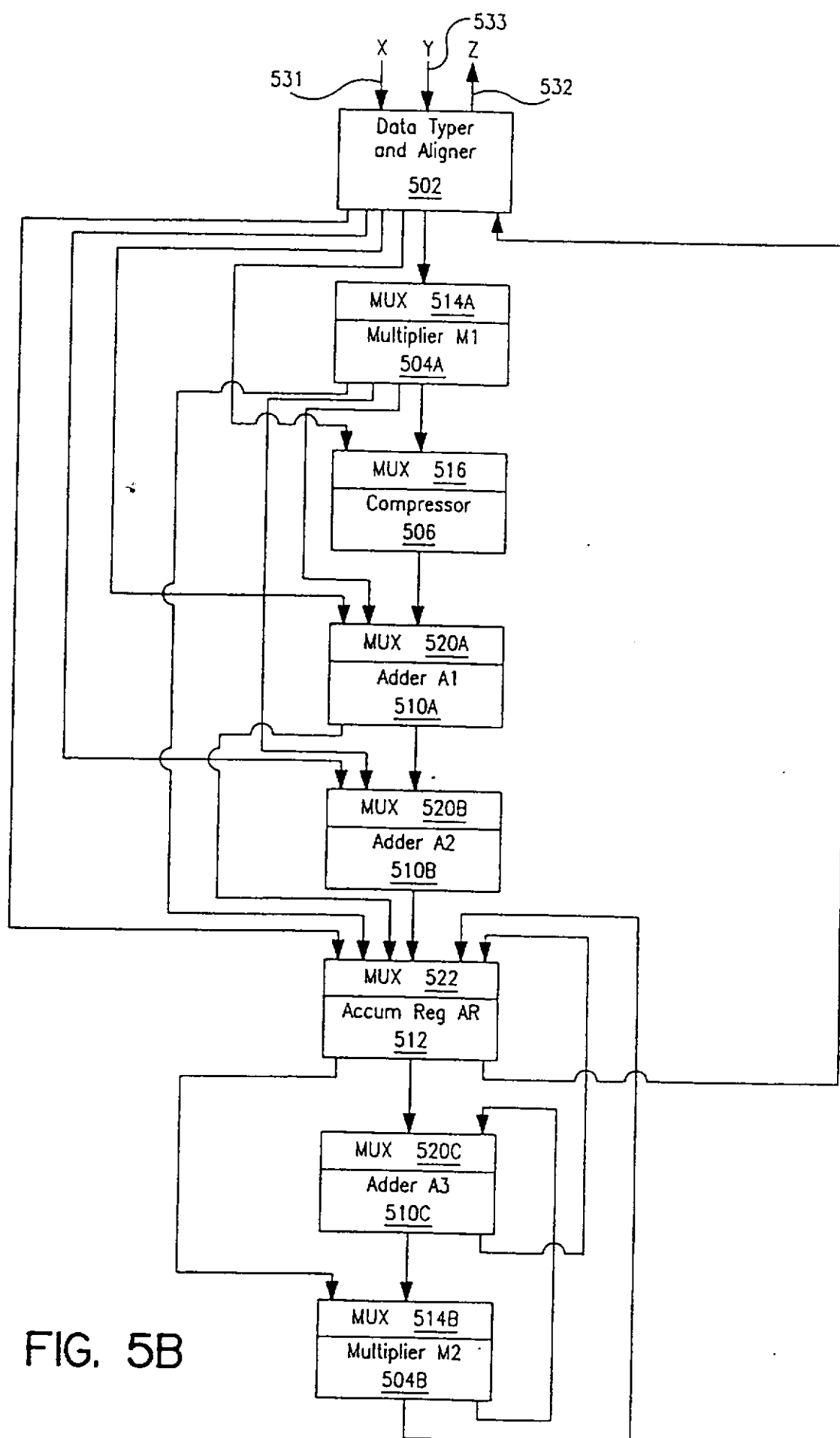


FIG. 5B

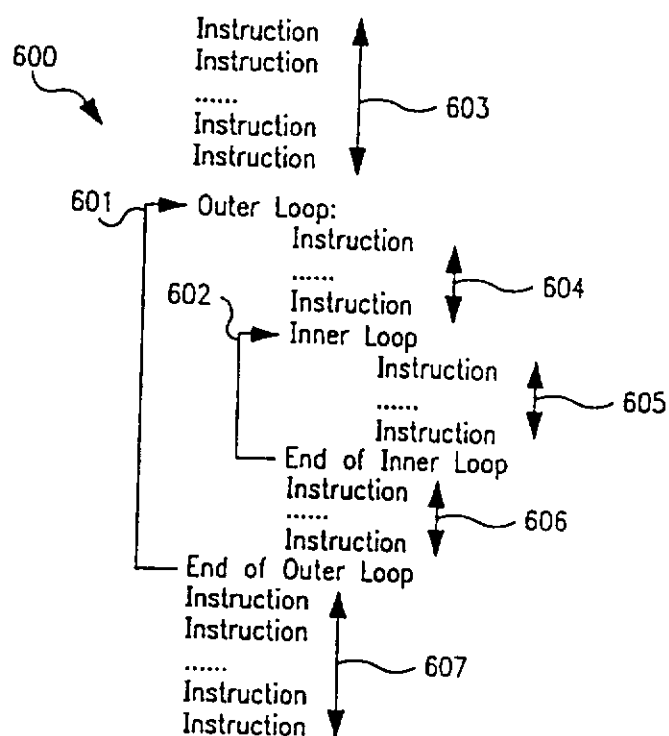


FIG. 6A

610	
611	612
MAIN OP	SUB OP
MULT	NOP
ADD	MIN/MAX
MIN/MAX	ADD
NOP	MULT

FIG. 6B

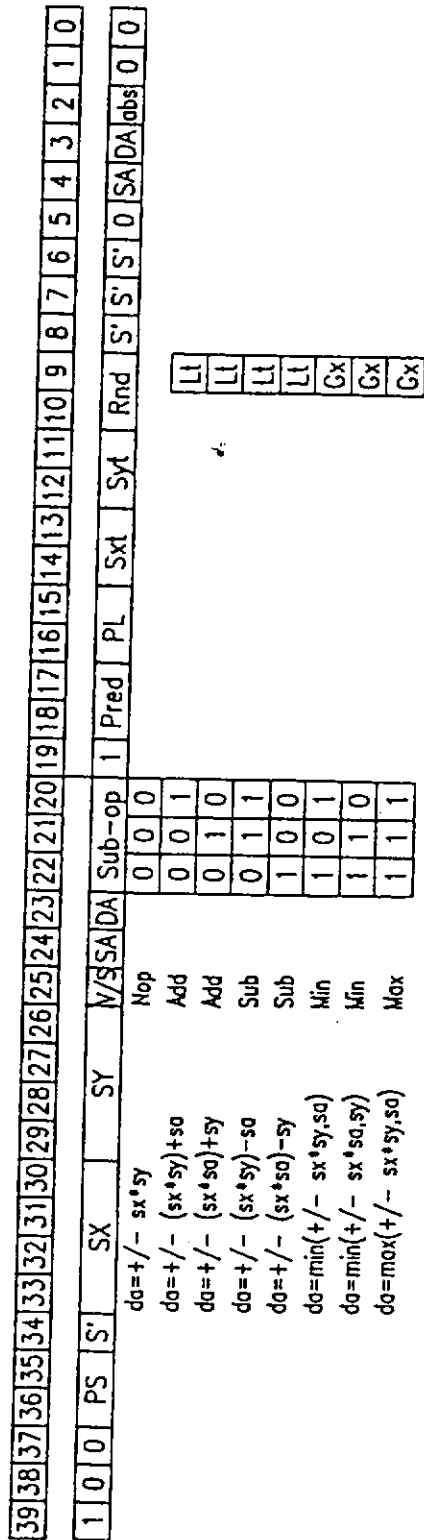


FIG. 6C

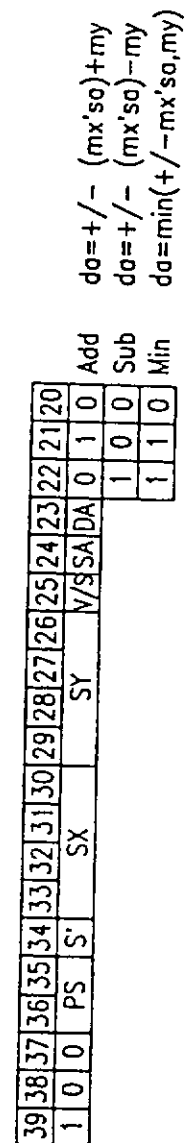


FIG. 6D

20-bit ISA

39	19
0	0
0	1
1	0
1	1

20-bit parallel
20-bit serial
40-bit extended
20-bit serial

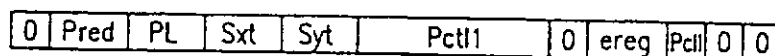
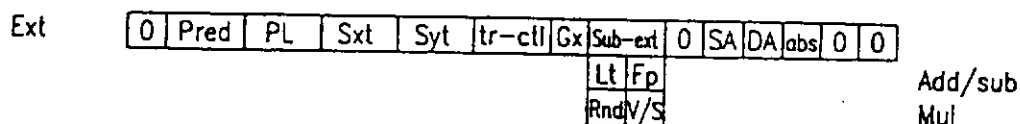
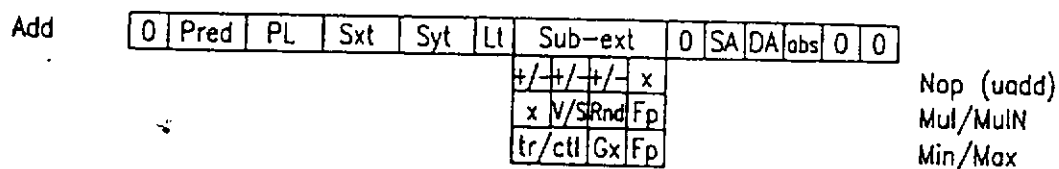
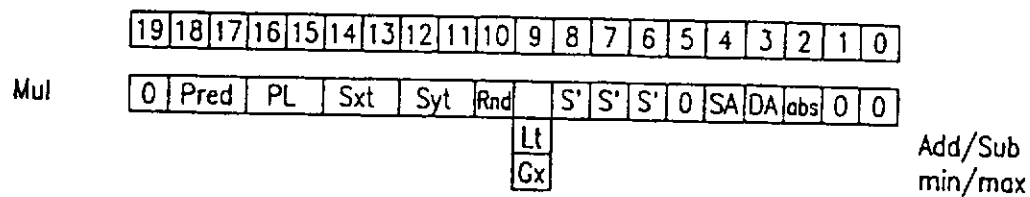
Control () Control
Control # Control
DSP extensions/Shadow
DSP # DSP

DSP instructions

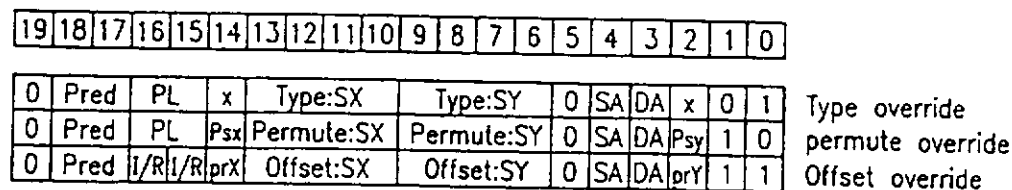
	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
Multiply	1	0	0	PS	S'	SX		SY		V/S	SA	DA	Sub-op							
													0	0	0					Nop
													0	0	1					Add
													0	1	0					Add
													0	1	1					Sub
													1	0	0					Sub
													1	0	1					Min
													1	1	0					Min
													1	1	1					Max
Add	1	0	1	PS	+/-	SX		SY		V/S	SA	DA	Sub-op							
													0	0	0					Nop
													0	0	1					Add
													0	1	0					AddSub
													0	1	1					Mul
													1	0	0					MulN
													1	0	1					Min
													1	1	0					Max
													1	1	1					CombAdd
Extremum	1	1	0	PS	x/n	SX		SY		V/S	SA	DA	Sub-op							
													0	0	0					Nop
													0	0	1					Ext
													0	1	0					Mul
													0	1	1					MulN
													1	0	0					Add
													1	0	1					Sub
													1	1	0					amax
type-match	1	1	0	PS	0	SX		SY		x	x	x	1	1	1					
Permute	1	1	0	PS	1	SX		Type		x	ereq		1	1	1					Permute
Reserved	1	1	1	PS	x	SX		SY		SA	DA	V/S	Sub-op							

FIG. 6E-1

Control and specifier Extensions



Type/offset/permute extensions



Shadow DSP

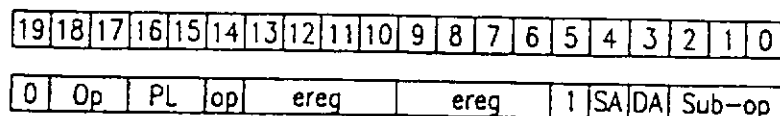


FIG. 6E-2

Control instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
add,sub	L	Pred	0	0	0			RX				RY					RZ		+/-	0	
max,min	L	Pred	0	0	0			RX				RY					RZ		X/N	1	
Shift	L	Pred	0	0	1			RX				UI4					RZ		UI2	R/L	<Bit1,Bits9-6>
Logic	L	Pred	0	1	0			RX				RY					RZ		&	&1	==UI5 (Shift Amount)
Mux	L	Pred	0	1	1			RX				RY					RZ		Pd	0	
mov	L	Pred	0	1	1			RX				DZ			Rxt	Dzt	0	0	0	1	
addi	L	Pred	0	1	1			SI4				DZ			x	x	1	0	0	1	
mov2erg	L	Pred	0	1	1			RX			unit	ereq			gd	type	1	0	1		
l.dm	L	Pred	0	1	1			RX				DZ1					DZ2		1	1	
Set4bits	L	Pred	1	0	0			UI4:POS				RZ			Rzt		UI4			0	
Set2bits	L	Pred	1	0	0			UI4:POS				RZ			Rzt	UI2	0	0	1		
Setbit	L	Pred	1	0	0			UI4:POS				RZ			Rzt	UI1	UI1	1	0	1	<Bit3,Bits13-10>==UI5 POS
Movi	L	Pred	1	0	0					SI8							RZ		1	1	
Jmp	L	Pred	1	0	1					SI9						0	PRED	0	0		
Call	L	Pred	1	0	1					SI9						1	PRED	0	0		
Loop	L	Pred	1	0	1			UI5:Lcount				UI5:Lsize					UI2:Lst	0	1		
Jmpi	L	Pred	1	0	1			RX		x	x	x	x	x	0		PRED	1	0		
Calli	L	Pred	1	0	1			RX		x	x	x	x	x	1		PRED	1	0		
Loopi	L	Pred	1	0	1			RX		x		UI5:Lsize					UI2:Lst	1	1		
Test	L	Pred	1	1	0			RX				RY					PZ		=,<,>	0	
Testbit	L	Pred	1	1	0			RX				UI5					PZ	B	0	1	
Andp, orp	L	Pred	1	1	0			Pa		Pb		Pc					PZ	&	1	1	
Load	L	Pred	1	1	1			MX				RZ					Ext	0	0	0	
Store	L	Pred	1	1	1			MZ				RZ					Ext	1	0	0	
eLoad	L	Pred	1	1	1			MX				RY			1	1	1	0	0	0	
eStore	L	Pred	1	1	1			MZ				RY			1	1	1	1	0	0	
Extended	L	Pred	1	1	1							Bits 27:16							1	0	
Logic2	L	Pred	1	1	1			RX				RY/RZ			Rxt	Ryt	&1,&1	0	1		
mov-erg	L	Pred	1	1	1			unit	ereq			RZ			gd	Sft	0	1	1		
Crb	L	Pred	1	1	1			RX				RZ			s/m	0	0	1	1	1	
Panty	L	Pred	1	1	1			RX				PZ	10/E	0	1	0	1	1	1	1	
Stm	L	Pred	1	1	1			MZ				RX			1	1	0	1	1	1	
Abs	L	Pred	1	1	1			RX				RZ			0	0	1	1	1	1	
Neg	L	Pred	1	1	1			RX				RZ			0	1	1	1	1	1	
Div-step	L	Pred	1	1	1			RX				RZ			1	0	1	1	1	1	
Test&Set	L	Pred	1	1	1			RX				PZ	0		1	1	1	1	1	1	
Reserved	L	Pred	1	1	1						0	0	1	1	1	1	1	1	1	1	
Return	L	Pred	1	1	1			Pred	1-ctl	0	1	0	1	1	1	1	1	1	1	1	
Zero-ac	L	Pred	1	1	1			ac #		1	1	0	1	1	1	1	1	1	1	1	
eSync	L	Pred	1	1	1			RZ		0	1	1	1	1	1	1	1	1	1	1	
Swi	L	Pred	1	1	1			UI3	0	1	1	1	1	1	1	1	1	1	1	1	
Nop	L	Pred	1	1	1			UI3	1	1	1	1	1	1	1	1	1	1	1	1	

FIG. 6F

Extended Control

Bits 13:2 of upper half (39:20)																			
13	12	11	10	9	8	7	6	5	4	3	2	19	18	17	16	15	14	13	12
Insert/Extract																			
RX												0	0	0	0	0	0	0	0
Inserti																			
UI4 length												0	0	0	0	0	0	0	0
RX												0	0	0	0	0	0	0	0
Shift																			
RZ												0	0	0	0	0	0	0	0
Rotate																			
RZ												0	0	0	0	0	0	0	0
jmp, call																			
UI7												0	0	0	0	0	0	0	0
UI4 outer LC												0	0	0	0	0	0	0	0
RX												0	0	0	0	0	0	0	0
dloopi																			
RZ												0	0	0	0	0	0	0	0
mult																			
RZ												0	0	0	0	0	0	0	0
add/sub																			
RZ												0	0	0	0	0	0	0	0
Reserved																			
RZ												0	0	0	0	0	0	0	0
logicp																			
RZ												0	0	0	0	0	0	0	0
Testi																			
RZ												0	0	0	0	0	0	0	0
Mov																			
RZ												0	0	0	0	0	0	0	0
loadi																			
RZ												0	0	0	0	0	0	0	0
storei																			
RZ												0	0	0	0	0	0	0	0
loadt																			
RZ												0	0	0	0	0	0	0	0
storet																			
RZ												0	0	0	0	0	0	0	0
Addi/subi																			
RZ												0	0	0	0	0	0	0	0
mini,maxi																			
RZ												0	0	0	0	0	0	0	0
andi,on																			
RZ												0	0	0	0	0	0	0	0

FIG. 6G

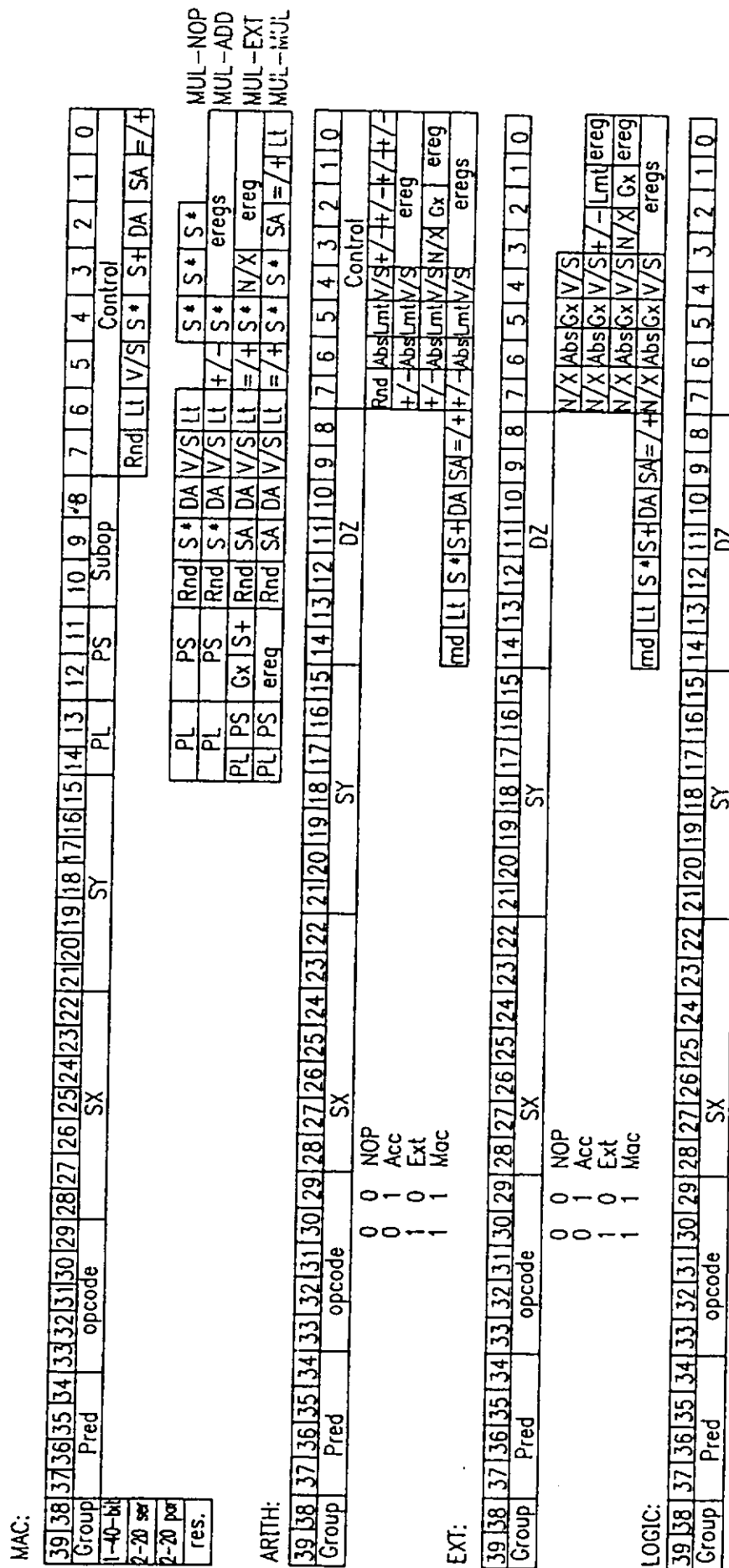


FIG. 6H-I

Misc:

FIG. 6H-2

ac-names

3	2	1	0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

A0 (use type, SIMD)

A1

T

TR

A00 (unit 0)

A10

T0

TR0

SX1

SX1s

SX2

SX2s

SY1

SY1s

SY2

SY2s

SPR:

gpr-type

ereg type

fu-ctl

pls-ctl

cb-ctl

loop-ctl

pcr

status

ereg names

3	2	1	0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

A0

A1

T

TR

PPO

Aout

PP1

Dout

SX1

SX1s

SX2

SX2s

SY1

SY1s

SY2

SY2s

FIG. 6I-2

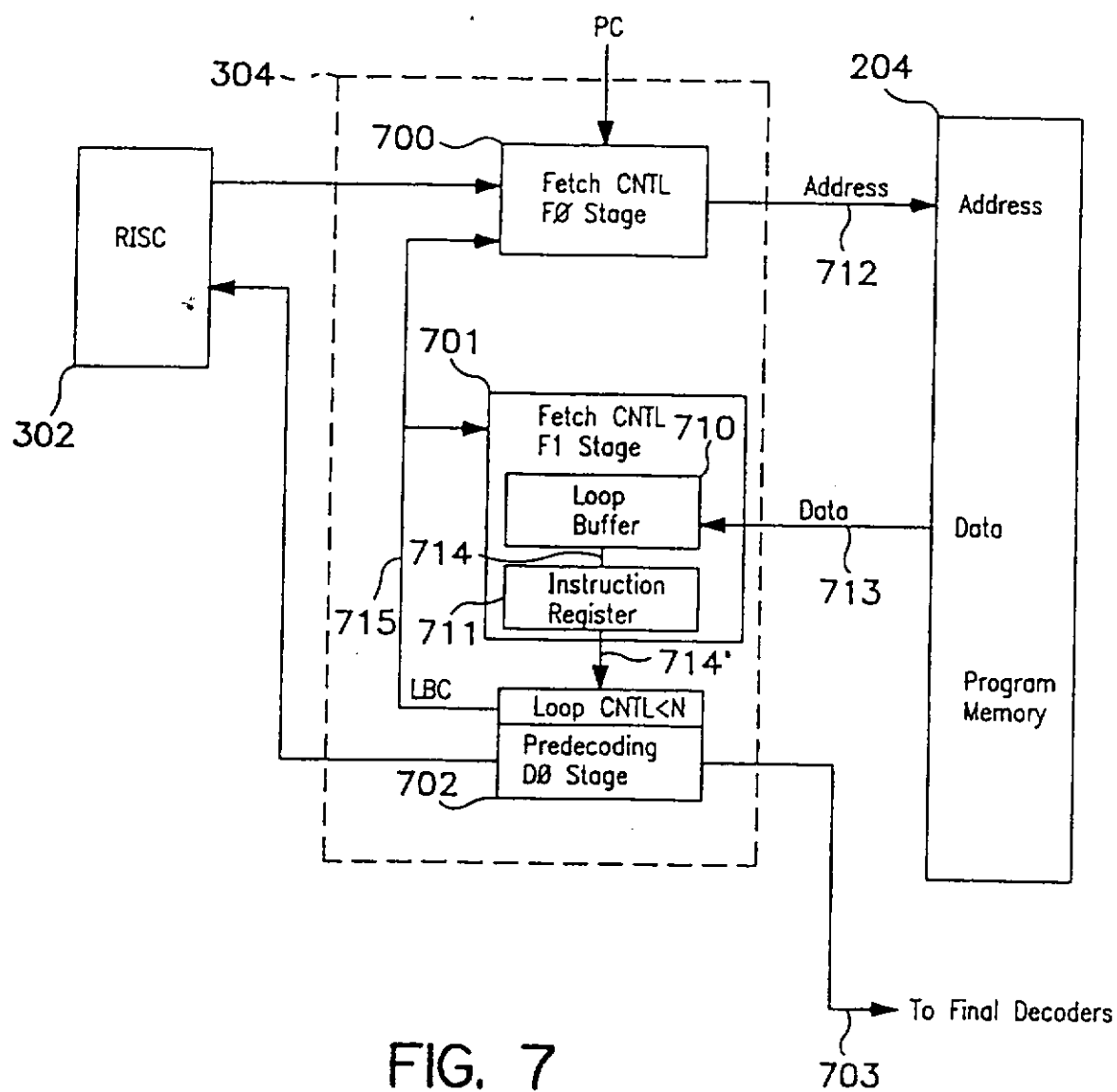


FIG. 7

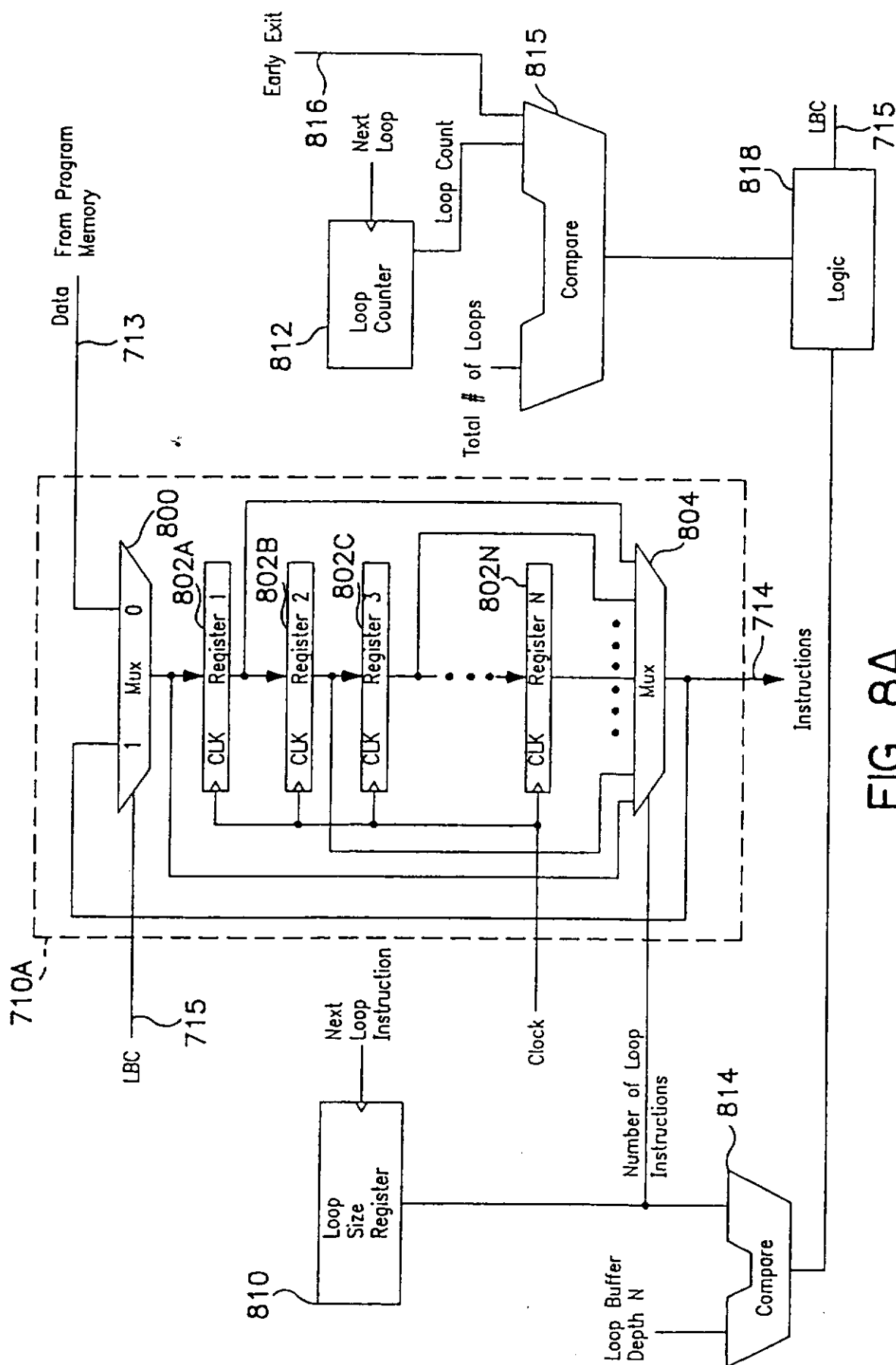


FIG. 8A

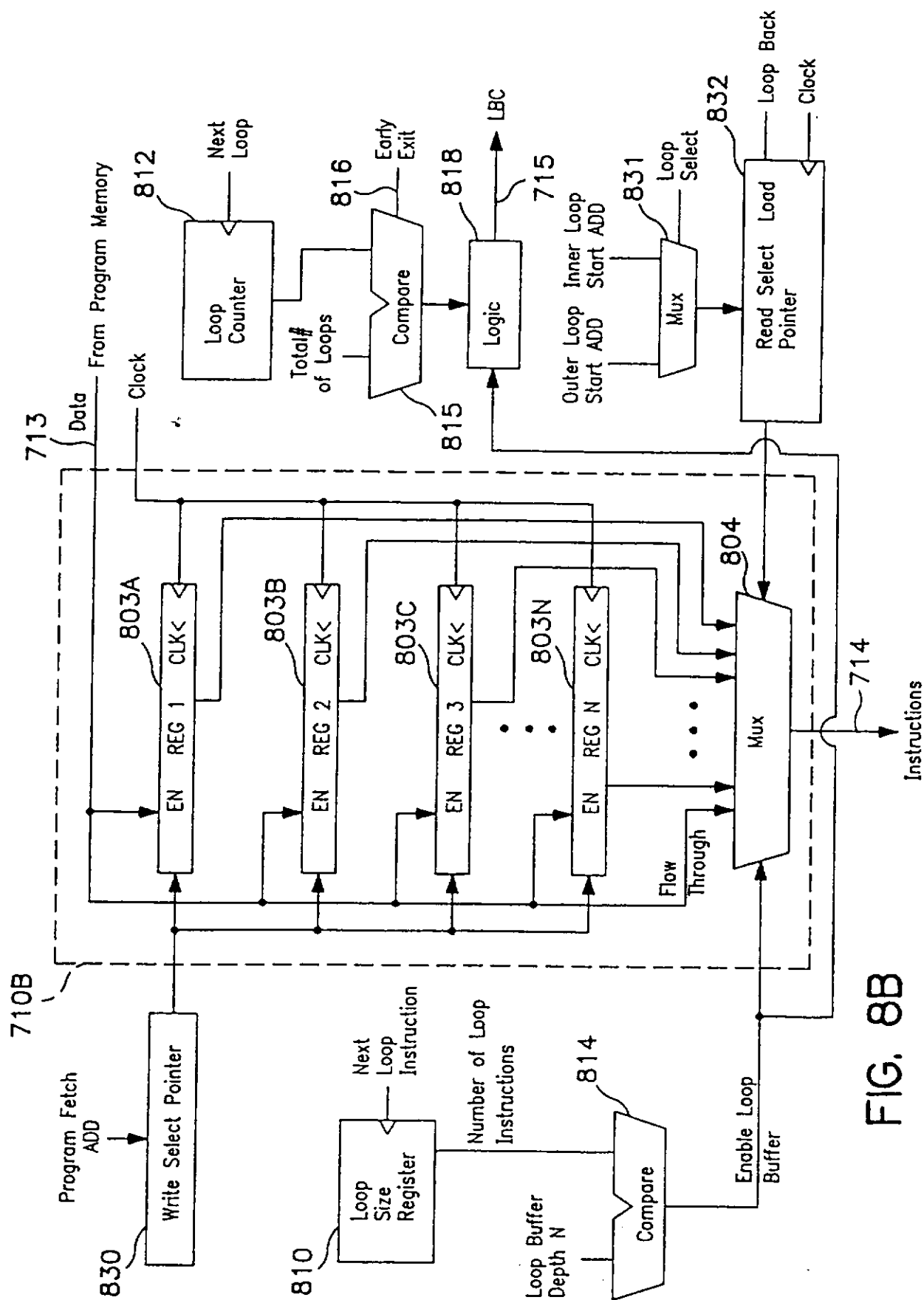


FIG. 8B