Methods for Cell Phasing and Placement in Dynamic Array Architecture and Implementation of the Same

by inventors

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BACKGROUND

[0001] In modern semiconductor chip ("chip") design, standard cells are placed on the chip to define a particular logic function. To ensure that each standard cell will be manufacturable when arbitrarily placed on the chip, each standard cell is defined to have an edge exclusion zone sized equal to one-half of a design rule (DR) spacing requirement between adjacent conductive features. In this manner, when any two standard cells are placed next to each other, their combined exclusion zone sizes at their interfacing boundaries will equal at least the DR spacing requirement between adjacent conductive features. Thus, the exclusion zone enables features to be placed arbitrarily within a standard cell without concern for cell-to-cell interface problems. However, when many standard cells are placed together on the chip, the edge exclusion zones associated with the standard cells can combine to occupy an expensive amount of chip area.

[0002] In view of the foregoing, it is of interest to optimize cell layout and placement such that chip area and routing resources can be most efficiently utilized, particularly when cells are defined according to a constrained layout architecture.

SUMMARY

[0003] In one embodiment, a semiconductor chip is disclosed. The semiconductor chip includes a logic block area. The logic block area includes a first chip level in which layout features are placed according to a first virtual grate. The logic block area also includes a second chip level in which layout features are placed according to a second virtual grate. A rational spatial relationship exists between the first and second virtual grates. A number of cells are placed within the logic block area. Each of the number of cells is defined according to an appropriate one of a number of cell phases. The appropriate cell phase causes layout features in the first and second chip levels of a given placed cell to be aligned with the first and second virtual grates as positioned within the given placed cell.

[0004] In another embodiment, a method is disclosed for defining cell variants of different cell phase to enable placement of cells within a designated area of a semiconductor chip. The method includes an operation for identifying a phase space for the designated area of

the semiconductor chip. The phase space is defined as a distance extending perpendicularly between successive occurrences of a same relationship between the two virtual grates that have a rational spatial relationship within the designated area of the semiconductor chip. The method also includes an operation for aligning a left boundary of a subject cell with a left edge of the phase space. With the left boundary of the subject cell aligned with the left edge of the phase space, an operation is performed to define a first phase of the subject cell based on locations of the two virtual grates relative to the left boundary of the subject cell. The first phase of the subject cell is stored in a cell library. The method further includes an operation for moving the left boundary of the subject cell from its current position across the phase space to a next possible location of the left boundary of the subject cell within the phase space. With the left boundary of the subject cell aligned with the next possible location, an operation is performed to define a next phase of the subject cell based on locations of the two virtual grates relative to the left boundary of the subject cell. The next phase of the subject cell is stored in the cell library. The method continues by moving the left boundary of the subject cell to each of its possible locations within the phase space, and by defining and storing a different phase of the subject cell at each possible location of the left boundary of the subject cell within the phase space.

[0005] In another embodiment, a method is disclosed for placing cells within a designated area of a semiconductor chip. The method includes an operation for defining respective virtual grates for each of two phased chip levels within the designated area of the semiconductor chip. The virtual grates of the two phased chip levels are defined to have a rational spatial relationship. The method also includes an operation for placing cells within the designated area of the semiconductor chip. The method further includes an operation for determining a required cell phase for each placed cell within the designated area of the semiconductor chip. For each placed cell within the designated area of the semiconductor chip, an operation is performed to substitute a variant of the placed cell having the required cell phase, such that layout features in each of the two phased chip levels within the substituted variant of the placed cell align with the virtual grates of the two phased chip levels.

[0006] In one embodiment, a computer readable storage medium is disclosed to include a semiconductor chip layout recorded in a digital format. The semiconductor chip layout includes a logic block area including a first chip level in which layout features are placed according to a first virtual grate. The semiconductor chip layout also includes a second chip

level in which layout features are placed according to a second virtual grate. A rational spatial relationship exists between the first and second virtual grates. The semiconductor chip layout further includes a number of cells placed within the logic block area. Each of the number of cells is defined according to an appropriate one of a number of cell phases. The appropriate one of the number of cell phases causes layout features in the first and second chip levels of a given placed cell to be aligned with the first and second virtual grates as positioned within the given placed cell.

[0007] In one embodiment, a cell library stored in a digital format on a computer readable storage medium is disclosed. The cell library includes a plurality of cell layouts corresponding to different phases of a given cell. The given cell includes at least one chip level in which layout features are placed in accordance with a virtual grate. The virtual grate is defined by a set of parallel equally spaced virtual lines extending across the cell layout. Each different phase of the given cell is defined by a different spacing between a reference cell boundary and a nearest virtual line of the virtual grate.

[0008] Other aspects and advantages of the invention will become more apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A is an illustration showing a semiconductor chip defined to include a logic block, in accordance with one embodiment of the present invention;

Figure 1B is an illustration showing placement of cells in the logic block, in accordance with one embodiment of the present invention;

Figure 2A is an illustration showing the logic block area of the chip having two separate virtual grates defined thereover, in accordance with one embodiment of the present invention;

Figure 2B is an illustration showing the exemplary logic block in conjunction with the gate level and M2 level virtual grates, which are indexed to the origin at the lower-left corner of the logic block, in accordance with one embodiment of the present invention;

Figure 2C is an illustration showing the cell placement of Figure 2B, with an appropriate cell variant substituted for each cell based on the required cell phasing for the various cell placements within the logic block, in accordance with one embodiment of the present invention;

Figures 3A-3H are illustrations showing different cell phases that may exist for a cell placed in the logic block of Figure 2A, in accordance with one embodiment of the present invention;

Figures 3I-3P are illustrations showing different cell phases in which virtual grates are phased with each other without actually aligning with each other, in accordance with one embodiment of the present invention;

Figure 4 is an illustration showing Row 1 of the logic block of Figure 2C, with exemplary gate level and M2 level layout shapes depicted for each cell therein, in accordance with one embodiment of the present invention;

Figure 5 is an illustration showing a flowchart of a method for defining cell variants of differing cell phase to enable placement of cells within an area on a semiconductor chip defined according to a dynamic array architecture, in accordance with one embodiment of the present invention;

Figure 6 is an illustration showing a flowchart of a method for placing cells within a portion of a semiconductor chip defined according to a dynamic array architecture, in accordance with one embodiment of the present invention;

Figure 7 is an illustration showing an example of different phasings in a second interconnect level of adjacently disposed logic cells defined within a DAS, in accordance with one embodiment of the present invention; and

Figure 8 shows an example of virtual lines defined within the dynamic array architecture, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0009] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

[0010] Figure 1A is an illustration showing a semiconductor chip ("chip") 101 defined to include a logic block 103, in accordance with one embodiment of the present invention. The logic block 103 includes integrated circuit devices in the form of multi-level structures defined on a silicon substrate of the chip 101. At a substrate level, transistor devices with diffusion regions are formed. In subsequent levels, interconnect metallization lines are patterned and electrically connected to the transistor devices to define a desired integrated

circuit device. Also, patterned conductive layers are insulated from other conductive layers by dielectric materials. The structural features used to define the diffusion regions, transistor devices, metallization lines, interconnects, etc. within each level of the chip 101 are defined according to a specified layout. Additionally, the global layout for a given level of the chip 101 may be segmented into many small layout areas, where each layout area is associated with a given logic construct. Moreover, layout areas within multiple levels of the chip 101 within a given vertical column of the chip 101 can be integrated together to form a logic unit referred to as a cell.

[0011] A cell, as referenced herein, represents an abstraction of a logic function, and encapsulates lower-level integrated circuit layouts for implementing the logic function. It should be understood that a given logic function can be represented by multiple cell variations, wherein the cell variations may be differentiated by feature size, performance, and process compensation technique (PCT) processing. For example, multiple cell variations for a given logic function may be differentiated by power consumption, signal timing, current leakage, chip area, OPC (optical proximity correction), RET (reticle enhancement technology), etc. It should also be understood that each cell description includes the layouts for the cell in each level of a chip within the associated vertical column of the chip, as required to implement the logic function of the cell. More specifically, a cell description includes layouts for the cell in each level of the chip extending from the substrate level up through a particular interconnect level.

[0012] In one embodiment, the logic block 103 is defined by placing a number of cells of various logic function in rows within the logic block 103. For example, consider that a number of cells A-Z are available for use within the logic block 103, where each of cells A-Z is defined to perform a different logic function. In this exemplary embodiment, the logic block 103 may be defined by placement of cells A-Z within rows 1-10 of the logic block 103, as shown in Figure 1B. In this exemplary embodiment, the width of the cells as measured from left-to-right across a given row can vary from cell-to-cell. However, the height of the cells as measured vertically within a given row is essentially the same from cell-to-cell, thereby allowing the logic block 103 to be populated by adjacently defined rows of cells of consistent height. Also, in some embodiments, the height of cells may vary from row-to-row and/or within a row.

[0013] A dynamic array architecture represents a semiconductor device design paradigm in which layout features are defined along a regular-spaced virtual grate (or regular-spaced

virtual grid) in a number of levels of a cell, i.e., in a number of levels of a semiconductor chip, such as chip 101. The virtual grate is defined by a set of equally spaced, parallel virtual lines extending across a given level in a given chip area. The equal spacing, as measured perpendicularly between adjacent virtual lines of the virtual grate, is defined as the virtual grate pitch. For example, Figure 2A shows the logic block 103 area of the chip 101 having two separate virtual grates defined thereover, in accordance with one embodiment of the present invention. More specifically, one virtual grate is defined over the logic block 103 for the gate level of the chip 101, and another virtual grate is defined over the logic block 103 for the second interconnect level (M2 level) of the chip 101.

[0014] In one embodiment, the virtual grate of a given level is oriented to be substantially perpendicular to the virtual grate of an adjacent level. For example, in this embodiment, a virtual grate for the first interconnect level (M1 level) (not shown) extends in a direction perpendicular to both the gate level and M2 level virtual grates. However, it should be appreciated, that in some embodiments, the virtual grate of a given level may be oriented either perpendicular or parallel to the virtual grate of an adjacent level.

[0015] In one embodiment, each virtual grate within various levels of the chip is indexed to an origin of a single coordinate system. Therefore, the coordinate system enables control of a spatial relationship between the virtual grates within the various levels of the chip. For example, in the exemplary embodiment of Figure 2A, each of the gate level and M2 level virtual grates is indexed to an origin (0,0) of a coordinate system, where the origin (0,0) is located at a lower-left corner of the logic block 103 area on the chip 101. It should be understood that the origin (0,0) of the coordinate system can be located at any location on the chip 101, and is not required to be located at a particular position of a logic block in which cells are to be placed (e.g., at the lower-left corner of the logic block 103). Also, it should be understood that indexing of a virtual grate to a given spatial location means that the virtual grate is defined such that one of its virtual lines passes through the given spatial location.

[0016] The spatial relationship between virtual grates in various levels of the chip can be defined in essentially any number of ways. However, the spatial relationship between commonly oriented (i.e., parallel in direction of extent across the chip) virtual grates can be defined by a rational number, such that the virtual grates align with each other at a particular spatial frequency. Specifically, for any two virtual grates that are indexed to the origin of the same coordinate system, a ratio of their virtual grate pitches can be defined by a rational

number, such that the two virtual grates align at a particular spatial frequency. For example, Figure 2A shows that the spatial relationship between the M2 level and gate level virtual grates is defined by a M2 level-to-gate level virtual grate pitch ratio of 4/3. Thus, the M2 level and gate level virtual grates align with each other at every fourth gate level virtual grate line relative to the origin (0,0). Two virtual grates that are commonly oriented, indexed to a common spatial location, and have the ratio of their virtual grate pitches defined by a rational number are considered to have a rational spatial relationship.

[0017] Figure 8 shows an example of virtual lines 801A-801E defined within the dynamic array architecture, in accordance with one embodiment of the present invention. Virtual lines 801A-801E extend across the layout in a parallel manner, with a perpendicular spacing therebetween equal to a specified pitch 807. For illustrative purposes, complementary diffusion regions 803 and 805 are shown in Figure 8. It should be understood that the diffusion regions 803 and 805 are defined in a diffusion level below a gate level. Also, it should be understood that the diffusion regions 803 and 805 are provided by way of example and in no way represent any limitation on diffusion region size, shape, and/or placement within the diffusion level relative to the dynamic array architecture.

[0018] Within the dynamic array architecture, a feature layout channel is defined about a given virtual line so as to extend between virtual lines adjacent to the given virtual line. For example, feature layout channels 801A-1 through 801E-1 are defined about virtual lines 801A through 801E, respectively. It should be understood that each virtual line has a corresponding feature layout channel. Also, for virtual lines positioned adjacent to an edge of a prescribed layout space, e.g., adjacent to a cell boundary, the corresponding feature layout channel extends as if there were a virtual line outside the prescribed layout space, as illustrated by feature layout channels 801A-1 and 801E-1. It should be further understood that each feature layout channel is defined to extend along an entire length of its corresponding virtual line.

[0019] Figure 8 further shows a number of exemplary layout features 809-823 defined in accordance with the feature layout channels 801A-1 through 801E-1 corresponding to virtual lines 801A through 801E, respectively. Within the dynamic array architecture, layout features associated with a given virtual line are defined within the feature layout channel associated with the virtual line. Also, physical contact is prohibited between layout features defined in feature layout channels that are associated with adjacent virtual lines.

[0020] A contiguous layout feature can include both a portion which defines an active part of a circuit, and a portion that does not define a part of the circuit. For example, in the gate level, a contiguous layout feature can extend over both a diffusion region and a dielectric region of an underlying chip level. In one embodiment, each portion of a gate level layout feature that forms a gate electrode of a transistor is positioned to be substantially centered upon a given virtual line. Furthermore, in this embodiment, portions of the gate level layout feature that do not form a gate electrode of a transistor can be positioned within the feature layout channel associated with the given virtual line. Therefore, a given gate level layout feature can be defined essentially anywhere within a feature layout channel, so long as gate electrode portions of the given gate level layout feature are centered upon the virtual line corresponding to the given feature layout channel, and so long as the given gate level layout feature complies with design rule spacing requirements relative to other gate level layout features in adjacent feature layout channels.

[0021] As shown in Figure 8, the layout feature 809 is defined within the feature layout channel 801A-1 associated with virtual line 801A. Some portions of layout feature 809 are substantially centered upon the virtual line 801A. Also, other portions of layout feature 809 maintain design rule spacing requirements with layout features 811 and 813 defined within adjacent feature layout channel 801B-1. Similarly, layout features 811-823 are defined within their respective feature layout channel, and include portions substantially centered upon the virtual line corresponding to their respective feature layout channel. Also, it should be appreciated that each of layout features 811-823 maintains design rule spacing requirements with layout features defined within adjacent feature layout channels, and avoids physical contact with any other layout feature defined within adjacent feature layout channels.

[0022] As illustrated by the example feature layout channels 801A-1 through 801E-1 of Figure 8, each feature layout channel is associated with a given virtual line and corresponds to a layout region that extends along the given virtual line and perpendicularly outward in each opposing direction from the given virtual line to a closest of either an adjacent virtual line or a virtual line outside a layout boundary. Also, it should be understood that each layout feature is defined within its feature layout channel without physically contacting another layout feature defined within an adjoining feature layout channel.

[0023] Some layout features may have one or more contact head portions defined at any number of locations along their length. A contact head portion of a given layout feature is

defined as a segment of the layout feature having a height and a width of sufficient size to receive a contact structure, wherein "width" is defined across the substrate in a direction perpendicular to the virtual line of the given layout feature, and wherein “height” is defined across the substrate in a direction parallel to the virtual line of the given layout feature. It should be appreciated that a contact head of a layout feature, when viewed from above, can be defined by essentially any layout shape, including a square or a rectangle. Also, depending on layout requirements and circuit design, a given contact head portion of a layout feature may or may not have a contact defined thereabove.

[0024] In one embodiment, the layout features are defined to provide a finite number of controlled layout shape-to-shape lithographic interactions which can be accurately predicted and optimized for in manufacturing and design processes. In this embodiment, the layout features are defined to avoid layout shape-to-shape spatial relationships which would introduce adverse lithographic interaction within the layout that cannot be accurately predicted and mitigated with high probability. However, it should be understood that changes in direction of layout features within their feature layout channels are acceptable when corresponding lithographic interactions are predictable and manageable.

[0025] In one embodiment, each layout feature of a given level is substantially centered upon one of the virtual lines of the virtual grate associated with the given level. A layout feature is considered to be substantially centered upon a particular line of a virtual grate when a deviation in alignment between of the centerline of the layout feature and the particular line of the virtual grate is sufficiently small so as to not reduce a manufacturing process window from what would be achievable with a true alignment between of the centerline of the layout feature and the line of the virtual grate. Therefore, in this embodiment, layout features placed in different chip levels according to virtual grates of rational spatial relationship will be aligned at a spatial frequency defined by the rational spatial relationship. In one embodiment, the above-mentioned manufacturing process window is defined by a lithographic domain of focus and exposure that yields an acceptable fidelity of the layout feature. In one embodiment, the fidelity of a layout feature is defined by a characteristic dimension of the layout feature.

[0026] In the dynamic array architecture, variations in a vertical cross-section shape of an as-fabricated layout feature can be tolerated to an extent, so long as the variation in the vertical cross-section shape is predictable from a manufacturing perspective and does not adversely impact the manufacture of the given layout feature or its neighboring layout

features. In this regard, the vertical cross-section shape corresponds to a cut of the as-fabricated layout feature in a plane perpendicular to both the centerline of the layout feature and the substrate of the chip. It should be appreciated that variation in the vertical cross-section of an as-fabricated layout feature along its length can correspond to a variation in width of the layout feature along its length. Therefore, the dynamic array architecture also accommodates variation in the width of an as-fabricated layout feature along its length, so long as the width variation is predictable from a manufacturing perspective and does not adversely impact the manufacture of the layout feature or its neighboring layout features.

[0027] Additionally, different layout features within a given level can be designed to have the same width or different widths. Also, the widths of a number of layout features defined along adjacent lines of a given virtual grate can be designed such that the number of layout features contact each other so as to form a single layout feature having a width equal to the sum of the widths of the number of layout features.

[0028] Within a given level defined according to the dynamic array architecture, proximate ends of adjacent, co-aligned linear-shaped layout features may be separated from each other by a substantially uniform gap. More specifically, adjacent ends of linear-shaped layout features defined along a common line of a virtual grate are separated by an end gap, and such end gaps within the level associated with the virtual grate may be defined to span a substantially uniform distance. Additionally, in one embodiment, a size of the end gaps is minimized within a manufacturing process capability so as to optimize filling of a given level with linear-shaped layout features.

[0029] Also, in the dynamic array architecture, a level can be defined to have any number of virtual grate lines occupied by any number of layout features. In one example, a given level can be defined such that all lines of its virtual grate are occupied by at least one layout feature. In another example, a given level can be defined such that some lines of its virtual grate are occupied by at least one layout feature, and other lines of its virtual grate are vacant, i.e., not occupied by any layout features. Furthermore, in a given level, any number of successively adjacent virtual grate lines can be left vacant. Also, the occupancy versus vacancy of virtual grate lines by layout features in a given level may be defined according to a pattern or repeating pattern across the given level.

[0030] Additionally, within the dynamic array architecture, vias and contacts are defined to interconnect a number of the layout features in various levels so as to form a number of functional electronic devices, e.g., transistors, and electronic circuits. Layout features for the

vias and contacts can be aligned to a virtual grid, wherein a specification of this virtual grid is a function of the specifications of the virtual grates associated with the various levels to which the vias and contacts will connect. Thus, a number of the layout features in various levels form functional components of an electronic circuit. Additionally, some of the layout features within various levels may be non-functional with respect to an electronic circuit, but are manufactured nonetheless so as to reinforce manufacturing of neighboring layout features.

[0031] It should be understood that the dynamic array architecture is defined to enable accurate prediction of semiconductor device manufacturability with a high probability, even when layout features of the semiconductor device are sized smaller than a wavelength of light used to render the layout features in a lithographic manufacturing process. Additionally, it should be understood that the dynamic array architecture is defined by placement of layout features on a regular-spaced grate (or regular-spaced grid) in a number of levels of a cell, such that layout features in a given level of the cell are confined within their feature layout channel, and such that layout features in adjacent feature layout channels do not physically contact each other. Furthermore, it should be understood that the dynamic array architecture can be applied to one or more chip levels. For example, in one embodiment, only the gate level of the chip is defined according to the dynamic array architectures. In another embodiment, the gate level and one or more interconnect levels are defined according to the dynamic array architecture.

[0032] With reference back to Figure 1B, the exemplary logic block 103 is defined by placement of cells A-Z within rows 1-10. Figure 2B is an illustration showing the exemplary logic block 103 in conjunction with the gate level and M2 level virtual grates, which are indexed to the origin (0,0) at the lower-left corner of the logic block 103. In one embodiment of the dynamic array architecture, in order for each of cells A-Z to be placeable within the logic block 103, each of cells A-Z should be defined based on use of the gate level and M2 level virtual grates of the logic block 103. However, depending on where a cell is placed in the logic block 103, a position of the gate level and M2 level virtual grates may vary within the boundaries of the cell, and relative to the boundaries of the cell. For example, a distance between the left boundary of the cell and the nearest gate level virtual grate line within the cell can vary between different positions of the cell in the logic block 103. Similarly, a distance between the left boundary of the cell and the nearest M2 level

virtual grate line within the cell can vary between different positions of the given cell in the logic block 103.

[0033] Each cell placed within the logic block 103 should have its cell-based gate level and M2 level virtual grates aligned with the gate level and M2 level virtual grates of the logic block 103. Because the position of the gate level and M2 level virtual grates of the logic block 103 can vary within a given cell depending on where the given cell is placed in the logic block 103, it is necessary to have different versions of the given cell available for placement in the logic block 103, such that at least one version of the given cell is defined to have its gate level and M2 level virtual grates respectively align with the gate level and M2 level virtual grates of the logic block 103.

[0034] Generally speaking, each cell is defined to have a width that is an integer multiple of either a virtual grate pitch, or one-half of a virtual grate pitch, to enable alignment of the cell boundaries to either a virtual grate line or a midpoint between adjacent virtual grate lines. In one embodiment, each cell is defined to have a width that is an integer multiple of one-half of the gate level virtual grate pitch. In another embodiment, each cell is defined to have a width that is an integer multiple of the gate level virtual grate pitch. Additionally, each cell can be placed in the logic block 103 such that its left cell boundary is aligned with either a gate level virtual grate line or a midpoint between adjacent gate level virtual grate lines. Therefore, when the cell width is an integer multiple of one-half of the gate level virtual grate pitch, the right cell boundary will also be aligned with either a gate level virtual grate line or a midpoint between adjacent gate level virtual grate lines. For ease of discussion, placement of a cell such that its left cell boundary is aligned with either a gate level virtual grate line or a midpoint between adjacent gate level virtual grate lines is referred to as placement of the cell on the gate level virtual grate half-pitch.

[0035] Placement of cells on the gate level virtual grate half-pitch in combination with the rational spatial relationship between the gate level and M2 level virtual grates enables creation of a finite number of layout variations for a given cell, such that a suitable layout variation for the given cell is available for each possible combination of gate level and M2 level virtual grate placements that may occur within the given cell, depending upon where the given cell is placed in the logic block 103. In this regard, each layout variation for a given cell defines a cell phase, wherein each cell phase is defined by a different combination of gate level and M2 level virtual grate placements within the given cell

relative to a reference boundary of the given cell, e.g., relative to the left boundary of the given cell.

[0036] It should be understood that in the above-described embodiment, the width of each cell is an integer multiple of the gate level virtual grate half-pitch, but not necessarily an integer multiple of the M2 level virtual grate pitch. Therefore, although the left and right cell boundaries will align with the gate level virtual grate, the left and right cell boundaries may not always align with the M2 level virtual grate. However, the cell phasing methods described herein allow for placement of active M2 level layout shapes on the M2 level virtual grate. Therefore, the cell phasing and cell placement methods described herein, in conjunction with the dynamic array architecture, serve to optimize routing resources by not having an M2 level layout shape placed between adjacent M2 level virtual grate lines so as to consume the two adjacent M2 level virtual grate lines with one M2 level layout shape.

[0037] Figures 3A-3H illustrate different cell phases that may exist for a cell placed under the following conditions:

1. The cell is placed in a logic block defined according to the dynamic array architecture where the rational spatial relationship between the M2 level and gate level virtual grates is defined by a M2 level-to-gate level virtual grate pitch ratio of 4/3;
2. The cell is placed on the gate level virtual grate half-pitch; and
3. The cell width is an integer multiple of one-half of the gate level virtual grate pitch.

[0038] It should be understood that the cell phasing principles illustrated in Figures 3A-3H can be applied to any combination of commonly oriented chip levels (i.e., beyond the illustrated gate and M2 levels) having any rational spatial relationship (i.e., beyond the 4/3 M2-to-gate pitch ratio), so long as the virtual grates of the logic block that are associated with the cell phasing are indexed to a common spatial location.

[0039] Figure 3A shows a first phase (ph1) of a cell 300. The cell 300 includes a left cell boundary 301. The cell 300 is defined by a gate level virtual grate represented by commonly oriented solid lines, and by a M2 level virtual grate represented by commonly oriented dashed lines. The pitch ratio between the M2 level and gate level virtual grates is 4/3. Therefore, the M2 level and gate level virtual grate will align with each other at every fourth gate level virtual grate line. The number of gate level virtual grate lines between alignment of the gate level and M2 level virtual grates defines a phase space 303. Generally speaking, a phase space is defined as a distance extending perpendicularly between successive

occurrences of a same relationship between the two virtual grates that have a rational spatial relationship. In the exemplary embodiment of Figures 3A-3H the successive occurrences of a same relationship between the two virtual grates that have a rational spatial relationship correspond to successive alignments of the two virtual grates that have the rational spatial relationship.

[0040] Each cell phase is associated with a different allowed position of the left cell boundary 301 (e.g., reference cell boundary) within the phase space 303. In the example of Figures 3A-3H, the left cell boundary 301 can be placed on the gate level virtual grate half-pitch. Therefore, the left cell boundary 301 can be placed on each gate level virtual grate line within the phase space 303, and at the midpoint between adjacent gate level virtual grate lines within the phase space 303. Therefore, because the phase space 303 covers four gate level virtual grate pitches and because the cell can be placed on the gate level virtual grate half-pitch, the number of possible cell phases is eight. In Figures 3A-3H, the position of the left cell boundary 301 for each of the eight possible cell phases is identified by a respective arrow labeled ph1-ph8. Because the gate level and M2 level virtual grates are associated with the logic block 103, their respective positions remain unchanged in each of Figures 3A-3H as the left cell boundary 301 is shifted through the eight possible phases (ph1-ph8).

[0041] It should be understood that the eight possible cell phases of Figures 3A-3H are a result of the particular specifications of the exemplary embodiment. For example, in another embodiment, if the phase space 303 covered four gate level virtual grate pitches, but the cell could only be placed on the gate level virtual grate (whole) pitch, the number of possible cell phases would be four instead of eight, and would correspond to cell phases (ph1, ph3, ph5, ph7) as shown in Figures 3A-3H.

[0042] Generally speaking, a cell phase is defined by a combination of index values for each of the chip levels associated with the phasing. The index value for a given chip level as used in defining a cell phase represents a distance measured perpendicularly between the left boundary of the cell and the nearest virtual line of the given chip level’s virtual grate. It should be understood that each phased chip level of a given cell has a corresponding index value. Also, it should be understood that a phased chip level of a cell is any chip level of the cell defined by a virtual grate that has a rational spatial relationship with a virtual grate of at least one other chip level of the cell. Also, as previously discussed, a rational spatial relationship exists between two chip levels when each of the two chip levels is defined by

commonly oriented virtual grates that are indexed to a common spatial location, and have the ratio of their virtual grate pitches defined by a rational number. In the exemplary embodiment of Figures 3A-3H, each cell phase (ph1-ph8) is defined by two index values: 1) G_{index}, and 2) $M2_{index}$, where G_{index} is the index value for the gate level and $M2_{index}$ is the index value for the M2 level. As shown in Figures 3A-3H, each phase is defined by a unique combination of G_{index} and $M2_{index}$ values.

[0043] The cell phasing example illustrated by Figures 3A-3H is based on a virtual grate phasing relationship in which the two virtual grates are indexed to periodically align with each other according to their rational spatial relationship. It should be understood, however, that in some embodiments, virtual grates can be phased with each other without actually aligning with each other. For example, Figures 3I-3P illustrate another embodiment in which the pitch ratio between the M2 level and gate level virtual grates is 4/3, and in which the M2 level virtual grate is indexed in an offset relationship with the gate level virtual grate, such that the M2 level and gate level virtual grates do not align with each other at any phase. The same concepts described with regard to Figures 3A-3H also apply to Figures 3I-3P. Generally speaking, it should be understood that the phase space 303' in Figures 3I-3P is defined over an area between extending successive occurrences of a same relationship between the phased virtual grates. Specifically, at phase (ph1') the index value for the gate level is given by $G_{index}=0$, and the index value for the M2 level is given by $M2_{index}=(1/6)*G_{pitch}$. Therefore, the phase space 303' extends to a location where the phase (ph1') reoccurs, i.e., where $G_{index}=0$ and $M2_{index}=(1/6)*G_{pitch}$. For ease of discussion, the remainder of the description herein is provided with reference to the phasing as illustrated in Figures 3A-3H.

[0044] In one embodiment, a cell library is compiled to include a number of different cells defined in accordance with the dynamic array architecture, and further defined based on a particular rational spatial relationship between particular chip levels. For example, with respect to the logic block 103 embodiment of Figures 2A-2B, a cell library can be compiled to include cells A-Z, where each of cells A-Z is defined in accordance with the dynamic array architecture, and is further defined based on a rational spatial relationship of 4/3 between the virtual grate pitches of the M2 level and the gate level. To ensure that gate level and M2 level layouts of each cell in the library can be aligned with the gate level and M2 level virtual grates of the logic block 103, regardless of cell placement within the logic block, the cell library should include variants of each cell that respectively correspond to

each possible cell phase. Therefore, with regard to the embodiment of Figures 2A-2B, the cell library should include eight different cell variants (one for each cell phase) for each of cells A-Z. Variants of cells A-Z for cell phases 1 through 8 may be identified as A-ph1, A-ph2, ... Z-ph7, Z-ph8.

[0045] In one embodiment, cells may be first placed in the logic block 103 without regard to cell phasing, as shown in Figure 2B. Then, each placed cell can be replaced by an appropriate variant corresponding to the required cell phase based on its exact position in the logic block 103, relative to the gate level and M2 level virtual grates of the logic block 103. In another embodiment, appropriate cell variants corresponding to the required cell phasing can be determined when the cells are initially placed in the logic block 103. Figure 2C shows the cell placement of Figure 2B, with an appropriate cell variant substituted for each cell based on the required cell phasing for the various cell placements within the logic block 103.

[0046] As previously discussed, each cell phase is defined by the combination of index values for the phased chip levels. Therefore, in order to determine the appropriate cell phase to be used for a given cell placement, the index values for the phased chip levels of the placed cell are calculated. Then, the calculated index values for the phased chip levels of the placed cell are compared to the index values of the various cell phases to identify the matching cell phase. The matching cell phase of the placed cell is then substituted for the placed cell.

[0047] For example, in the embodiment of Figure 2B, each cell phase is defined by the combination of the gate level index value (G_{index}) and the M2 level index value ($M2_{index}$). Therefore, in order to determine the appropriate cell phase to be used for a given cell placement, the G_{index} and the $M2_{index}$ values for the placed cell are calculated. Then, the calculated G_{index} and $M2_{index}$ values for the placed cell are compared to the G_{index} and $M2_{index}$ values of the various cell phases to identify the matching cell phase. Then, the matching cell phase of the placed cell is substituted for the originally placed cell.

[0048] To illustrate further, consider the leftmost placed cell A of Row 1 in the logic block 103 of Figure 2B as the subject cell. The G_{index} value of the subject cell is calculated to be zero, i.e., the left cell boundary 301 is aligned with the gate level virtual grate. The $M2_{index}$ value of the subject cell is calculated to be zero, i.e., the left cell boundary 301 is aligned with the M2 level virtual grate. The calculated index values of the subject cell (G_{pitch}=0, and $M2_{index}$=0) match the index values of cell phase 1, as shown in Figure 3A. Therefore, cell

phase 1 should be used for the subject cell, as indicated by corresponding cell A-ph1 in Row 1 of Figure 2C.

[0049] To illustrate further, consider the rightmost placed cell U of Row 4 in the logic block 103 of Figure 2B as the subject cell. The G_{index} value of the subject cell is calculated to be $((1/2)*G_{pitch})$, wherein G_{pitch} is the gate level virtual grate pitch. The $M2_{index}$ value of the subject cell is calculated to be $((1/6)*G_{pitch})$. The calculated index values of the subject cell ($G_{pitch}=((1/2)*G_{pitch})$, and $M2_{index}=((1/6)*G_{pitch})$) match the index values of cell phase 6, as shown in Figure 3F. Therefore, cell phase 6 should be used for the subject cell, as indicated by corresponding cell U-ph6 in Row 4 of Figure 2C.

[0050] Figure 4 shows Row 1 of the logic block 103 of Figure 2C, with exemplary gate level and M2 level layout shapes depicted for each cell therein. Due to specification of the appropriate cell phase for each cell in Row 1, it can be seen that the gate level layout shapes of each cell align with the gate level virtual grate of the logic block 103, and the M2 level layout shapes of each cell align with the M2 level virtual grate of the logic block 103.

[0051] The cell phasing methods described herein with regard to the M2 level-to-gate level rational spatial relationship can be equally applied to any plurality of chip levels. Additionally, the rational spatial relationship between any two chip levels can be based on essentially any virtual grate pitch ratio between the two chip levels. For example, while the exemplary embodiments of Figures 2A-4 are based on a M2 level-to-gate level pitch ratio of 4/3, the M2 level-to-gate level pitch ratio in other embodiments may be 3/2, 5/3, 5/4, 2/3, 3/5, 4/5, etc.

[0052] It should be appreciated that the cell phasing methods described herein provide for maximum packing of cells within a given chip area, e.g., logic block 103, without comprising adherence to the dynamic array architecture. In other words, the cell phasing methods described herein allow cells to be placed cell boundary-to-cell boundary within the given chip area, while ensuring that the layout shapes within the phased chip levels of the cells align with virtual grates of the phased chip levels. Therefore, the cell phasing methods described herein alleviate the need to expand a width of a cell to accommodate alignment of layout features within the cell to multiple virtual grates, thereby providing for optimized chip area utilization in conjunction with use of the dynamic array architecture. Additionally, the cell phasing methods described herein alleviate the need to leave unoccupied chip area between adjacently placed cells to accommodate alignment of layout features within the cell

to multiple virtual grates, thereby providing for optimized chip area utilization in conjunction with use of the dynamic array architecture.

[0053] Figure 5 is an illustration showing a flowchart of a method for defining cell variants of differing cell phase to enable placement of cells within an area of a semiconductor chip defined according to a dynamic array architecture, in accordance with one embodiment of the present invention. It should be understood that the area on the semiconductor chip may correspond to an area that is substantially smaller than the total area of the semiconductor chip. The method includes an operation 501 for identifying a phase space based on a rational spatial relationship between virtual grates of phased chip levels. The virtual grates of the phased chip levels represent part of the dynamic array architecture used to define the area of the semiconductor chip. As previously discussed, the phase space is defined as a distance extending perpendicularly between successive alignment positions of two virtual grates that have a rational spatial relationship. For example, if first and second virtual grates have a rational spatial relationship such that the first and second virtual grates align at every fourth virtual line of the first virtual grate, then the phase space spans a distance of four times the pitch of the first virtual grate extending between successive alignments of the first and second virtual grates.

[0054] The method continues with an operation 503 in which a left boundary of a subject cell is aligned with a left edge of the phase space. Therefore, following operation 503, the left boundary of the subject cell is simultaneously aligned with a virtual line of each virtual grate of the phased chip levels. Figure 3A shows an example of alignment between the left boundary 301 of the cell 300 and the left edge of the phase space 303. Thus, in the example of Figure 3A, the left boundary 301 of the cell 300 is simultaneously aligned with a virtual line of each virtual grate of the phased chip levels (i.e., the gate level and the M2 level).

[0055] With the left boundary of the subject cell aligned with the left edge of the phase space, the method continues with an operation 505 for defining a first phase of the subject cell based on locations of the virtual grates of the phased chip levels relative to the left cell boundary. The first phase of the subject cell represents a first variant of the subject cell that is suitable for placement on the semiconductor chip at a location where the first phase of a given cell is required. The first phase of the subject cell can be characterized by index values for each phased chip level, where the index value for a given phased chip level is defined as the distance measured perpendicularly between the left boundary of the cell and the nearest virtual line of the given chip level’s virtual grate within the phase space. Figures

3A-3H show corresponding index values G_{index} and $M2_{index}$ for the gate and M2 phased chip levels. Operation 505 includes storage of the first phase of the subject cell in a cell library for future recall and use. In one embodiment, the cell library is stored in a digital format on a computer readable medium.

[0056] Following the operation 505, the method proceeds with an operation 507 in which the left boundary of the cell is moved from its current position across the phase space to a next possible location of the left boundary of the cell within the phase space. It should be understood that the left boundary of the cell is moved across the phase space in operation 507 without moving the virtual grates of the phased chip levels within the phase space. Figure 3B shows an example of moving the left boundary 301 of the cell 300 from its current position (i.e., from its position in Figure 3A) to the next possible location (ph2) of the left boundary of the cell within the phase space 303.

[0057] If the particular dynamic array architecture embodiment for the area of the semiconductor chip allows for cell widths that are an integer multiple of the gate level virtual grate half-pitch, then the possible locations of the left cell boundary within the phase space correspond to each gate level virtual grate line within the phase space and to each midpoint between each adjacent pair of gate level virtual grate lines within the phase space. This situation is exemplified in Figures 3A-3H. If the particular dynamic array architecture embodiment for the area of the semiconductor chip only allows cell widths that are an integer multiple of the gate level virtual grate (whole) pitch, then the possible locations of the left cell boundary within the phase space correspond to either a gate level virtual grate line or a midpoint between an adjacent pair of gate level virtual grate lines within the phase space.

[0058] With the left boundary of the subject cell aligned with the next possible location of the left boundary of the cell within the phase space, the method continues with an operation 509 for defining a next phase of the subject cell based on locations of the virtual grates of the phased chip levels relative to the left cell boundary. This next phase of the subject cell represents another variant of the subject cell that is suitable for placement on the semiconductor chip at a location where this next phase of a given cell is required. This next phase of the subject cell can also be characterized by index values for each phased chip level. Operation 509 includes storage of this next phase of the subject cell in the cell library for future recall and use.

[0059] The method then proceeds with a decision operation 511 for determining whether another possible location of the left boundary of the cell exists within the phase space. If another possible location of the left boundary of the cell does exist within the phase space, the method reverts back to operation 507. However, if another possible location of the left boundary of the cell does not exist within the phase space, the method concludes. Following completion of the method of Figure 5, the cell library will include a variant of the subject cell for each possible cell phase that may occur within the area on the semiconductor chip defined according to the phased chip levels of the dynamic array architecture.

[0060] Figure 6 is an illustration showing a flowchart of a method for placing cells within a portion of a semiconductor chip defined according to a dynamic array architecture, in accordance with one embodiment of the present invention. The method includes an operation 601 for defining respective virtual grates for each of two phased chip levels within the portion of the semiconductor chip. The two phased chip levels are defined to have a rational spatial relationship. As previously discussed, two virtual grates that are commonly oriented, indexed to a common spatial location, and have the ratio of their virtual grate pitches defined by a rational number are considered to have a rational spatial relationship. In one embodiment, the two phased chip levels correspond to a gate level and a second interconnect level. However, it should be understood that in other embodiments, the two phased chip levels can correspond to any two chip levels.

[0061] The method then proceeds with an operation 603 for placing cells within the portion of the chip. In one embodiment, the two phased chip levels are indexed to a lower-left corner of the portion of the chip, and the cells are placed in rows extending from left to right across the portion of the chip. Also, in one embodiment, the cells can be placed such that their boundaries, which are commonly oriented with the virtual grates of the two phased chip levels, align with the half-pitch of the virtual grate of the phased chip level having the smaller virtual grate pitch.

[0062] The method then proceeds with an operation 605 for determining the cell phase required for each cell placed in operation 603. In one embodiment, the required cell phase for a given cell is identified by index values for the phased chip levels within the placed cell. Again, the index value for a given phased chip level within the placed cell is defined as the distance measured perpendicularly between the left boundary of the placed cell and the nearest virtual line of the given phased chip level's virtual grate within the placed cell, i.e., the nearest virtual line of the given phased chip level virtual grate that is to the right of the

left boundary of the cell. Calculated index values for the phased chip levels of each placed cell can be compared to corresponding index values of variants of the same placed cell within a cell library to identify a particular variant of the same placed cell having the required cell phase. An operation 607 is then performed to substitute for each placed cell the particular variant of the placed cell that has the required cell phase, thereby causing the layout features in the phased chip levels of each placed cell to align with the virtual grates of the phased chip levels defined across the portion of the semiconductor chip.

[0063] Based on the foregoing, in one embodiment, a semiconductor chip is defined to include a logic block area. The logic block area includes a first chip level in which layout features are placed according to a first virtual grate. The logic block area also includes a second chip level in which layout features are placed according to a second virtual grate. A rational spatial relationship exists between the first and second virtual grates. A number of cells are placed within the logic block area. Each of the number of cells is defined according to an appropriate one of a number of cell phases. The appropriate cell phase causes layout features in the first and second chip levels of a given placed cell to be aligned with the first and second virtual grates as positioned within the given placed cell. It should be understood that a given cell defined in accordance with either of the number of cell phases is defined to perform a same logic function associated with the given cell. Moreover, in one embodiment, it is of interest to define each variant of a given cell, corresponding to the various cell phases, to have similar electrical characteristics. Also, in one embodiment, some of the number of cells include at least one layout feature placed in either the first chip level or the second chip level in a substantially centered manner along a cell boundary that is parallel to virtual lines of the first and second virtual grates.

[0064] In one embodiment, the number of cells are placed in rows within the logic block area, such that interfacing cell boundaries are co-aligned. Also, in one embodiment, a height of each of the number of cells is uniform. The height of each of the number of cells is measured in a direction parallel to virtual lines of the first and second virtual grates. Additionally, in one embodiment, a width of each of the number of cells is an integer multiple of a pitch of the first virtual grate, and each boundary of each placed cell (that is parallel to virtual lines of the first virtual grate) is aligned with a virtual line of the first virtual grate. In another embodiment, a width of each of the number of cells is an integer multiple of a pitch of the first virtual grate, and each boundary of each placed cell (that is parallel to virtual lines of the first virtual grate) is aligned with a midpoint between adjacent

virtual lines of the first virtual grate. In yet another embodiment, a width of each of the number of cells is an integer multiple of one-half of a pitch of the first virtual grate, and each boundary of each placed cell (that is parallel to virtual lines of the first virtual grate) is aligned with either a virtual line of the first virtual grate or a midpoint between adjacent virtual lines of the first virtual grate.

[0065] Additionally, while the above-described embodiments are discussed within the context of phasing each cell placed within a given logic block, it should be understood that in an alternative embodiment, the cell phasing methods described herein may be applied to a portion of the cells placed within a given logic block, with a remainder of the cells in the logic block left unphased. For instance, if a first group of cells in a given logic block are defined according to the dynamic array architecture and utilize appropriate phasing when placed, and a second group of cells in the given logic block are defined by another architecture (i.e., non-dynamic array architecture) that does not utilize phasing, the first group of cells can be placed and phased in accordance with the methods disclosed herein, and the second group of cells can be left unphased.

[0066] A dynamic array section (DAS) is defined as a subdivision of dynamic array architecture in which the features present in each vertically delineated level of the subdivision are defined with consideration of other features in the subdivision according to a set of rules, wherein the rules are established to govern relationships between features in a given level of the subdivision and between features in separate levels of the subdivision. A DAS can be defined to occupy a substrate area of arbitrary shape and size. A DAS can also be defined to occupy an area of arbitrary shape and size above the substrate.

[0067] Also, as discussed in co-pending U.S. Patent Application No. 12/013,342, conductive features in a given level of a logic cell, i.e., in a given level of a DAS containing the logic cell, can be indexed relative to an origin of the logic cell. For example, the origin of the logic cell in a given level is considered to be located at a lower left corner of the logic cell when viewed in a direction perpendicular to the plane of the substrate. Because logic cell widths are variable, a logic cell boundary in the width direction may not always fall on a conductive feature pitch or half-pitch within a given DAS level. Therefore, depending on the origin of the logic cell relative to the virtual grate of the given DAS level, the conductive features in the given DAS level of the logic cell may need to be shifted relative to the logic cell origin in order to align with the virtual grate of the given DAS level when the logic cell is placed on the chip. As discussed above, the shifting of conductive features

in a given level of a logic cell relative of the origin of the logic cell is called phasing. Therefore, phasing provides for alignment of conductive features in a given level of a logic cell to the virtual grate of the DAS for the given chip level, depending on the location of the origin of the logic cell. For example, in the case where the gate electrode virtual grate extends across logic cell boundaries, phasing may be required to maintain alignment of second interconnect level conductive features in a given logic cell to the second interconnect level virtual grate.

[0068] Figure 7 is an illustration showing an example of different phasings in a second interconnect level of adjacently disposed logic cells defined within a DAS, in accordance with one embodiment of the present invention. Figure 7 corresponds to Figure 33 of co-pending U.S. Patent Application No. 12/013,342. Figure 7 shows three exemplary cells (Cell 1, Phase A; Cell 1, Phase B; and Cell 1, Phase C) disposed adjacent to each other in a DAS. Therefore, each of the three cells share a virtual grate in each level of the DAS. To facilitate description of the phasing concept, the second interconnect level conductive features 3303 of each cell are shown superimposed over the gate electrode level conductive features 3301 of each cell. The cell boundaries in the width direction fall on the gate electrode half-pitch.

[0069] It should be understood that the M2 level-to-gate level virtual grate pitch ratio of 4/3 as used in the examples of Figures 2A-4 to illustrate the cell phasing principles is one example of many possible virtual grate pitch ratios that can be applied between different chip levels. For instance, in the exemplary embodiment of Figure 7, an M2 level-to-gate level virtual grate pitch ratio of 3/4 is used, such that four second interconnect level conductive feature pitches are provided for every three gate electrode level conductive feature pitches.

[0070] The origin of each cell is shown to reside at the cell's lower left corner. Each phasing of Cell 1 for the second interconnect level is defined by an indexing of the second interconnect level conductive features to the origin of the cell. As shown in the example of Figure 7, the index, i.e., spacing, of the second interconnect level conductive features relative to the origin is consecutively reduced for each of Phases A, B, and C. By defining each level of each logic cell to have an appropriate phase, it is possible to place logic cells next to one another in a common DAS such that conductive features defined within the various logic cells within a given DAS level can be aligned to a common virtual grate associated with the given DAS level. Additionally, it should be appreciated that in one

embodiment adjacent cells within a DAS can be defined and placed so as to share conductive features in one or more levels of the DAS. For example, the Phase B and C instances of Cell 1 in Figure 7 are depicted as sharing a second interconnect level conductive feature.

[0071] It should be understood that in some embodiments the dynamic array architecture may only be applied to a portion of one chip level, with overlying portions of other chip levels unconstrained with respect to dynamic array architecture restrictions. For example, in one embodiment, the gate electrode level is defined to comply with the dynamic array architecture, and the higher interconnect levels are defined in an unconstrained manner, i.e., in a non-dynamic array manner. In this embodiment, the gate electrode level is defined by a virtual grate and its corresponding feature layout channels within which gate electrode level conductive features are defined, as discussed above. Also, in this embodiment, the layout features of the non-dynamic array higher interconnect levels can be unconstrained with regard to a virtual grate and associated feature layout channels. For instance, in this particular embodiment, layout features in any interconnect level above the gate electrode level can include bends so as to form arbitrary two-dimensionally shaped layout features.

[0072] As an alternative to the above-mentioned embodiment, other embodiments can exist in which multiple chip levels are defined according to the dynamic array architecture. It should be understood that the phasing techniques disclosed herein are equally applicable to any embodiment that uses the dynamic array architecture, regardless of the number of chip levels that are defined according to the dynamic array architecture.

[0073] It should be understood that the cell phasing techniques as disclosed herein can be defined in a layout that is stored in a tangible form, such as in a digital format on a computer readable medium. For example, the cell phasing layouts as disclosed herein can be stored in a layout data file of one or more cells, selectable from one or more libraries of cells. The layout data file can be formatted as a GDS II (Graphic Data System) database file, an OASIS (Open Artwork System Interchange Standard) database file, or any other type of data file format suitable for storing and communicating semiconductor device layouts. Also, multi-level layouts utilizing the cell phasing techniques can be included within a multi-level layout of a larger semiconductor device. The multi-level layout of the larger semiconductor device can also be stored in the form of a layout data file, such as those identified above.

[0074] Also, the invention described herein can be embodied as computer readable code on a computer readable medium. For example, the computer readable code can include the layout data file within which one or more layouts including the cell phasing techniques are stored. The computer readable code can also include program instructions for selecting one or more layout libraries and/or cells that include a layout utilizing the cell phasing techniques as defined therein. The layout libraries and/or cells can also be stored in a digital format on a computer readable medium.

[0075] The computer readable medium mentioned herein is any data storage device that can store data which can thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, magnetic tapes, and other optical and non-optical data storage devices. The computer readable medium can also be distributed over a network of coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[0076] Any of the operations described herein that form part of the invention are useful machine operations. The invention also relates to a device or an apparatus for performing these operations. The apparatus may be specially constructed for the required purpose, such as a special purpose computer. When defined as a special purpose computer, the computer can also perform other processing, program execution or routines that are not part of the special purpose, while still being capable of operating for the special purpose. Alternatively, the operations may be processed by a general purpose computer selectively activated or configured by one or more computer programs stored in the computer memory, cache, or obtained over a network. When data is obtained over a network the data maybe processed by other computers on the network, e.g., a cloud of computing resources.

[0077] The embodiments of the present invention can also be defined as a machine that transforms data from one state to another state. The data may represent an article, that can be represented as an electronic signal and electronically manipulate data. The transformed data can, in some cases, be visually depicted on a display, representing the physical object that results from the transformation of data. The transformed data can be saved to storage generally, or in particular formats that enable the construction or depiction of a physical and tangible object. In some embodiments, the manipulation can be performed by a processor. In such an example, the processor thus transforms the data from one thing to another. Still further, the methods can be processed by one or more machines or processors that can be

connected over a network. Each machine can transform data from one state or thing to another, and can also process data, save data to storage, transmit data over a network, display the result, or communicate the result to another machine.

[0078] It should be further understood that the cell phasing embodiments as disclosed herein can be manufactured as part of a semiconductor device or chip. In the fabrication of semiconductor devices such as integrated circuits, memory cells, and the like, a series of manufacturing operations are performed to define features on a semiconductor wafer. The wafer includes integrated circuit devices in the form of multi-level structures defined on a silicon substrate. At a substrate level, transistor devices with diffusion regions are formed. In subsequent levels, interconnect metallization lines are patterned and electrically connected to the transistor devices to define a desired integrated circuit device. Also, patterned conductive layers are insulated from other conductive layers by dielectric materials.

[0079] While this invention has been described in terms of several embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. Therefore, it is intended that the present invention includes all such alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention.

CLAIMS

1. A semiconductor chip, comprising:

a plurality of cells positioned in an adjoining manner such that each of the plurality of cells has at least one coincident cell boundary with another of the plurality of cells, the plurality of cells including linear-shaped conductive features formed in a first chip level and linear-shaped conductive features formed in a second chip level, wherein the linear-shaped conductive features in both the first and second chip levels of the plurality of cells extend lengthwise in a common direction, wherein each linear-shaped conductive feature formed in the first chip level at any given coincident cell boundary is positioned according to a first virtual grate, wherein each linear-shaped conductive feature formed in the second chip level at any given coincident cell boundary is positioned according to a second virtual grate, and wherein the first and second virtual grates are commonly oriented to extend in the common direction, are indexed to a common spatial location, and have a ratio of their virtual grate pitches defined by a rational number.

2. A semiconductor chip as recited in claim 1, wherein the first virtual grate is defined by a first set of equally spaced parallel virtual lines extending across the first chip level, and wherein the second virtual grate is defined by a second set of equally spaced parallel virtual lines extending across the second chip level.

3. A semiconductor chip as recited in claim 1, wherein the first and second virtual grates periodically align with each other according to the ratio of their virtual grate pitches.

4. A semiconductor chip as recited in claim 1, wherein the rational number is 3/4.

5. A semiconductor chip as recited in claim 1, wherein the rational number is 2/3.

6. A semiconductor chip as recited in claim 1, wherein the rational number is 1/1.

7. A semiconductor chip as recited in claim 1, wherein the plurality of cells are placed in a row such that each coincident cell boundary of the plurality of cells is oriented in a height direction of the row.

8. A semiconductor chip as recited in claim 1, wherein a height of each of the plurality of cells is uniform, and wherein the height of each of the plurality of cells is measured in a direction parallel to virtual lines of the first and second virtual grates.

9. A semiconductor chip as recited in claim 1, wherein a width of each of the plurality of cells is an integer multiple of a pitch of the first virtual grate.

10. A semiconductor chip as recited in claim 9, wherein each of the plurality of cells has two cell boundaries oriented in a same direction as the first virtual grate, each of the two cell boundaries aligned with a separate virtual line of the first virtual grate.

11. A semiconductor chip as recited in claim 9, wherein each of the plurality of cells has two cell boundaries oriented in a same direction as the first virtual grate, each of the two cell boundaries located at a respective midpoint between adjacent virtual lines of the first virtual grate.

12. A semiconductor chip as recited in claim 1, wherein a width of each of the plurality of cells is an integer multiple of one-half of a pitch of the first virtual grate.

13. A semiconductor chip as recited in claim 12, wherein each of the plurality of cells has two cell boundaries oriented in a same direction as the first virtual grate, each of the two cell boundaries aligned with a separate virtual line of the first virtual grate.

14. A semiconductor chip as recited in claim 12, wherein each of the plurality of cells has two cell boundaries oriented in a same direction as the first virtual grate, each of the two cell boundaries located at a respective midpoint between adjacent virtual lines of the first virtual grate.

15. A semiconductor chip as recited in claim 1, wherein the first chip level is a gate level of the chip and the second chip level is a second interconnect level of the chip.

16. A semiconductor chip as recited in claim 1, wherein some of the plurality of cells include at least one linear-shaped conductive feature in either the first or second chip levels that is placed in a substantially centered manner along a cell boundary that is parallel to virtual lines of the first and second virtual grates.

17. A method for defining a layout of a semiconductor chip, comprising:

forming, using a computer, a plurality of cells to include linear-shaped conductive features formed in a first chip level and linear-shaped conductive features formed in a second chip level, wherein the linear-shaped conductive features in both the first and second chip levels of the plurality of cells extend lengthwise in a common direction;

positioning, using a computer, each linear-shaped conductive feature formed in the first chip level at any given potentially coincident cell boundary according to a first virtual grate;

positioning, using a computer, each linear-shaped conductive feature formed in the second chip level at any given potentially coincident cell boundary according to a second virtual grate, wherein the first and second virtual grates are commonly oriented to extend in the common direction, are indexed to a common spatial location, and have a ratio of their virtual grate pitches defined by a rational number; and

positioning, using a computer, the plurality of cells in an adjoining manner such that each of the plurality of cells has at least one coincident cell boundary with another of the plurality of cells.