CLAIMS

1. A sense amplifier, comprising:

an amplification circuit, configured to amplify a voltage difference between a bit line and a reference bit line when the sense amplifier is at an amplification stage; and

a controlled power circuit, connected to the amplification circuit, and configured to determine a drive current range according to a rated compensation voltage range between the bit line and the reference bit line, and supply a drive current to the amplification circuit according to the drive current range, so as to control the amplification circuit to pull a compensation voltage between the bit line and the reference bit line to be a rated compensation voltage at an offset cancellation stage; wherein the rated compensation voltage is within the rated compensation voltage range;

wherein the controlled power circuit is configured to determine the drive current range according to the rated compensation voltage range in the following manner:

testing the sense amplifier to obtain a mapping relationship between the compensation voltage between the bit line and the reference bit line and the drive current, and

determining the drive current range according to the mapping relationship and the rated compensation voltage range.

2. The sense amplifier of claim 1, wherein

the controlled power circuit comprises:

a first controlled power circuit, connected to a first terminal of the amplification circuit, and configured to supply the drive current to the amplification circuit;

a second controlled power circuit, connected to a second terminal of the amplification circuit, and configured to supply the drive current to the

amplification circuit; and

a controller, connected to the first controlled power circuit, further connected to the second controlled power circuit, and configured to determine the drive current range according to the rated compensation voltage range, and control the first controlled power circuit and the second controlled power circuit to supply the drive current to the amplification circuit according to the drive current range.

3. The sense amplifier of claim 2, wherein

the first controlled power circuit comprises:

N first controlled current sources, wherein each first controlled current source of the N first controlled current sources is provided with a control terminal, a first terminal, and a second terminal; the first terminal of the each first controlled current source is connected to a first power supply terminal, the second terminal of the each first controlled current source is connected to the first terminal of the amplification circuit, the control terminal of the each first controlled current source is connected to the controller, and N is a positive integer.

4. The sense amplifier of claim 3, wherein

the second controlled power circuit comprises:

N second controlled current sources, wherein each second controlled current source of the N second controlled current sources is provided with a control terminal, a first terminal, and a second terminal; the first terminal of the each second controlled current source is connected to a second power supply terminal, the second terminal of the each second controlled current source is connected to the second terminal of the amplification circuit, and the control terminal of the each second controlled current source is connected to the controller.

5. The sense amplifier of claim 4, wherein

the controller is configured to:

determine a first drive current range and a second drive current range

according to the rated compensation voltage range;

select at least one first target current source from the N first controlled current sources, and select at least one second target current source from the N second controlled current sources; wherein a total current provided by the at least one first target current source is within the first drive current range, and a total current provided by the at least one second target current source is within the second drive current range; and

generate a first control signal used to control the at least one first target current source to work, and generate a second control signal used to control the at least one second target current source to work; such that the first controlled power circuit controls the amplification circuit to pull voltages of the bit line and the reference bit line at the offset cancellation stage, and the second controlled power circuit controls the amplification circuit to pull the voltages of the bit line and the reference bit line at the offset cancellation stage.

6. The sense amplifier of claim 4 or 5, wherein

a drive current of an i^{th} first current source is $2^{i-1} \times I_b$, a drive current of a j^{th} second current source is $2^{j-1} \times I_b$, and I_b represents a unit current.

7. The sense amplifier of claim 4 or 5, wherein

the each first controlled current source is a P-type transistor, and the each second controlled current source is an N-type transistor.

8. The sense amplifier of any one of claims 2-5, wherein

the amplification circuit comprises:

at least one cross-coupled amplifier circuit, wherein each cross-coupled amplifier circuit of the at least one cross-coupled amplifier circuit is provided with a first terminal, a second terminal, a third terminal, and a fourth terminal; the first terminal of the each cross-coupled amplifier circuit is connected to an output terminal of the first controlled power circuit, the second terminal of the each cross-coupled amplifier circuit is connected to an output terminal of the second controlled power circuit, the third terminal of the each cross-coupled amplifier circuit is connected to the bit line, and the fourth terminal of the each

cross-coupled amplifier circuit is connected to the reference bit line.

9. The sense amplifier of claim 8, wherein

the each cross-coupled amplifier circuit comprises: a first transistor, a second transistor, a third transistor, a fourth transistor, a first switch, a second switch, a third switch, and a fourth switch;

a first terminal of the first transistor forms the first terminal of the each cross-coupled amplifier circuit, a second terminal of the second transistor forms the second terminal of the each cross-coupled amplifier circuit, a second terminal of the first transistor forms the third terminal of the each cross-coupled amplifier circuit, and a second terminal of the third transistor forms the fourth terminal of the each cross-coupled amplifier circuit;

the second terminal of the first transistor is connected to a first terminal of the second transistor, the second terminal of the third transistor is connected to a first terminal of the fourth transistor, the first terminal of the first transistor is connected to a first terminal of the third transistor, and the second terminal of the second transistor is connected to a second terminal of the fourth transistor;

a control terminal of the first transistor is connected to the second terminal of the third transistor, a control terminal of the second transistor is connected to the second terminal of the third transistor by the first switch, and the control terminal of the second transistor is connected to the first terminal of the second transistor by the third switch; and

a control terminal of the third transistor is connected to the second terminal of the first transistor, a control terminal of the fourth transistor is connected to the second terminal of the first transistor by the second switch, and the control terminal of the fourth transistor is connected to the first terminal of the fourth transistor by the fourth switch.

10. The sense amplifier of claim 9, wherein

the first transistor and the third transistor are P-type transistors, and the second transistor and the fourth transistor are N-type transistors.

11. A memory, comprising

the sense amplifier of claim 1 and a plurality of memory cells, wherein

a part of the plurality of memory cells constitutes a first storage array, another part of the plurality of memory cells constitutes a second storage array, the sense amplifier is located between the first storage array and the second storage array, a third terminal of the sense amplifier is connected to the bit line of the first storage array, and a fourth terminal of the sense amplifier is connected to the reference bit line of the second storage array.

12. A control method of a sense amplifier, wherein

the sense amplifier comprises an amplification circuit and a controlled power circuit;

obtaining a rated compensation voltage range between a bit line and a reference bit line;

determining a drive current range of the controlled power circuit according to the rated compensation voltage range; and

generating, according to the drive current range, a control signal used to control the amplification circuit, so as to control the amplification circuit to pull a compensation voltage between the bit line and the reference bit line to be a rated compensation voltage at an offset cancellation stage; wherein the rated compensation voltage is within the rated compensation voltage range;

wherein the determining a drive current range of the controlled power circuit according to the rated compensation voltage range comprises:

testing the sense amplifier to obtain a mapping relationship between the compensation voltage between the bit line and the reference bit line and a drive current; and

determining the drive current range according to the mapping relationship and the rated compensation voltage range.

13. The method of a sense amplifier of claim 12, wherein

the determining a drive current range of the controlled power circuit according to the rated compensation voltage range comprises:

determining a first drive current range and a second drive current range

according to the rated compensation voltage range.

14. The method of a sense amplifier of claim 13, wherein

the controlled power circuit comprises a first controlled power circuit and a second controlled power circuit; and

the generating, according to the drive current range, a control signal used to control the amplification circuit comprises:

selecting at least one first target current source from N first controlled current sources, and selecting at least one second target current source from N second controlled current sources, wherein a total current provided by the at least one first target current source is within the first drive current range, and a total current provided by the at least one second target current source is within the second drive current range; and

generating a first control signal used to control the at least one first target current source to work, and generating a second control signal used to control the at least one second target current source to work.

15. The sense amplifier of claim 1, wherein

in response to the amplification circuit pulling the compensation voltage between the bit line and the reference bit line to be the rated compensation voltage at the offset cancellation stage, a voltage of the bit line is decreased from an initial voltage of the bit line at a beginning of the offset cancellation stage to reach a minimal value, and then is increased to reach a first value, and a voltage of the reference bit line is successively decreased from an initial voltage of the reference bit line at the beginning of the offset cancellation stage to reach a second value, wherein a difference between the first value and the second value is the rated compensation voltage.