CLAIMS

Claim 1:

A tiled display panel, comprising:

a plurality of substrates, wherein each of the plurality of substrates has a display region and at least one boundary region, and the at least one boundary region is respectively located between the display region and a tiled boundary tiled by the plurality of substrates;

a plurality of liquid crystal pixels, arranged in an array in the display region;

a plurality of light-emitting diode (LED) pixels, arranged in an array in the at least one boundary region;

a plurality of light-emitting circuits, arranged in series in the at least one boundary region along a first direction and electrically connected to the plurality of LED pixels operable to provide a plurality of light-emitting signals for the plurality of LED pixels;

a plurality of first gate lines, spanning the display region along the first direction and for receiving a plurality of gate signals; and

a plurality of second gate lines, spanning the display region and the at least one boundary region along a second direction perpendicular to the first direction, wherein each of the plurality of second gate lines is electrically connected to one or part of the plurality of first gate lines, part of the plurality of liquid crystal pixels, and part of the plurality of LED pixels.

Claim 2:

The tiled display panel according to claim 1, wherein the plurality of light-emitting circuits are arranged in series between the plurality of LED pixels and the tiled boundary.

Claim 3:

The tiled display panel according to claim 1, further comprising:

a plurality of first break over lines, electrically connected to one of the plurality of second gate lines respectively, and extending along the first direction respectively to be electrically connected to a first-level light-emitting circuit and a next-level light-emitting circuit of the plurality of light-emitting circuits.

Claim 4:

The tiled display panel according to claim 3, wherein a configuration direction of the first-level light-emitting circuit relative to the second gate line electrically connected to each of the plurality of first break over lines is opposite to a configuration direction of the next-level light-emitting circuit relative to the second gate line electrically connected to each of the plurality of first break over lines.

Claim 5:

The tiled display panel according to claim 1, further comprising:

a plurality of second break over lines, electrically connected to one of the plurality of second gate lines respectively, and extending along the first direction to be electrically connected to a first-level light-emitting circuit of the plurality of light-emitting circuits respectively; and

a plurality of third gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of third gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first

gate line electrically connected to each of the third gate lines is closer to the at least one boundary region than the first gate line electrically connected to the plurality of adjacent second gate lines.

Claim 6:

The tiled display panel according to claim 1, further comprising:

a plurality of third break over lines, electrically connected to one of the plurality of second gate lines respectively, and extending along the first direction to be electrically connected to a next-level light-emitting circuit of the plurality of light-emitting circuits respectively; and

a plurality of fourth gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of fourth gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first gate line electrically connected to each of the plurality of fourth gate lines is further away from the at least one boundary region than the first gate lines electrically connected to the plurality of adjacent second gate lines.

Claim 7:

The tiled display panel according to claim 1, further comprising:

a plurality of fifth gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of fifth gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first

gate line electrically connected to each of the fifth gate lines is closer to the at least one boundary region than the plurality of first gate lines electrically connected to the plurality of adjacent second gate lines; and

a plurality of sixth gate lines, spanning the display region and the at least one boundary region along the second direction, wherein each of the plurality of sixth gate lines is located between two adjacent second gate lines and is electrically connected to one of the plurality of first gate lines and one of the plurality of light-emitting circuits, and the first gate line electrically connected to each of the plurality of sixth gate lines is further away from the at least one boundary region than the plurality of first gate lines electrically connected to the plurality of adjacent second gate lines.

Claim 8:

The tiled display panel according to claim 1, wherein each of the plurality of liquid crystal pixels comprises:

a switch transistor, having a first terminal for receiving a pixel data voltage, a control terminal for receiving a first gate signal of the plurality of gate signals, and a second terminal;

a first pixel capacitance, coupled between the second terminal of the switch transistor and a first common terminal; and

a second pixel capacitance, coupled between the second terminal of the switch transistor and a second common terminal.

Claim 9:

The tiled display panel according to claim 1, wherein each of the plurality of

LED pixels comprises:

a light-emitting diode (LED), having an anode and a cathode for receiving a system low voltage;

a first transistor, having a first terminal for receiving a pixel data voltage, a control terminal for receiving a first gate signal of the plurality of gate signals, and a second terminal;

a second transistor, having a first terminal for receiving a system high voltage, a control terminal coupled to the second terminal of the first transistor, and a second terminal;

a third transistor, having a first terminal coupled to the second terminal of the second transistor, a control terminal for receiving a corresponding one of the plurality of light-emitting signals, and a second terminal coupled to the anode of the LED; and

a first capacitance, coupled between the control terminal of the second transistor and the second terminal of the second transistor.

Claim 10:

The tiled display panel according to claim 1, wherein each of the plurality of LED pixels includes:

an LED, having an anode and a cathode for receiving a system low voltage;

a fourth transistor, having a first terminal for receiving a pixel data voltage, a control terminal for receiving a first gate signal of the plurality of gate signals, and a second terminal;

a fifth transistor, having a first terminal, a control terminal coupled to the second terminal of the fourth transistor, and a second terminal;

a second capacitance, coupled between the first terminal of the fifth transistor

and the control terminal of the fifth transistor;

a sixth transistor, having a first terminal for receiving a reference voltage, a control terminal for receiving the first gate signal, and a second terminal coupled to the first terminal of the fifth transistor;

a seventh transistor, having a first terminal for receiving a system high voltage, a control terminal for receiving a corresponding one of the plurality of light-emitting signals, and a second terminal coupled to the first terminal of the fifth transistor; and

an eighth transistor, having a first terminal coupled to the second terminal of the fifth transistor, a control terminal for receiving a corresponding one of the plurality of light-emitting signals, and a second terminal coupled to the anode of the LED.

Claim 11:

The tiled display panel according to claim 1, wherein each of the plurality of light-emitting circuits comprises:

a ninth transistor, having a first terminal for receiving a gate high voltage, a control terminal for receiving a second gate signal of the plurality of gate signals, and a second terminal coupled to a corresponding one of the plurality of light-emitting signals; and

a tenth transistor, having a first terminal coupled to the second terminal of the ninth transistor, a control terminal for receiving a third gate signal of the plurality of gate signals, and a second terminal for receiving a gate low level.

Claim 12:

The tiled display panel according to claim 11, wherein each of the plurality of

light-emitting circuits further comprises:

an eleventh transistor, having a first terminal for receiving one of a plurality of clock signals, a control terminal coupled to the second terminal of the ninth transistor, and a control terminal coupled to the corresponding one of the plurality of light-emitting signals.

Claim 13:

The tiled display panel according to claim 11, wherein each of the plurality of light-emitting circuits comprises:

a third capacitance, coupleable between the second terminal of the ninth transistor and one of a reference voltage and the gate low level.

Claim 14:

The tiled display panel according to claim 11, wherein each of the plurality of light-emitting circuits comprises:

a twelfth transistor, having a first terminal coupled to the second terminal of the ninth transistor, a control terminal for receiving a fourth gate signal of the plurality of gate signals, and a second terminal for receiving the gate low level.

Claim 15:

The tiled display panel according to claim 1, further comprising:

a plurality of clock lines, for receiving a plurality of clock signals and electrically connected to the plurality of light-emitting circuits operable to transmit the plurality of clock signals to the plurality of light-emitting circuits respectively.

Claim 16:

The tiled display panel according to claim 1, wherein a material of the plurality of substrates comprises one of a P-type amorphous silicon (a-Si) substrate, an N-type amorphous silicon (a-Si) substrate, an indium gallium zinc oxide (IGZO) substrate, and a low-temperature polycrystalline silicon (LTPS) substrate.

Claim 17:

The tiled display panel according to claim 1, wherein the plurality of LED pixels comprise a plurality of red LED pixels, a plurality of green LED pixels, and a plurality of blue LED pixels.

Claim 18:

A tiled display panel, comprising:

a plurality of substrates, wherein each of the plurality of substrates has a display region and at least one boundary region, and the at least one boundary region is respectively located between the display region and a tiled boundary tiled by the plurality of substrates;

a plurality of liquid crystal pixels, arranged in an array in the display region;

a plurality of LED pixels, arranged in an array in the at least one boundary region;

at least one light-emitting driving line, for receiving at least one light-emitting signal, spanning the at least one boundary region along a first direction, and electrically connected to the plurality of LED pixels operable to provide the at least one light-emitting signal for the plurality of LED pixels;

a plurality of first gate lines, spanning the display region along the first direction and for receiving a plurality of gate signals; and

a plurality of second gate lines, spanning the display region and the at least one boundary region along a second direction perpendicular to the first direction, wherein each of the plurality of second gate lines is electrically connected to one or part of the plurality of first gate lines, part of the plurality of liquid crystal pixels, and part of the plurality of LED pixels.

Claim 19:

The tiled display panel according to claim 18, wherein the at least one light-emitting driving line comprises a light-emitting driving line, the light-emitting driving line configured to receive a light-emitting signal and being electrically connected to the plurality of LED pixels operable to provide the light-emitting signal for the plurality of LED pixels.

Claim 20:

The tiled display panel according to claim 19, wherein the plurality of LED pixels are configured to be lit up by the light-emitting signal during a data enable period of a frame period.

Claim 21:

The tiled display panel according to claim 19, wherein the plurality of LED pixels are configured to be lit up by the light-emitting signal during a vertical blank period of a frame period.

Claim 22:

The tiled display panel according to claim 18, wherein the plurality of LED

pixels comprise a plurality of red LED pixels, a plurality of green LED pixels, and a plurality of blue LED pixels, and the at least one light-emitting driving line comprises a first light-emitting driving line, a second light-emitting driving line, and a third light-emitting driving line,

wherein the first light-emitting driving line is configured to receive a red light-emitting signal and is electrically connected to the plurality of red LED pixels operable to provide the red light-emitting signal for the plurality of red LED pixels,

wherein the second light-emitting driving line is configured to receive a green light-emitting signal and is electrically connected to the plurality of green LED pixels operable to provide the green light-emitting signal for the plurality of green LED pixels, and

wherein the third light-emitting driving line is configured to receive a blue light-emitting signal and is electrically connected to the plurality of blue LED pixels operable to provide the blue light-emitting signal for the plurality of blue LED pixels.

Claim 23:

The tiled display panel according to claim 18, wherein the at least one light-emitting driving line comprises a plurality of light-emitting driving lines coupled to the plurality of LED pixels operable to light up the plurality of LED pixels in groups.

Claim 24:

The tiled display panel according to claim 18, wherein the plurality of light-emitting driving lines are disposed between the plurality of LED pixels and the tiled boundary.