What is claimed : ~~CLAIMS~~

1. A method, implemented at a computer system that includes one or more processors, for performing breakpoint detection via a cache, the method comprising:

detecting an occurrence of a memory access; and

based at least on detecting the occurrence of the memory access, identifying whether any cache line of the cache matches an address associated with the memory access, and

when a cache line does match the address associated with the memory access, determining that no breakpoint was encountered; or

when no cache line matches the address associated with the memory access, identifying whether any cache line matches the address associated with the memory access when one or more flag bits are ignored, and

when a cache line does match the address associated with the memory access when the one or more flag bits are ignored, performing a check for whether a breakpoint was encountered; or

when no cache line matches the address associated with the memory access when the one or more flag bits are ignored,

processing a cache miss; and

determining whether a cache line imported into the cache based on processing the cache miss overlaps with any address from a monitoring collection .

~~2. The method of claim 1, further comprising, when no cache line matches the address associated with the memory access when the one or more flag bits are ignored, determining whether a cache line imported into the cache based on processing the cache miss overlaps with any address from a monitoring collection.~~

2.~~3.~~ The method of claim 1~~2~~, further comprising, when the cache line imported into the cache overlaps with an address from the monitoring collection, setting a flag bit on the cache line.

3. The method od claim 1, wherein performing the check for whether a breakpoint was encountered comprises determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.

~~4. The method of claim 1, wherein performing the check for whether a breakpoint was encountered comprises determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.~~

4.~~5.~~ The method of claim 3~~4~~, wherein the monitoring collection is stored in system memory.

5.~~6.~~ The method of claim 3~~4~~, wherein the monitoring collection is stored in a processor memory.

6.~~7.~~ The method of claim 5~~6~~, wherein the processor memory comprises a cache coherence protocol directory.

7. The method of claim 1, wherein performing the check for whether a breakpoint was encountered comprises consulting a translation look aside buffer to determine if a page table corresponding to the memory address contains any monitored memory address.

~~8. The method of claim 1, wherein performing the check for whether a breakpoint was encountered comprises consulting a translation look aside buffer to determine if a page table corresponding to the memory address contains any monitored memory address.~~

8.~~9.~~ The method of claim 7~~8~~, further comprising, when the page table corresponding to the memory address does contain a monitored memory address, determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.

9.~~10.~~ The method of claim 1, wherein performing the check for whether a breakpoint was encountered compromises placing an address of the cache line into a hardware debug register.

10.~~11.~~ A computer system, comprising:

one or more processors; and

one or more hardware storage devices ~~computer-readable media~~ having stored thereon computer-executable instructions that configure the one or more processors to perform breakpoint detection via a cache comprising a plurality of cache lines, including at least:

detecting an occurrence of a memory access at a particular memory address; and

based at least on detecting the occurrence of the memory access, identifying whether any cache line of the cache matches the particular memory ~~an~~ address associated with the memory access by comparing a corresponding memory address associated with each of the plurality of cache lines with the particular memory address, and

when a cache line does match the particular memory address associated with the memory access, determining that no breakpoint was encountered; or

when no cache line matches the particular memory address associated with the memory

access, identifying whether any cache line matches the particular memory address associated

with the memory access when one or more ~~flag~~ bits of each corresponding memory address are ignored, and

when a cache line does match the particular memory address associated with the

memory access when the one or more ~~flag~~ bits of each corresponding memory address are ignored,

performing a check for whether a breakpoint was encountered, wherein the one or more bits indicate whether there is a breakpoint on a memory address overlapping with the cache line ; or

when no cache line matches the particular memory address associated with the memory

access when the one or more ~~flag~~ bits are of each corresponding memory address ignored, processing a cache miss.

11.~~12.~~ The computer system of claim 10~~11~~, wherein the one or more processors comprise the hardware storage devices ~~computer-readable media~~ and the cache, and wherein the computer-executable instructions comprise processor microcode.

12. A method, implemented at a computer system that includes one or more processors and a system memory, for configuring a cache for breakpoint detection, the method comprising :

identifying a particular memory address in the system memory that is to be monitored; and

based at least on identifying the particular memory address in the system memory to be monitored, determining whether a cache line comprising a tag field storing the particular memory address already exists in a cache of the system memory, the cache comprising a plurality of cache lines that each comprises a corresponding tag field storing a corresponding memory address and a corresponding data block storing cached data for the corresponding memory address, and

when the cache line comprising the tag field storing the particular memory address already exists in the cache, setting a flag in the tag field of the cache line, wherein setting the flag in the tag field of the cache line comprises modifying at least one bit in the tag field that is used to store the particular memory address within the tag field.

13. The method of claim 12, wherein setting the flag in the tag field of the cache line comprises setting a bit that is reserved based on the tag field containing more bits than are needed to address a full address space accessible by the one or more processors.

14. The method of claim 12, wherein setting the flag in the tag field of the cache line comprises setting a bit that is reserved based on memory alignment.

15. The method of claim 12, wherein setting the flag in the tag field of the cache line comprises setting a bit that is reserved at boot time based on an amount of available physical memory.

16. The method of claim 12, further comprising setting one or more flags in the tag field of the cache line that indicate a breakpoint type.

17. The method of claim 12, the method also comprising adding the memory address to a collection of monitored addresses stored in an on-processor memory.

18. The method of claim 12, the method also comprising adding the memory address to a collection of monitored addresses stored in system memory.

19. The method of claim 12, further comprising configuring a page table entry for a page table to indicate that one or more of the page table or a child page table contains a monitored memory address.

~~13. The computer system of claim 11, the computer-executable instructions also configuring the one or more processors to determine whether a cache line imported into the cache based on processing the cache miss overlaps with any address from a monitoring~~

~~collection when no cache line matches the address associated with the memory access when the one or more flag bits are ignored.~~

~~14. The computer system of claim 11, wherein performing the check for whether a breakpoint was encountered comprises determining if any address from a monitoring collection overlaps with a plurality of memory addresses covered by the cache line.~~

~~15. The computer system of claim 14, wherein the monitoring collection is stored in a processor memory.~~