CONDUCTORS FOR MICROELECTRONIC CIRCUITS AND METHOD OF MANUFACTURE

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is related to coaxial conductors and, more particularly, to processes of integrating coaxial conductors onto integrated circuit chips.

Background Description

Coaxial cables are well known. Miniature coaxial cables are also well known. Coaxial cables are widely used for low loss data transmission. Signals transmitted on coaxial cables are shielded from exterior noise that might otherwise interfere with signals on an unshielded line.

To reduce signal loss, signals transmitted on coaxial cable require termination for impedance matching. Typical impedance matching termination on an integrated circuit (IC) chip is a resistor tied at one end to a supply.

Very few IC processes include coaxial signal distribution conductors because of the difficulty in fabricating coaxial structures in IC processes. Further, prior art coaxial conductors have irregularities in spacing between the core conductor and the outer shield conductor. These irregularities

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lead to nonuniform characteristic impedance along the conductor. The nonuniformity in the characteristic impedance introduces noise from reflections and attenuations into signals on the core conductor.

Thus there is a need for coaxial conductors in ICs that have uniform spacing between the core conductor and the outer shield conductor.

SUMMARY OF THE INVENTION

It is a purpose of the invention to reduce noise on signals transmitted on integrated circuit chips.

It is another purpose of the present invention to simplify fabrication of coaxial conductors on integrated circuit chips.

The present invention is an integrated circuit (IC) conductor and the process of making the conductor. In a first preferred embodiment, the conductor is a coaxial conductor. Multiple conductors may be included in the first preferred embodiment to form, for example triaxial conductors. In a second preferred embodiment, the conductor is a clad conductor. In a third preferred embodiment, the conductor is a monofilament conductor.

First, in all three preferred embodiments, a trench is formed in a dielectric layer. An outer material layer is deposited on the dielectric layer and in the trench. The deposited outer layer is thick enough that as it forms along the sidewalls of the trench, it builds up along the surface edges of

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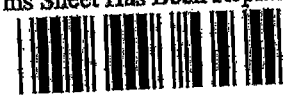

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the trench until it merges together in a seam over the trench forming a void under the seam. The outer material layer is conducting material for the first embodiment coaxial conductor, a cladding material for the second embodiment clad conductor and dielectric for the third embodiment monofilament conductor. For the first embodiment, an inner dielectric liner layer is formed on the walls of the void and a core conductor is formed in the liner layer to form the coaxial conductor. The void is filled with a conductor for both the clad and monofilament conductors.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figures 1A-C show a trench formed for first preferred embodiment, coaxial conductor;

Figures 2A-C show the outer conductor an a void formed therein in the trench of Figs 1A-C;

Figures 3A-C show accesses opened through the outer conductor of Figs 2A-C;

Figures 4A-C show a dielectric liner formed on the outer conductor in the void;

Figures 5A-C show the core conductor filling the void in the dielectric liner;

Figures 6A-C show the first preferred embodiment coaxial conductor;

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Figures 7A-C show a cladding layer formed in the trench of Figs. 1A-C in the second preferred embodiment clad conductor;

Figures 8A-C show accesses opened through the cladding layer of Figs 7A-C to the void;

Figures 9A-C show conductor material filling the void;

Figures 10A-C show the second preferred embodiment clad conductor;

Figures 11A-C show an outer dielectric layer with a void therein in the trench of Figs. 1A-1C;

Figures 12A-C show accesses opened through the outer dielectric layer to the void of Figs 11A-C;

Figures 13A-C show conductor material filling the void;

Figures 14A-C show the third preferred embodiment monofilament conductor.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

The present invention is a family of dielectric encased conductors for integrated circuit (IC) chips and the method of making the conductors on IC chips. In one preferred embodiment the conductor is a coaxial conductor. In a second preferred embodiment, the conductor is a clad conductor. In a third preferred embodiment, the conductor is a monofilament conductor.

Figures 1A-C to 6A-C show the first preferred embodiment conductor, a coaxial conductor for microelectronic circuits, after preferred steps of

making the conductor. Figures 1A-6A are a plan view, Figs. 1B-6B are respective cross-sectional views through B-B and Figs. 1C-6C are respective cross-sectional views through C-C.

First, in Figs. 1A-1C, a .1 micron (μm) to 100μm thick outer dielectric layer 100 of insulating material is formed on a semiconductor wafer 102. Preferably the insulating material is silicon oxide, the layer 100 is slightly thicker than 5000Å and the wafer 102 is silicon. Next, a 5000Å deep trench 104 is formed in the outer dielectric layer 100, preferably using lithography and reactive ion etching (RIE). The trench 104 defines the size and shape of an outer conductor. Alternatively, any suitable etching technique may be substituted for RIE. Preferably, although not required, the walls 106 of the trench 104 are bowed out, so that the trench's width is greater at its middle than at its top. Preferably, each trench's aspect ratio (height/width) is ≥1.

Next, in Figs. 2A-C, an outer conductor 108 is formed in the trench 104. The outer conductor 108 is analogous to the wire mesh shield in state of the art coaxial cables. To form the outer conductor 108, a very thin seed layer 112 of TiN over Ti is deposited on the outer dielectric layer 100 and in the trench 104. Preferably, the seed layer thickness at the bottom 110 of the trench 104 should be, depending on the trench dimensions, 30-3000Å TiN, preferably 50Å, on 30-3000Å Ti, preferably 50Å.

Then, the outer conductor 108 is formed on the seed layer. Preferably, the outer conductor 108 is a 3000Å tungsten layer deposited by chemical vapor

deposition (CVD). Preferably, the deposited conductor material thickness, essentially, is uniform on the field and in the trench 104, on its sides 106 and bottom 110. Deposition of the outer conductor 108 continues until the material build up along the trench's sidewalls 106, is thick enough to seam together, merging together to form seam 116, while leaving a void 118 beneath and running along the length of the seam. Thus, the deposited conductor material must be sufficiently thick that the seam forms at the top of the trench, while a void or "low density" material remains embedded in the outer conductor material, along the whole length of the seam. Excess metal is removed from the field, (the wafer's surface around the trench 104) preferably by chem-mech polishing (CMP) the wafer.

Optionally, a capping dielectric layer may be formed on the outer conductor 108 at this point. However, preferably, the capping dielectric layer is formed later in the process, after an inner dielectric & conductor are formed.

After forming the outer conductor 108, in Figs. 3A-C, an access 120, 122 is opened to the void 118 at each end of the outer conductor 108 and the void 118 is widened along the length of the outer conductor 108. First, the access holes 120, 122 are etched in the ends of the outer conductor 108 to expose the void 118. Then, the void 118 is etched to enlarge its diameter to 3000 Å. In the preferred embodiment, the outer conductor material, W, is etched with HNO_3/HF. Optionally, if the coaxial line is to be connected to a lower level, the access hole may be sub-etched below the bottom of the outer

conductor, preferably using reactive ion etching (RIE) to etch to a conductor (not shown) below.

Next, in Figs. 4A-C, a dielectric liner 124 is formed lining the void 118. Preferably, an 1000Å silicon oxide layer 124 is formed on the inner surface 126 using CVD. The liner 124 must completely coat the inner surface 126 of the void 118 without plugging it. The dielectric liner 124 is insulates the preferred coaxial conductor's inner conducting core from the outer conductor 108. In the preferred embodiment, as the dielectric liner 124 is formed, a dielectric cap 128 forms, simultaneously, on the top surface of the outer conductor 108.

Optionally, after forming the dielectric liner 124, dielectric at the bottom of the access holes 120, 122 may be removed, exposing a lower level conductor (not shown) using an anistropic etch. Additionally, contacts may be opened through the dielectric cap 128. So, the dielectric is patterned using normal photo-lithographic processes and anisotropically etched, e.g., RIE. Alternately, a blanket RIE without patterning may be used to remove the dielectric from both the bottom of the access holes 120, 122 and surface of the wafer.

Next, in Figs. 5A-C, a core conductor 130 is formed in and along the length of the inner dielectric 124. Preferably, the core conductor 130 is deposited by CVD, first depositing a seed layer of TiN followed by CVD of tungsten. Optionally, if the conductor length exceeds the CVD fill capability, intermediate access holes (not shown), identical to 120, 122 formed at each end in the

present example, may be included, as required, along the length of the trench 104.

Finally, in Figs. 6A-C, excess conductor is removed from the surface 132. The excess conductor may be removed using an appropriate CMP or RIE technique. Once the coaxial conductor is completed, the outer and core conductors can be contacted by standard semiconductor circuit connection methods.

In an alternate example of this first preferred embodiment, a 7000Å deep and 2500Å wide trench is formed in a surface SiO_2 layer located on a silicon wafer. A 6000Å outer conductor layer of polysilicon may be formed on the wafer and over the 7000Å by 2500Å trench using CVD. Excess conductor may be removed from the field using CMP. As in the first preferred embodiment, the polysilicon seams above a void in the trench. Access holes are opened through the polysilicon outer conductor at each end of the trench. An isotropic etchant such as a mixture of NH_4OH, H_2O_2 in deionized water may be used to etch the polysilicon from within the void to enlarge the void diameter to 500Å. A 150Å dielectric liner, of Si_3N_4 is deposited in the void using CVD. The liner must completely coat the inner polysilicon surface without plugging the void, leaving a void diameter of 200Å. Finally, an As doped polysilicon core conductor is deposited to fill the void.

Further, this first preferred embodiment may be used for multiple levels of wiring, by repeating the steps depicted in Figs. 1A-C to 6A-C on the surface above the structure in Figs 6A-C.

In another alternate embodiment of this first preferred embodiment the method of forming the

coaxial conductor is extended to three or more coaxial conducting layers, e.g., three conductors forming a triaxial conductor. In this alternate embodiment, a deeper & wider trench may be combined with thinner dielectric and conductor layers such that the second conductor (the core conductor in the first preferred embodiment) lines, but does not completely fill the void 118.

Then, for this alternate embodiment, a third dielectric layer (not shown) is deposited on the second conductor, leaving the void 118 open for the third conductor. Additional dielectric and conducting layers may be identically formed as desired until the void 118 has been filled with a core conductor or dielectric. As with the first preferred embodiment, once the core coaxial conductor is completed, the coaxial conductors can be contacted by standard semiconductor circuit connection methods.

Figures 7A-C to 10A-C show the second preferred embodiment conductor, a clad conductor for microelectronic circuits, after preferred steps of making the conductor. Figures 7A-10A are a plan view, Figs. 7B-10B are respective cross-sectional views through B-B and Figs. 7C-10C are respective cross-sectional views through C-C.

The first step in the second preferred embodiment is to form a trench 104 in a surface dielectric layer 100 in Figs. 1A-C.

After defining the trench 104, in Figs. 7A-C, a cladding layer 200 is deposited by CVD. The cladding layer may be conductive, wherein tantalum is deposited or, dielectric wherein silicon nitride is

deposited. Alternately, the conductive cladding material may be Al, Mg, a refractory metal or a compound thereof, including, for example, nitrides, silicides, carbides and borides.

As with the outer conductor 108 in Figs. 2A-C, the cladding layer field thickness and thickness on the sides & bottom of the trench, preferably, are identical. As with the outer conductor 108, cladding layer 200 deposition continues until the material build up along the trench's sidewalls 202, is thick enough to seam together, merging together to form seam 204, while leaving a void 206 beneath and running along the length of the seam 204. Thus, the deposited conductor material must be sufficiently thick that the seam 204 forms at the top of the trench 104, while a void 206 or "low density" material remains embedded in the cladding material, along the whole length of the seam 204. As with the first preferred embodiment, optionally, a capping dielectric layer may be formed at this point, or after the core conductor is formed.

Next in Figs. 8A-C, as in Figs. 3A-C, an access 210, 212 is opened to the void 206 at each end of the cladding layer 200 and the void 206 is enlarged along the length of the cladding layer 200. Access holes 210, 212 are etched in the ends of the cladding layer 200 to expose the void 206. After opening the access holes 210, 212 the void 200 is etched to enlarge it to 3000 Å. In the preferred embodiment, the cladding layer 200 is etched with HNO_3/HF for Ta or hot H_3PO_4 for silicon nitride cladding. Optionally, if the coaxial line is to be connected to a lower level, the access hole may be

sub-etched below the bottom of the outer conductor, preferably using reactive ion etching (RIE) to connect to a conductor (not shown) below it.

Next, in Figs. 9A-C, the core conductor 214 is deposited along the length of the void 206. Preferably, the core conductor 214 material is Cu deposited by plating or CVD. Alternately, the core material may be Al, Co, W, Si, doped Si or Mo. Optionally, as with the first preferred embodiment, if the conductor length exceeds the CVD fill capability, intermediate access holes (not shown), identical to those formed 210, 212 at each end in the present example, may be included, as required, along the length of the trench 104.

Finally, in Figs. 10A-C, excess conductor is removed from the surface 216. The excess conductor may be removed using an appropriate CMP or RIE technique. Once the clad conductor is completed, the conductor may be contacted by standard semiconductor circuit connection methods.

Figures 11A-C to 14A-C show the third preferred embodiment conductor, a monofilament conductor for microelectronic circuits, after preferred steps of making the conductor. Figures 11A-14A are a plan view, Figs. 11B-14B are respective cross-sectional views through B-B and Figs. 11C-14C are respective cross-sectional views through C-C.

The first step in the third preferred embodiment is to form a trench 104 in a surface dielectric layer 100 in Figs. 1A-C.

After defining the trench 104, in Figs. 11A-C, a second outer dielectric 300, preferably of silicon oxide is formed on the wafer, preferably by CVD. As

with the outer conductor 108 in Figs. 2A-C, the second outer dielectric 300 thickness in the field and on the sides and bottom of the trench, preferably, are identical. As with the outer conductor 108, second outer dielectric 300 deposition continues until the material build up along the trench's sidewalls 302, is thick enough to seam together, merging together to form seam 304, while leaving a void 306 beneath and running along the length of the seam 304. Thus, the deposited second dielectric material must be sufficiently thick that the seam 304 forms at the top of the trench 104, while a void 306 or "low density" material remains embedded in the second dielectric material, along the whole length of the seam 304.

Optionally, excess dielectric may be removed from the field of the wafer (outside the trench) by CMP or RIE. As with the first preferred embodiment, optionally, a capping dielectric layer may be formed at this point, or after the monofilament conductor is formed.

Next in Figs. 12A-C, as in Figs. 3A-C, an access 308, 310 is opened to the void 306 at each end of the second outer dielectric 300 and the void 306 is enlarged along the length of the second outer dielectric 300. Access holes 308, 310 are etched in the ends of the second outer dielectric 300 to expose the void 306. After opening the access holes 308, 310 the void 306 is etched with HF to enlarge it. Optionally, if the monofilament line is to be connected to a lower level, the access hole may be sub-etched below the bottom of the trench, preferably using reactive ion etching (RIE) to open

a contact to connect the monofilament to a conductor (not shown) below it.

Next, in Figs. 13A-C, the monofilament conductor 312 is formed along the length of the void 306. Preferably, the monofilament conductor 312 material is Cu or W formed by depositing a seed layer of TiN and then depositing W on the seed layer, preferably by CVD. Optionally, as with the first preferred embodiment, if the monofilament conductor length exceeds the CVD fill capability, intermediate access holes (not shown), identical to those formed 308, 310 at each end in the present example, may be included, as required, along the length of the trench 104.

Finally, in Figs. 14A-C, excess conductor is removed from the surface 312. The excess conductor may be removed using an appropriate CMP or RIE technique. Once the monofilament conductor is completed, the conductor may be contacted by standard semiconductor circuit connection methods.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

We Claim:

1. A method of making a conductor on an integrated circuit (IC) comprising the steps of:

a) forming a trench in an insulating material;

b) forming an outer layer of a first material on said insulating material and in said trench, said outer layer seaming together over a void in said trench;

c) opening access holes through said outer layer to said void; and

d) filling said void with conducting material.

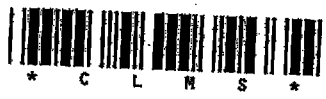
2. The method of claim 1 wherein said trench is formed by etching partially through said insulating material and said trench's depth exceeds its width.

3. The method of claim 1 wherein said insulating material is an SiO_2 layer and said trench is formed by reactive ion etching said SiO_2 layer.

4. The method of claim 1 wherein said trench is wider at it bottom than at its top.

5. The method of claim 1 wherein said trench is bowed out at its middle.

6. The method of claim 2 wherein said insulating material is an SiO_2 layer and said trench is formed by reactive ion etching said SiO_2 layer.



7. The method of claim 1 wherein the step (c) of opening the access holes further comprises etching the void to widen it.

8. The method of claim 1 wherein the step (d) of filling the void with conducting material comprises the steps of:

i) depositing a seed layer;

ii) depositing a conductor layer on said seed layer; and,

iii) removing excess said deposited conductor layer material and seed layer material from said insulating material.

9. The method of claim 8 wherein the seed layer is a 50Å TiN layer on a 50Å Ti layer and the conductor layer material is W.

10. The method of claim 9 wherein said conductor is a monofilament conductor and said first material is a dielectric material.

11. The method of claim 10 wherein the dielectric material is SiO_2 deposited using CVD and the void is etched with HF to open it to 3000Å.

12. The method of claim 1 wherein said conductor is a coaxial conductor, said first material is a conducting material and further comprising, before the step (d) of filling the void, the step of:

c1) lining said void with an inner dielectric.

13. The method of claim 12 wherein the step (b) of forming the outer conducting layer comprises the steps of:

i) depositing an outer conductor seed layer;

ii) depositing an outer conductor layer on said outer conductor seed layer; and,

iii) removing excess said deposited outer conductor layer material and outer conductor seed layer material from said insulating material.

14. The method of claim 13 wherein the outer conductor seed layer is a 50Å TiN layer on a 50Å Ti layer, the outer conductor layer material is W and the void is etched with HNO_3/HF to widen it to 3000Å.

15. The method of claim 1 wherein said conductor is a clad conductor, said first material is a cladding material of Ta and the Ta cladding layer is etched with HNO_3/HF to widen it to 3000Å.

16. The method of claim 1 wherein said first material is silicon nitride deposited using CVD and the void is etched with H_3PO_4 to widen it to 3000Å.

17. A method of making a coaxial conductor on an integrated circuit (IC) comprising the steps of:

a) etching a trench in an insulating layer;

b) depositing an outer conductor layer on said insulating layer and in said trench, said outer conductor layer seaming together in said trench over a void;

c) removing excess outer conductor material from said insulating layer;

d) opening access holes through said outer conductor layer to said void;

e) etching said outer conductor material in said void to widen said void;

f) lining said void with an inner dielectric;

g) depositing a core conductor, said core conductor filling said void; and

h) removing excess core conductor material from said insulating layer.

18. The method of claim 17 wherein said insulating layer is an SiO_2 layer and the step (b) of depositing the outer conductor comprises the steps of:

i) depositing an outer conductor seed layer;

ii) depositing an outer conductor layer on said outer conductor seed layer; and,

iii) removing excess said deposited outer conductor layer material and outer conductor seed layer material from said SiO_2.

19. The method of claim 18 wherein the inner dielectric is SiO_2 and the step (h) of depositing the core conductor comprises the steps of:

i) depositing a seed layer;

ii) depositing conductor material on said seed layer; and,

iii) removing excess said deposited conductor material and seed layer material from said SiO_2.

20. The method of claim 19 wherein the core conductor seed layer and the outer conductor seed layer are each a 50Å TiN layer on a 50Å Ti layer, the core conductor and outer conductor material is W and the void is etched with HNO_3/HF to widen it to 3000Å.

21. The method of claim 17 wherein the coaxial conductor is a triaxial conductor and further comprising, before the step (g) of depositing the core conductor, the steps of:

f1) lining said void with an inner conductor layer;

f2) opening access holes through said inner conductor layer;

f3) lining said void with a second inner dielectric; and

f4) opening access holes through said second inner dielectric layer.

22. A method of making a clad conductor on an integrated circuit (IC) comprising the steps of:

a) etching a trench in an insulating layer;

b) depositing a cladding layer on said insulating layer and in said trench, said cladding layer seaming together in said trench over a void;

c) removing excess cladding material from said insulating layer;

d) etching access holes through said cladding layer to said void;

e) etching the surface of said cladding layer in said void to widen said void;

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f) depositing a seed layer, said seed layer lining said void;

g) depositing conductor material on said seed layer; and,

h) removing excess said deposited conductor material and seed layer material from said SiO_2.

23. The method of claim 22 wherein said cladding layer is a layer of Ta and the Ta cladding layer is etched with HNO_3/HF to widen the void to 3000Å.

24. The method of claim 23 wherein said cladding layer is a layer of silicon nitride deposited using CVD and the silicon nitride cladding layer is etched with H_3PO_4 to widen the void to 3000Å.

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