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AN ANTI-PUNCHTHOUGH ION IMPLANTATION FOR SUB-HALF MICRON CHANNEL LENGTH MOSFET DEVICES

ABSTRACT

A method for forming a MOSFET device, with reduced exposure to source and drain leakage currents, that can arise due to a junction depletion punchthrough phenomena, has been developed. An anti-punchthrough, ion implantation, is performed in a confined area below the channel region. The ability to confine the area used for the anti-punchthrough region, results in protection against leakage, however with only a minimum of parasitic capacitance increase. The confined, anti-punchthrough region is obtained via ion implantation procedures into a channel region, using polysilicon sidewalls for purposes of placing the implanted region only into desired regions below the channel region.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)