MULTIPLE LOGICAL INTERFACES TO A SHARED COPROCESSOR RESOURCE

ABSTRACT OF THE DISCLOSURE

An embedded processor complex contains multiple protocol processor units (PPUs) (10). Each unit (10) includes at least one, and preferably two independently functioning core language processors (Cps) (34, 36). Each CLP (34, 36) supports dual threads which interact through logical coprocessor execution or data interfaces with a plurality of special purpose coprocessors that serve each PPU (10). Operating instructions enable the PPU (10) to identify long and short latency events and to control and shift priority for thread execution based on this identification. The instructions also enable the conditional execution of specific coprocessor operations upon the occurrence or non-occurrence of certain specified events.

FIG. 1