What is Claimed is:

1. A storage device comprising:

a nonvolatile memory device; and

a storage controller configured to access the nonvolatile memory device based on a request of an external host device,

wherein the storage controller sends a signal to the external host device, depending on a used amount of a throughput in accessing the nonvolatile memory device being within a specific range.

2. The storage device of claim 1, wherein the signal includes a local processor request based on a non-uniform memory access (NUMA).

3. The storage device of claim 1, wherein the signal includes information of the throughput.

4. The storage device of any one of claims 1 to 3, wherein the signal includes a message signaled interrupt (MSI) format defined in a peripheral component interconnect express (PCIe) standard.

5. The storage device of claim 1, wherein the storage controller periodically sends a second signal including information of the throughput to the external host device.

6. The storage device of claim 1, wherein the storage controller sends a second signal including information of the throughput to the external host device, based on a change in a range to which a value of the throughput belongs.

7. The storage device of claim 1, wherein the storage controller sends a second signal to the external host device based on a value of the throughput being less than a threshold value, and

wherein the threshold value is less than a lower value of the specific range.

8. The storage device of any one of claims 1 to 7, wherein the specific range corresponds to a range from 60% to 70% of a maximum value of the throughput.

9. An operating method comprising:

accessing, at a storage controller, a nonvolatile memory device based on a request of an external host device;

monitoring, at the storage controller, a throughput in accessing the nonvolatile memory device; and

sending, from the storage controller, a signal to the external host device depending on a used amount of the throughput being within a specific range.

10. The method of claim 9, further comprising:

sending, from the storage controller to the external host device, a second signal including information of the throughput.

11. The method of claim 9, further comprising:

sending, from the storage controller to the external host device, a second signal including information of the throughput based on a change in a range to which a value of the throughput belongs.

12. The method of claim 9, further comprising:

sending, from the storage controller to the external host device, the signal based on a value of the throughput being less than a threshold value.

13. An electronic device comprising:

a first processor group including a plurality of first processors;

a second processor group including a plurality of second processors, the second processor group being configured to communicate with the first processor group; and

a storage device connected with the second processor group,

wherein the plurality of second processors directly access the storage device,

wherein the plurality of first processors access the storage device through the plurality of second processors, and

wherein, depending on a used amount of a throughput of the storage device being within a specific range, the storage device sends a signal to a processor that accesses the storage device from among the plurality of first processors and the plurality of second processors.

14. The electronic device of claim 13, wherein, when an input and output (IO) requirement for the storage device necessary for a new process is less than a threshold value, the new process is executed by an idle processor that is in an idle state from among the plurality of first processors.

15. The electronic device of claim 13, wherein, when an input and output (IO) requirement for the storage device necessary for a new process is greater than a threshold value, the new process is executed by an idle processor that is in an idle state from among the plurality of second processors.

16. The electronic device of claim 15, wherein, when there is no idle processor that is in the idle state from among the plurality of second processors, the new process is executed by an idle processor that is in the idle state from among the plurality of first processors.

17. The electronic device of claim 13, wherein, when a process executed by at least one first processor of the plurality of first processors accesses the storage device, based on the signal the process is switched to be executed by at least one second processor that is in an idle state from among the plurality of second processors.

18. The electronic device of claim 13, wherein, when a process executed by at least one second processor of the plurality of second processors accesses the storage device, the signal is ignored.

19. The electronic device of any one of claims 13 to 18, wherein the signal includes a message signaled interrupt (MSI) format defined in a peripheral component interconnect express (PCIe) standard.

20. The electronic device of any one of claims 13 to 19, wherein the plurality of first processors are implemented with multiple cores of a central processing unit, and the plurality of second processors are implemented with multiple cores of a central processing unit.