

FAST SYMBOL SYNCHRONIZER

ABSTRACT

[00116] The present embodiment proposes a system for fast symbol synchronization capable of rapidly performing “phase lock” to decode system critical information in the header sequence but also continue to “track out” the residual timing error during payload. The system 10 comprises a timing estimator 30 and a timing recovery module 20, both adapted for receiving an input data stream 5 comprising of a plurality of received symbols. The timing estimator 30 receives the data stream and implements a feedforward algorithm for estimating an estimated timing error 35 from the input data stream 5. The system 10 further comprises of a formatter 50 which is adapted for producing an initialization value *nco_initial* 55 from the estimated timing error 35 from the timing estimator 30. The initialization value *nco_initial* 55 is then fed back into the timing recovery module 20. The timing recovery module 20 implementing a feedback based algorithm utilizes the initialization value *nco_initial* 55 together with the data stream 5 to produce an output data stream 27 comprising of a plurality of timing recovered symbols. The timing recovered symbols are then sent to subsequent stages in the communication system for demodulation and data recovery. In the present embodiment, the timing estimator 30, the timing recovery module 20 and the formatter 50 all operate on a T/2 architecture.

[00117] FIG.1 accompanies the abstract.