CLAIMS

1. Process for treating a structure of semiconductor-on-insulator type successively comprising a support substrate (1), a dielectric layer (2) and a semiconductor layer (3) having a thickness of less than or equal to 100 nm, said semiconductor layer (3) being covered with a sacrificial oxide layer (4), **characterized** in that it comprises:

- measuring, at a plurality of points distributed over the surface of the structure, the thickness of the sacrificial oxide layer (4) and of the semiconductor layer (3), so as to produce a mapping of the thickness of the semiconductor layer (3) and to determine, from said measurements, the average thickness of the semiconductor layer (3),
- selective etching of the sacrificial oxide layer (4) so as to expose the semiconductor layer (3), and
- carrying out a chemical etching of the semiconductor layer (3), the application, temperature and/or duration conditions of which are adjusted as a function of said mapping and/or of the mean thickness of the semiconductor layer (3), so as to thin, at least locally, said semiconductor layer (3) by a thickness identified as being an overthickness at the end of the measurement step.

2. Process according to Claim 1, applied to a batch of semiconductor-on-insulator structures, characterized in that at the end of the thickness measurement, the structures are sorted by mean thickness class of the semiconductor layer (3), and a chemical etching is carried out under identical conditions for all the structures belonging to one and the same class.

3. Process according to Claim 2, characterized in that said chemical etching is carried out by simultaneously immersing all the structures of one and the same class in a bath of a chemical etching solution.

4. Process according to either of Claims 2 and 3, characterized in that from 3 to 6 mean thickness classes are defined beforehand.

5. Process according to one of Claims 2 to 4, characterized in that said mean thickness classes have a width of from 0.3 to 0.5 nm.

6. Process according to Claim 1, characterized in that, starting from the mapping of the thickness of the semiconductor layer (3), at least one region is determined that has an overthickness to be thinned in order to standardize the thickness of the semiconductor layer (3) within said structure.

7. Process according to Claim 6, characterized in that during the chemical etching of the semiconductor layer (3) said at least one region to be thinned of the layer (3) is heated locally so as to provide a greater thinning in said region.

8. Process according to either of Claims 6 and 7, characterized in that the chemical etching solution is distributed selectively by a jet over the surface of the semiconductor layer (3), so as to deposit a greater amount of solution on said at least one region to be thinned.

9. Process according to one of Claims 6 to 8, characterized in that during the chemical etching of the semiconductor layer (3) the etching solution is applied to said region to be thinned for a duration greater than the duration of application to the rest of the layer (3).

10. Process according to Claim 1, implemented in a process for the batch manufacture of semiconductor-on-insulator type structures with a view to standardizing the mean thickness of the semiconductor layer (3) of the structures constituting said batch relative to that of another batch manufactured by the same process, characterized in that at the end of the thickness measurement, the mean thickness of the semiconductor layer (3) for the batch is calculated, a mean thickness class is allocated to said batch, and a chemical etching of the semiconductor layer (3) is carried out for the whole of said batch, the application, temperature and/or duration conditions of which chemical etching are adjusted as a function of said mean thickness class.

11. Process according to one of Claims 1 to 10, characterized in that said chemical etching of the semiconductor layer (3) is of SC1 type.

12. Process according to one of Claims 1 to 11, characterized in that the selective etching of the sacrificial oxide layer (4) is carried out by hydrofluoric acid.

13. Process according to one of Claims 1 to 12, characterized in that the thickness measurement is carried out by ellipsometry.

14. Process for manufacturing a structure of semiconductor-on-insulator type successively comprising a support substrate (1), a dielectric layer (2) and a semiconductor layer (3) having a thickness of less than or equal to 100 nm, comprising the steps of:

- providing a substrate, referred to as a donor substrate, comprising said semiconductor layer (3),
- forming at least one dielectric layer on the semiconductor layer and/or on the support substrate (1),
- adhesive bonding of the support substrate (1) to the semiconductor layer (3) of the donor substrate, said at least one dielectric layer being at the bonding interface, so as to form the dielectric layer (2) of the semiconductor-on-insulator structure,
- transferring the semiconductor layer (3) to the support substrate (1),
- smoothing of the semiconductor layer (3),
- forming a sacrificial oxide layer (4) on the semiconductor layer (3),

said process being characterized in that a treatment according to one of Claims 1 to 13 is carried out on the structure thus formed.

CLAIMS

The invention claimed is:

1. A method of treating a semiconductor-on-insulator (SeOI) structure successively comprising a support substrate, a dielectric layer and a semiconductor layer having a thickness of less than or equal to 100 nm, the semiconductor layer being covered with a sacrificial oxide layer, the method comprising: measuring, at a plurality of points distributed over a surface of the SeOI structure, a thickness of the sacrificial oxide layer and a thickness of the semiconductor layer and producing a map of the thickness of the semiconductor layer and determining an average thickness of the semiconductor layer from the measurements, selectively etching the sacrificial oxide layer and exposing the semiconductor layer, and chemically etching the semiconductor layer, and adjusting at least one of an application of an etchant of the etching process, a temperature of the etching process, and a duration of the etching process as a function of the mapping and/or of the mean thickness of the semiconductor layer and thinning, at least locally, the semiconductor layer by a thickness identified as being an overthickness at the end of the measuring process.

2. The method of claim 1, further comprising applying the method of claim 1 to a batch of SeOI structures, further comprising, at the end of the measuring process, sorting the SeOI structures by the mean thicknesses of the semiconductor layers into classes, and wherein the chemical etching is carried out under identical conditions for all the SeOI structures belonging to the same class.

3. The method of claim 2, wherein the chemical etching comprises simultaneously immersing all the SeOI structures of the same class in a bath of a chemical etching solution.

4. The method of claim 3, wherein the classes include 3 to 6 individual classes defined prior to the sorting of the SeOI structures.

5. The method of claim 4, wherein the classes have a width of from 0.3 nm to 0.5 nm.

6. The method of claim 1, wherein the measuring comprises identifying at least one region of the semiconductor layer having an overthickness, and wherein the chemical etching comprises selectively thinning the at least one region relative to another region of the semiconductor layer.

7. The method of claim 6, wherein selectively thinning the at least one region comprises locally heating the at least one region during the chemical etching of the semiconductor layer.

8. The method of claim 6, wherein selectively thinning the at least one region comprises selectively distributing a chemical etching solution over a surface of the semiconductor layer and depositing a greater amount of the chemical etching solution on the at least one region relative to the another region of the semiconductor layer.

9. The method of claim 8, wherein selectively distributing the chemical etching solution over the surface of the semiconductor layer comprises applying the chemical etching solution to the at least one region for a duration of time greater than a duration of time to which the chemical etching solution is applied to the another region of the semiconductor layer.

10. The method of claim 1, further comprising successively applying the method of claim 1 to batches of SeOI structures, calculating a mean thickness of the semiconductor layers in one of the batches, allocating a mean thickness class to the one of the batches, and carrying out the chemical etching of the semiconductor layers of the SeOI structures in the one of the batches and adjusting at least one of an application of an etchant of the etching process, a temperature of the etching process, and a duration of the etching process as a function of the mean thickness class allocated to the one of the batches.

11. The method of claim 1, wherein the chemical etching of the semiconductor layer is of Standard Cleaning 1 (SC1) type.

12. The method of claim 1, wherein selectively etching the sacrificial oxide layer comprises etching the sacrificial oxide layer with hydrofluoric acid.

13. The method of claim 1, wherein the measurement of the thickness of the sacrificial oxide layer and the thickness of the semiconductor layer comprises using ellipsometry to measure the thickness of the sacrificial oxide layer and the thickness of the semiconductor layer.

14. A method of manufacturing a semiconductor-on-insulator (SeOI) structure, comprising:

a support substrate, a dielectric layer and a semiconductor layer, having a thickness of less than or equal to 100 nm, the method comprising:

providing a donor substrate, comprising the semiconductor layer, forming at least one dielectric layer on at least one of the semiconductor layer and the support substrate, bonding the support substrate to the semiconductor layer of the donor substrate, at least one dielectric layer being at the bonding interface, and forming the dielectric layer of the SeOI structure, transferring the semiconductor layer to the support substrate, smoothing the semiconductor layer, forming a sacrificial oxide layer on the semiconductor layer; and the method being characterized in that a treatment according to one of claims 1 to 13 is carried out on the structure thus formed.

15. A method of treating a semiconductor-on-insulator (SeOI) structure successively comprising a support substrate, a dielectric layer and a semiconductor layer having a thickness of less than or equal to 100 nm, the semiconductor layer being covered with a sacrificial oxide layer, the method comprising;

measuring, at a plurality of points distributed over a surface of the SeOI structure, a thickness of the sacrificial oxide layer and a thickness of the semiconductor layer, producing a map of the thickness of the semiconductor layer, and determining an average thickness of the semiconductor layer from the measurements;

selectively etching the sacrificial oxide layer and exposing the semiconductor layer; and chemically etching the semiconductor layer and adjusting at least one of an application of an etchant of the etching process, a temperature of the etching process, and a duration of the etching process as a function of the mapping and/or of the mean thickness of the semiconductor layer and thinning, at least locally, the semiconductor

layer by a selected thickness.

16. The method of claim 15, further comprising applying the method of claim 15 to a batch of SeOI structures, and sorting the SeOI structures by the mean thicknesses of the semiconductor layers into classes, and wherein the chemical etching is carried out under identical conditions for all the SeOI structures belonging to the same class.

17. The method of claim 16, wherein the chemical etching comprises simultaneously immersing all the SeOI structures of the same class in a bath of a chemical etching solution.

18. The method of claim 17, wherein the classes include 3 to 6 individual classes defined prior to the sorting of the SeOI structures.

19. The method of claim 18, wherein the classes have a width of from 0.3 nm to 0.5 nm.

20. The method of claim 15, wherein the measuring comprises identifying at least one region of the semiconductor layer having an overthickness, and wherein the chemical etching comprises selectively thinning the at least one region relative to another region of the semiconductor layer.

21. The method of claim 20, wherein selectively thinning the at least one region comprises locally heating the at least one region during the chemical etching of the semiconductor layer.

22. The method of claim 20, wherein selectively thinning the at least one region comprises selectively, distributing a chemical etching solution over a surface of the semiconductor layer and depositing a greater amount of the chemical etching solution on the at least one region relative to the another region of the semiconductor layer.

23. The method of claim 22, wherein selectively distributing the chemical etching solution over the surface of the semiconductor layer comprises applying the chemical etching solution to the at least one region for a duration of time greater than a duration of time to which the chemical etching solution is applied to the another region of the

semiconductor layer.

24. The method of claim 15, further comprising successively applying the method of claim 1 to batches of SeOI structures, calculating a mean thickness of the semiconductor layers in one of the batches, allocating a mean thickness class to the one of the batches, and carrying out the chemical etching of the semiconductor layers of the SeOI structures in the one of the batches and adjusting at least one of an application of an etchant of the etching process, a temperature of the etching process, and a duration of the etching process as a function of the mean thickness class allocated to the one of the batches.

25. The method of claim 15, wherein the chemical etching of the semiconductor layer is of SC1 type.

26. The method of claim 15, wherein selectively etching the sacrificial oxide layer comprises etching the sacrificial oxide layer with hydrofluoric acid.

27. The method of claim 15, wherein measuring the thickness of the sacrificial oxide layer and the thickness of the semiconductor layer comprises using ellipsometry to measure the thickness of the sacrificial oxide layer and the thickness of the semiconductor layer.

28. A method of manufacturing a semiconductor-on-insulator (SeOI) structure, successively comprising a support substrate, a dielectric layer and a semiconductor layer, having a thickness of less than or equal to 100 nm, the method comprising: providing a donor substrate comprising the semiconductor layer; forming at least one dielectric layer on at least one of the semiconductor layer and the support substrate; bonding the support substrate to the semiconductor layer of the donor substrate, the at least one dielectric layer disposed at the bonding interface and forming the dielectric layer of the SeOI structure; transferring the semiconductor layer to the support substrate; smoothing a surface of the semiconductor layer; forming a sacrificial oxide layer on the surface of the semiconductor layer; measuring, at a plurality of points distributed over a surface of the sacrificial oxide layer, a thickness of the sacrificial oxide layer and a thickness of the semiconductor layer, and producing a map of the

thickness of the semiconductor layer and determining an average thickness of the semiconductor layer from the measurements; selectively etching the sacrificial oxide layer and exposing the semiconductor layer; and chemically etching the semiconductor layer and adjusting at least one of an application of an etchant of the etching process, a temperature of the etching process, and a duration of the etching process as a function of the mapping and/or of the mean thickness of the semiconductor layer and thinning, at least locally, the semiconductor layer by a selected thickness.