WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array comprising a first memory region and a second memory region;

signal lines configured to receive a command and an address from a source located outside the memory device;

a mode selector circuit configured to generate a processing mode selection signal for controlling the memory device to enter an internal processing mode based on the address received together with the command;

a command converter circuit configured to convert the received command into an internal processing operation command in response to activation of the processing mode selection signal; and

an internal processor configured to perform an internal processing operation on the first memory region in response to the internal processing operation command, in the internal processing mode,

wherein the mode selector circuit generates the processing mode selection signal in response to a specific address, which is included in the address received with the command and distinguishes the first memory region and the second memory region from each other.

2. The memory device of claim 1, wherein the signal lines are connected to a memory physical layer interface, which supports a double data rate (DDR) protocol or a low power double data rate (LPDDR) protocol and the memory physical layer interface is located outside the memory device.

~~3. The memory device of claim 1 or claim 2, wherein the mode selector circuit generates the processing mode selection signal in response to a specific address, which is included in the address received with the command and distinguishes the first memory region and the second memory region from each other.~~

~~4~~3. The memory device of claim ~~3~~1 or claim 2, wherein

the memory cell array comprises stacked memory layers,

the stacked memory layers include common channels, through silicon vias and electrode pads electrically connected to the through silicon vias, and, in the common channels, the stacked memory layers belonging to the first memory region and the stacked memory layers belonging to the second memory region are selectively accessed according to a stack identification signal, and

the specific address comprises the stack identification signal for accessing the stacked memory layers belonging to the first memory region.

~~5~~4. The memory device of claim ~~3~~1 or claim 2, wherein

the memory cell array comprises stacked memory layers,

the stacked memory layers include common channels, through silicon vias and electrode pads electrically connected to the through silicon vias, and, in the common channels, the stacked memory layers belonging to the first memory region and the stacked memory layers belonging to the second memory region are selectively accessed according to a channel address, and

the specific address comprises the channel address for accessing the stacked memory layers belonging to the first memory region.

~~6~~5. The memory device of any one of claims ~~3~~ 1 to ~~5~~4, wherein

the memory cell array comprises a plurality of banks,

from among the banks, banks belonging to the first memory region and banks belonging to the second memory region are selectively accessed according to a bank address, and

the specific address comprises the bank address for accessing the banks belonging to the first memory region.

~~7~~6. The memory device of any one of claims ~~3~~ 1 to ~~6~~5, wherein the first memory region and the second memory region are set to fixed regions by the specific address.

~~8~~7. The memory device of any one of claims ~~3~~ 1 to ~~6~~5, wherein the first memory region and the second memory region are set to variable regions by the specific

address.

~~9~~8. The memory device of any one of claims ~~3~~ 1 to ~~8~~7, wherein, when the specific address is not included in the address received with the command, the mode selector circuit~~s~~ deactivates the processing mode selection signal, such that the memory device enters a normal mode.

~~10. The memory device of any one of claims 1 to 9, wherein~~

~~the memory device sequentially receives first commands through the signal lines and sequentially receives addresses respectively corresponding to the sequentially received first commands, and~~

~~the mode selector circuit determines whether the sequentially received addresses coincide with an internal processing mode entering code and an internal processing mode exiting code and generates the processing mode selection signal based on a result of the determination.~~

~~11. The memory device of claim 10, wherein the mode selector circuit activates the processing mode selection signal when the sequentially received addresses coincide with the internal processing mode entering code and the sequentially received addresses do not coincide with the internal processing mode exiting code.~~

~~12. The memory device of claim 10 or claim 11, wherein the mode selector circuit deactivates the processing mode selection signal, such that the memory device enters a normal mode, when the sequentially received addresses do not coincide with the internal processing mode entering code or the sequentially received addresses coincide with the internal processing mode exiting code.~~

~~13~~9. A method of operating a memory device comprising a memory cell array comprising a first memory region and a second memory region, and internal processor configured to perform an internal processing operation, the method comprising:

receiving a command and an address from a source located outside the memory device through a pre-defined protocol interface;

generating a processing mode selection signal for controlling the memory device to enter an internal processing mode based on the address received together with the command;

converting the received command into an internal processing operation command in response to activation of the processing mode selection signal; and

performing, by the internal processor, ~~an~~ the internal processing operation on the first memory region in response to the internal processing operation command, in the internal processing mode,

wherein the method further comprises: determining whether the address received with the command comprises a specific address that distinguishes the first memory region and the second memory region from each other; and activating the processing mode selection signal when the specific address is included in the address received with the command.

~~14~~10. The method of claim ~~13~~9, wherein

the pre-defined protocol interface is a memory physical layer interface, which supports a double data rate (DDR) protocol or a low power double data rate (LPDDR) protocol.

~~15~~11. The method of claim ~~13~~ 9 or claim ~~14~~10, wherein the generating of the processing mode selection signal comprises:

~~determining whether the address received with the command comprises a specific address that distinguishes the first memory region and the second memory region from each other;~~

~~activating the processing mode selection signal when the specific address is included in the address received with the command; and~~

deactivating the processing mode selection signal when the specific address is not included in the address received with the command.

~~16~~12. The method of claim ~~15~~11, further comprising entering a normal mode in response to deactivation of the processing mode selection signal.

~~17~~13. The method of ~~claim 15 or claim 16~~any one of claims 9 to 12, wherein the specific address comprises a stack identification signal for addressing the first memory region, a channel address, or a bank address.

~~18~~14. The method of any one of claims ~~15~~ 9 to ~~17~~13, wherein the first memory region and the second memory region are set to fixed regions by the specific address.

~~19~~15. A memory system comprising:

a memory device; and

a memory controller configured to control the memory device by using a pre-defined protocol interface connected to the memory device,

wherein the memory device comprises:

a memory cell array comprising a first memory region and a second memory region;

a~~n~~ mode selector circuit configured to receive a command and an address from the memory controller through the pre-defined protocol interface and, based on the address received together with the command, generate a processing mode selection signal for controlling the memory device to enter an internal processing mode;

a command converter circuit configured to convert the received command into an internal processing operation command in response to activation of the processing mode selection signal; and

an internal processor configured to perform an internal processing operation on the first memory region in response to the internal processing operation command, in the internal processing mode, and

wherein the mode selector circuit generates the processing mode selection signal in response to a specific address, which is included in the address received with the command and distinguishes the first memory region and the second memory region from each other.

~~20~~16. The memory system of claim ~~19~~15, wherein the pre-defined protocol interface is a memory physical layer interface, which supports a double data rate (DDR) protocol or a low power double data rate (LPDDR) protocol.