

Apparatus And Method For A Memory Storage Cell Leakage Cancellation Scheme

FIELD OF INVENTION

5 [0001] The field of invention relates to semiconductor memory technology generally; and more specifically, to an apparatus and method for a memory storage cell leakage cancellation scheme.

Background

10 [0002] Figure 1 shows a prior art Random Access Memory (RAM) cell 100. The prior art RAM cell 100 of Figure 1 includes a plurality of "N" storage cells S_1 through S_N (each of which may correspond to static RAM (SRAM) cells). Each of the storage cells S_1 through S_N stores a bit of data. Data is read from a particular storage cell by activating its corresponding word line (WL) (e.g., WL_1 for storage cell S_1 , WL_2 for S_2 , etc.). During a typical storage cell read operation, the bit lines 101, 102 are pre-charged to a "high" voltage.

[0003] The word line of the storage cell to be read (e.g., word line WL_1 for storage cell S_1) is activated (e.g., with a "high" voltage) while the word lines for the remaining "un read" storage cells (e.g., word lines WL_2 through WL_N for storage cells S_2 through S_N , respectively) are deactivated (e.g., with a "low" voltage).
20 Upon the activation of the word line for the storage cell to be read (e.g., word line WL_1 for storage cell S_1), the storage cell to be read drives one of the bit lines to a "low" voltage.

[0004] For example, if the data stored in storage cell S_1 corresponds to a "1",
25 storage cell S_1 drives bit line 102 to a "low" voltage while bit line 101 remains at

the pre-charged "high" voltage. By contrast, if the data stored in storage cell S_1 corresponds to a "0", storage cell S_1 drives bit line 101 to a "low" voltage while bit line 102 remains at the pre-charged "high" voltage. Figure 1 shows an example of the later case (i.e., storage cell S_1 has a "0" stored) because drive current I_{sc} is observed being driven from bit line 101 by storage cell S_1 .

[0005] Because the voltages on the bit lines 101, 102 during a storage cell read are different (i.e., one voltage being high, the other voltage being low), a differential signal may be said to exist on the bit lines 101, 102. The differential signal provided on the bit lines 101, 102 may be expressed as:

10 $Signal = V1 - V2$ Eqn.1

where $V1$ is the voltage on bit line 101 and $V2$ is the voltage on bit line 102. Note that the actual high and low voltages on the bit lines may vary from embodiment to embodiment. Furthermore, note that the greater the difference between $V1$ and $V2$, the greater the differential signal observed on the bit lines 101, 102.

15 **[0006]** Storage cell leakage may cause an increase in the amount of time it takes the differential voltage to develop on the bit lines 101, 102 during a bit cell read. As such, the speed of operation of the RAM cell 100 may be adversely affected by the storage cell leakage. The rate at which the differential voltage is created during the course of a storage cell read, without storage cell leakage, may be expressed as:

20 $Dv/Dt = I_{sc}/(C_b + 2C_c)$ Eqn. 2

where: 1) C_b is the capacitance of the bit line being pulled down; 2) C_c is the capacitance between the bit lines 101, 102; and 3) I_{sc} is the amount of drive current pulled by a storage cell being read from.

[0007] From Equation 2, it is apparent that the rate at which the differential voltage is created increases as I_{sc} increases. Storage cell leakage has the effect of the reducing the I_{sc} term in Equation 2 and, as such, reduces the rate at which the differential voltage is created. Storage cell leakage is the tendency of a storage cell, that is not being read from, to pull current from a bit line. As the number of “un-read” cells that pull leakage current from the “high” bit line increases, the impact on the rate at which the differential voltage worsens.

[0008] A worse case condition is exemplified in Figure 1. Specifically, during a read of storage cell S_1 which pulls current I_{sc} from the low bit line 101, each of the remaining $N-1$ storage cells (i.e., storage cells S_2 through S_N) pull leakage current I_L from the high bit line 102. Each leakage current I_L from the high bit line 102 will cause a drop in the high bit line 102 voltage. As such, $N-1$ leakage currents I_L from the high bit line 102 (as seen in Figure 1) corresponds to a worst case voltage drop on the high bit line 102.

[0009] From the perspective of the differential voltage being established between the pair of bit lines 101 and 102, as the high bit line 102 voltage drops from the $N-1$ leakage currents I_L , the effect of dropping the low bit line 101 voltage with the drive current I_{sc} is reduced. This corresponds to a decrease in the differential signal voltage which corresponds to a decrease in the rate at which the differential signal voltage is developed.

[0010] That is, for the worst case condition shown in Figure 1, the rate at which the differential voltage is created during the course of a storage cell read, with storage cell leakage, may be expressed as:

$$Dv/Dt = (I_{sc} - (N-1)I_L) / (C_b + 2C_c) \quad \text{Eqn. 3}$$

where: 1) C_b is the capacitance of the bit line being pulled down; 2) C_c is the capacitance between the bit lines 101, 102; 3) I_{sc} is the amount of drive current pulled by a storage cell being read from; and 4) $(N-1)I_L$ is the total amount of leakage current being pulled from the high bit line 102. As seen in Equation 3, the leakage current term $(N-1)I_L$ subtracts from the drive current term I_{sc} . This corresponds to a drop in the rate at which the differential voltage is developed. As discussed, this corresponds to a drop in the speed of the RAM cell 100.

BRIEF DESCRIPTION OF DRAWINGS

10 **[0011]** The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings in which like references indicate similar elements and in which:

[0012] Figure 1 shows a prior art RAM cell.

[0013] Figure 2 shows an embodiment of an improved RAM cell.

15 **[0014]** Figure 3 shows an embodiment of control line signaling that may be used to read data from a storage cell within the improved RAM cell of Figure 2.

[0015] Figure 4 shows another embodiment of an improved RAM cell.

DETAILED DESCRIPTION

[0016] Providing cancellation current on the bit lines effectively nullifies the reduced differential signal quality described above in the background. Figure 2 shows an embodiment 200 of an improved RAM cell that effectively cancels the leakage current. Figure 3 shows an embodiment of control signaling that may be used to read the from a storage cell within the improved RAM cell 200 of Figure 2.

[0017] Referring to Figures 2 and 3, the read operation of a storage cell may be viewed as occurring in phases. A first phase (e.g., between times T_0 and T_1 of

Figure 3) equalizes and precharges the bit lines 201, 202. A second phase (e.g., between times T1 and T2 of Figure 3) approximately cancels the effect of any leakage current that may exist on the bit lines 201, 202 by providing a leakage supply current I_{L1} , I_{L2} on each bit line 201, 202 individually. A third phase (e.g., between times T2 and T3) maintains the leakage supply currents I_{L1} , I_{L2} while the bit lines 201, 202 are equalized again. A fourth phase (e.g., between times T3 and T4) reads data from a storage cell.

[0018] A first phase (e.g., between times T0 and T1 in Figure 3) equalizes and precharges the bit lines 201, 202. The bit lines 201, 202 are equalized by turning transistor Q5 on. Transistor Q5 is turned on by driving the equalize line 203, 303 low. Turning transistor Q5 on effectively creates a short circuit between the bit lines 201, 202 which causes the bit lines 201, 202 to have an approximately equal voltage. This activity may be referred to as equalizing the bit lines 201, 202.

[0019] Equalizing the bit lines 201, 202 helps to effectively "clear" the RAM cell 200 of a prior storage cell reading. For example if a storage cell was read from prior to time T0 in Figure 3, the bit lines 201, 202 may still maintain the differential voltage from the reading. That is, one bit line may be at a low voltage while another bit line may be at a high voltage. Driving the equalize line 203 low allows the bit lines 201, 202 to reach a common voltage.

[0020] The bit lines 201, 202 are also pre-charged when the sense line 204, 304 is driven low. In the embodiment of Figure 2, pre-charging the bit lines 201, 202 corresponds to bringing both the bit lines 201, 202 to a high voltage. During a subsequent read from a storage cell (e.g., between times T3 and T4 of Figure 4), the storage cell being read from pulls one of the pre-charged bit lines to a low voltage.

[0021] In the embodiment of Figure 2, the bit lines 201, 202 are pre-charged by turning transistors Q1 and Q2 on. Transistor's Q1 and Q2 are turned on in the embodiment of Figure 2 by driving the sense line low 204, 304. Note that, in the particular embodiment of Figure 2, the gate and drains of each of transistors Q1 and Q2 may be "shorted" by a transistor. That is, transistor Q3 shorts the drain and gate of transistor Q1 and transistor Q4 shorts the drain and gate of transistor Q2. Shorting the gate and drain of each of transistors Q1 and Q2 configures these transistors Q1, Q2 as an active load.

[0022] That is, driving the sense line 204, 304 low turns on transistors Q3 and Q4 which, in turn, respectively enables transistors Q1 and Q2 as active loads. The source to drain voltage V_{SD} of an active load may be approximated as:

$$V_{SD} = V_{SG} = V_T + (I_{SD}/B)^{0.5} \quad \text{Eqn. 4}$$

where: 1) V_{SG} is the source to gate voltage; 2) V_T is the threshold voltage; 3) I_{SD} is the source to drain current; and 3) B is the transconductance. For small source to drain currents I_{SD} , note that the source to drain voltage V_{SD} approaches V_T . As such, in the embodiment of Figure 2, the pre-charge voltage on the bit lines 201, 202 may typically correspond to a voltage near $V_{CC}-V_T$. Figure 3 shows an exemplary pre-charged bit line level 310 for the voltage 301 on bit line 201 of Figure 2.

[0023] In an alternate embodiment (in order to speed the rate at which the bit lines are pre-charged), the gate voltages of Q1 and Q2 may be forcibly driven low while transistors Q3 and Q4 are kept off during the first phase between times T_0 and T_1 . For example, between times T_0 and T_1 , the sense voltage may be placed at a high voltage (which turns off transistors Q3 and Q4) and the gate voltages of transistors Q1 and Q2 may be grounded.

[0024] This places transistors Q1 and Q2 in a "high current" output state which allows them to drive the capacitance associated with bit lines 201, 201. This allows the bit line 201, 202 voltages to approach their pre-charge voltage faster than a pure active load. As such, referring to Figure 3, the sense line 204 voltage
5 304 may be, in one embodiment: 1) at a high logic level between times T0 and T1; and 2) switched to a low logic level at time T1.

[0025] The equalization between times T0 and T1 may also be eliminated because the establishment of equal pre-charge voltages on the bit lines 201, 202 is not necessary between times T0 and T1. That is, the act of pre-charging the bit
10 lines 201, 202 effectively clears them of their most recent storage cell read information. In another alternate embodiment, transistors Q3 and Q4 may be replaced with transmission gates to protect against low bit line 201, 202 voltages. A transmission gate is a parallel coupling of an NMOS transistor and a PMOS transistor such that when one is "on", both are "on" and when one is "off" both are
15 "off".

[0026] During a second phase (e.g., between times T1 and T2 in Figure 3) the effect of any leakage current that may exist on the bit lines 201, 202 is approximately canceled by providing a leakage supply current I_{L1} , I_{L2} on each bit
line 201, 202 individually. This is accomplished by deactivating the equalization
20 between the bit lines 201, 202. In the embodiment of Figure 2, deactivating the equalization between the bit lines 201, 202 is accomplished by turning off transistor Q5 which, in turn, is accomplished by driving the equalization line 203, 303 high.

[0027] With the equalization deactivated, the bit lines 201, 202 are isolated from
25 one another. As such, transistors Q1 and Q2 individually supply the leakage

current that may exist on their respective bit lines 201, 202. That is, transistor Q1 provides a current I_{L1} which supplies any leakage currents that flow from bit line 201 (such as leakage current I_{La}). Transistor Q2 provides a current I_{L2} which supplies any leakage currents that flow from bit line 202 (such as leakage current I_{Lb}).

[0028] If X storage cells in the RAM cell 200 leak from bit line 201 and Y storage cells in the RAM cell 200 leak from bit line 202, then (assuming for simplicity each leakage into a storage cell corresponds to the same amount of leakage current I_L) $I_{L1} = XI_L$ and $I_{L2} = YI_L$. As discussed in more detail below, individually supplying the leakage currents on each bit line 201, 202, approximately cancels their effect on the differential signal established between the bit lines 201, 202 during a read operation of a storage cell.

[0029] Note that, in light of Equation 4, the source to gate voltages of transistors Q1 and Q2 may differ if I_{L1} does not equal I_{L2} . Given that the gate to source voltages of transistors Q1 and Q2 may differ if I_{L1} does not equal I_{L2} , note that (again in light of Equation 4) the voltage on the bit lines 201, 202 may differ as a consequence. That is, as an active load is configured to have $V_{SG} = V_{SD}$, a difference in source to gate voltage corresponds to a difference in source to drain voltage. This will result in different voltages as between the pair of bit lines 201, 202.

[0030] During a third phase (e.g., between times T2 and T3 of Figure 3) the bit lines 201, 202 are equalized while the leakage supply currents I_{L1} , I_{L2} are maintained. The equalization to the RAM cell 200 (which is accomplished in the embodiments of Figures 2 and 3 by dropping the voltage on the equalize line 203, 303 to a low voltage) "fixes" the difference in voltage, as between the pair of bit

lines 201, 202, that may develop as a result of separately supplying their corresponding leakage currents (as just described above).

[0031] As such, should a difference in voltage develop on the bit lines 201, 202, the equalization will force the bit line 201, 202 voltages to be approximately equal.

5 The leakage supply currents I_{L1} , I_{L2} are also maintained by turning transistors Q3 and Q4 off (which is accomplished in the embodiments of Figures 2 and 3 by raising the sense line 204, 304 to a high voltage). Turning off transistors Q3 and Q4 removes the short circuit that exists between gate and source of transistors Q1 and Q2.

10 **[0032]** However, due to the presence of capacitors C1 and C2, the leakage supply currents I_{L1} , I_{L2} (that respectively run through transistors Q1 and Q2) remain substantially unchanged. As such, the leakage supply currents may be said to be "maintained". Recall that a difference in bit line 201, 202 voltage may develop as a result of separately supplying the leakage currents for each bit line (between
15 times T1 and T2 as seen in Figure 3). As discussed, the gate voltages for Q1 and Q2 may differ as a consequence.

[0033] During the generation of the leakage supply currents I_{L1} , I_{L2} (between times T1 and T2 as seen in Figure 3) the voltage on capacitors C1, C2 will respectively "ramp up" to the voltage on their respective bit line (because of the short circuit
20 established by transistors Q3 and Q4). That is, capacitor C1 ramps up to the voltage maintained on bit line 201 and capacitor C2 ramps up to the voltage maintained on bit line 202. Again, this is consistent with $V_{SD} = V_{SG}$ for each transistor Q1 and Q2 when transistors Q3 and Q4 are on.

[0034] When transistors Q3 and Q4 are turned off (between times T2 and T3 as
25 seen in Figure 3), both capacitors C1, C2 "hold onto" their voltage. As such, the

leakage supply currents I_{L1} , I_{L2} continue to be generated from transistors Q1 and Q2 respectively. This corresponds to the leakage supply currents I_{L1} , I_{L2} being “maintained” as discussed above. When transistor Q5 is turned on (as seen in Figure 3 between times T2 and T3) bit lines 201, 202 begin to be equalized. After
5 a steady state is reached, the bit lines 201, 202 have approximately equal voltage and the leakage supply currents I_{L1} , I_{L2} continue to be generated from transistors Q1 and Q2 respectively.

[0035] In a fourth phase (e.g., between times T3 and T4 as seen in Figure 3), the data is read from a particular storage cell. As such, in order to read the data from
10 the storage cell, the equalization of the bit lines 201, 202 is terminated so that a differential voltage is allowed to develop across the bit lines. Note, therefore, that Figure 3 indicates the voltage 303 on the equalization line 203 is raised so that transistor Q5 is turned off.

[0036] In the exemplary embodiment of Figure 2, storage cell S_1 is being read
15 from (e.g., by activating 308 its corresponding word line WL_1) and contains digital information corresponding to a “0”. As such, storage cell S_1 pulls drive current I_{sc} from bit line 201 which pulls down the voltage 301 on bit line 201. As each of the leakage currents have been accounted for with the leakage supply currents I_{L1} , I_{L2} that are being provided by transistors Q1 and Q2, the differential voltage across
20 the bit lines develops about as fast as the “full rate” as originally provided by Equation 2.

[0037] Figure 4 shows an alternate embodiment that improves the speed at which the bit lines 401, 402 are pre-charged. The embodiment 400 of Figure 4 adds transistors Q6 and Q7 to the embodiment 200 of Figure 2. Transistors Q6 and Q7
25 further speed up may be used to further speed up the bit line pre-charge activity

that occurs between times T0 and T1 of Figure 3 (and/or between times T2 and T3 of Figure 3). Whenever the equalize line 403 voltage 303 drops to a low voltage, transistors Q6 and Q7 are "on" which effectively drives the capacitance of the bit lines 401, 402 resulting in the rapid increase of the bit line 401, 402 voltages.

[0038] The designs and approaches described above may be utilized within a memory device such as a semiconductor memory chip. The semiconductor chip may then be implemented in a system such as computing system or a networking system. For example, the memory device may be coupled to: 1) a general purpose processor; or 2) a digital signal processor or custom logic circuit (e.g., an Application Specific Integrated Circuit (ASIC); or 3) a bus structure (e.g., a PCI bus). In other applications the designs and approaches discussed above may be used in embedded memory applications. In embedded memory applications, a region of memory is constructed within a larger semiconductor chip (e.g., as an "on board" cache or as memory resources within a system on chip (SoC)).

[0039] Note also that embodiments of the present description may be implemented not only within a semiconductor chip but also within machine readable media. For example, the designs discussed above may be stored upon and/or embedded within machine readable media associated with a design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include: a behavioral level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine

readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

[0040] Thus, it is also to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing
5 core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media;
10 optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

[0041] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident
15 that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An apparatus, comprising:
 - 5 a) a plurality of storage cells coupled between a first bit line and a second bit line;
 - b) a first transistor that pre-charges said first bit line and provides a first supply of current for one or more leakage currents drawn from said first bit line by any of said plurality of storage cells; and
 - 10 c) a second transistor that pre-charges said second bit line and provides a second supply of current for one or more leakage currents drawn from said second bit line by any of said plurality of storage cells.
- 15 2. The apparatus of claim 1 further comprising an equalization line coupled to both said first and second bit lines, wherein a first voltage on said equalization causes said first and second bit lines to approach the same voltage and a second voltage on said equalization line allows said first and second bit lines to maintain different voltages .
- 20 3. The apparatus of claim 2 wherein said equalization line is coupled to both said first and second bit lines by a third transistor, said third transistor having a drain coupled to one of said bit lines, a source coupled to the other of said bit lines, a gate coupled to said equalization line.

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4. The apparatus of claim 3 further comprising a fourth transistor that provides current for said pre-charging of said first bit line, said fourth transistor coupled to said first bit line and said equalization line, said apparatus further comprising a fifth transistor that provides current for said pre-
- 5 charging of said second bit line, said fifth transistor coupled to said second bit line and said equalization line.
5. The apparatus of claim 1 wherein said apparatus corresponds to a Static Random Access Memory (SRAM) cell.
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6. The apparatus of claim 1 further comprising a sense line, said sense line coupled to both said first and second transistors, wherein a first voltage on said sense line causes said pre-charging of said first and second bit lines and a second voltage on said sense line causes said first and second
- 15 supplies of current to be maintained when a said storage cell is being read from.
7. The apparatus of claim 6 wherein said sense line is coupled to said first transistor by a third transistor and is coupled to said second transistor by a
- 20 fourth transistor, said third transistor having a first node coupled to said first bit line and a second node coupled to a gate of said first transistor, said third transistor having a gate coupled to said sense line, said fourth transistor having a first node coupled to said second bit line and a second node coupled to a gate of said second transistor, said fourth transistor
- 25 having a gate coupled to said sense line.

8. The apparatus of claim 1 further comprising a first capacitor that holds a gate voltage for said first transistor so that said first supply current may be maintained during a read of a said storage cell.

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9. The apparatus of claim 8 further comprising a second capacitor that holds a gate voltage for said second transistor so that said second supply current may be maintained during a read of a said storage cell.

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10. A method, comprising:

- a) pre-charging a first bit line with current provided by a first transistor;
- b) pre-charging a second bit line with current provided by a second transistor;
- c) drawing a first leakage supply current from said first transistor to supply one or more leakage currents drawn from said first bit line by one or more storage cells coupled to said first bit line;
- d) drawing a second leakage supply current from said first transistor to supply one or more leakage currents drawn from said first bit line by one or more of said storage cells coupled to said second bit line; and
- e) maintaining said first and second leakage supply currents during a read of a said storage cell.

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11. The method of claim 10 wherein said pre-charging a first bit line and said pre-charging a second bit line occur simultaneously.

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12. The method of claim 10 wherein said drawing a first leakage supply current and said drawing a second leakage current supply current occur simultaneously.

5 13. The method of claim 12 wherein said pre-charging a first bit line and said pre-charging a second bit line occur simultaneously.

14. The method of claim 10 further comprising equalizing said first and second bit lines after said pre-charging of said first and second bit lines, said
10 equalizing occurring prior to said read.

15. The method of claim 10 wherein said maintaining further comprises holding a first gate voltage on said first transistor with a first capacitor and holding a second gate voltage on said second transistor with a second capacitor.

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16. An apparatus, comprising:

a memory coupled to a processor, said memory further comprising:

a) a plurality of storage cells coupled between a first bit line and a second bit line;

20 b) a first transistor that pre-charges said first bit line and provides a first supply of current for one or more leakage currents drawn from said first bit line by any of said plurality of storage cells; and

c) a second transistor that pre-charges said second bit line and provides a second supply of current for one or more leakage

currents drawn from said second bit line by any of said plurality of storage cells.

5 17. The apparatus of claim 16 wherein said processor is a general purpose processor.

18. The apparatus of claim 16 wherein said processor is a digital signal processor.

10 19. The apparatus of claim 16 further comprising a bus coupled to said memory.