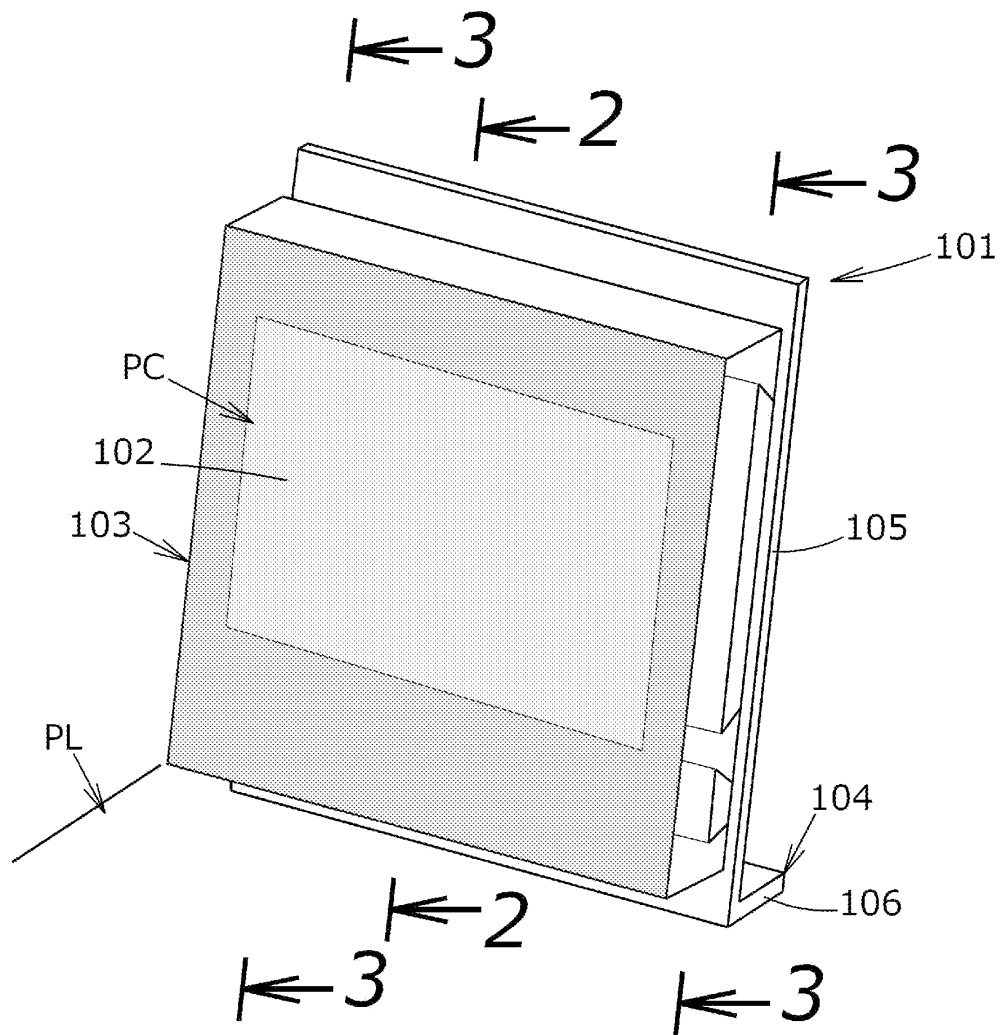
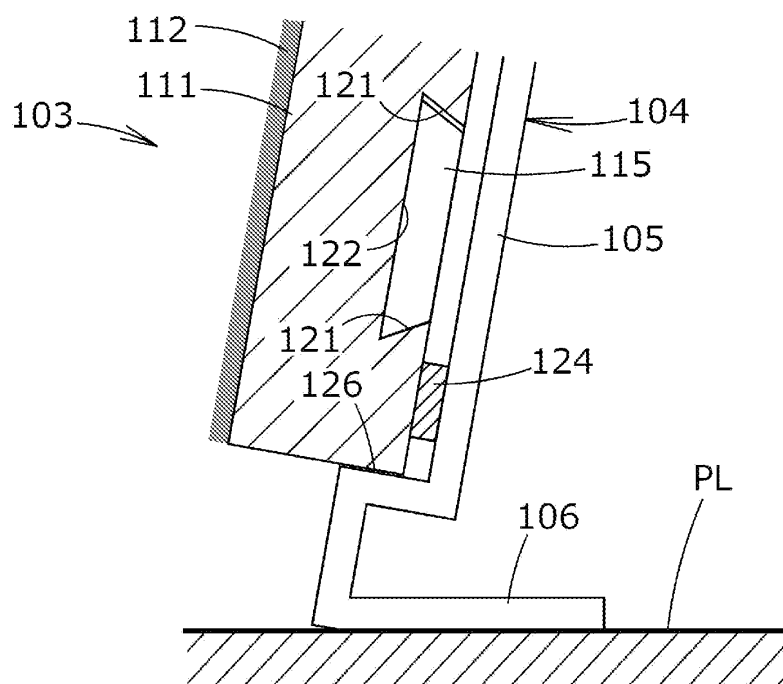


[図1]

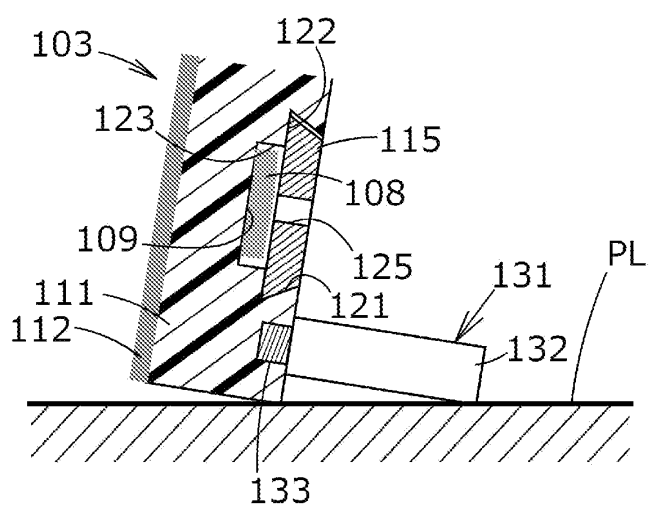


This diagram shows a cross-sectional view of a semiconductor device. A substrate 103 is shown with a trench 109. A gate structure 111 is formed on the side wall of the trench 109. The gate structure 111 includes a gate oxide layer 112 and a gate electrode 113. The gate electrode 113 is connected to a gate line 114. The gate line 114 is formed on a gate insulating layer 115. The gate insulating layer 115 is formed on a semiconductor layer 116. The semiconductor layer 116 is formed on a substrate 103. The gate structure 111 is formed on the side wall of the trench 109. The gate structure 111 includes a gate oxide layer 112 and a gate electrode 113. The gate electrode 113 is connected to a gate line 114. The gate line 114 is formed on a gate insulating layer 115. The gate insulating layer 115 is formed on a semiconductor layer 116. The semiconductor layer 116 is formed on a substrate 103.

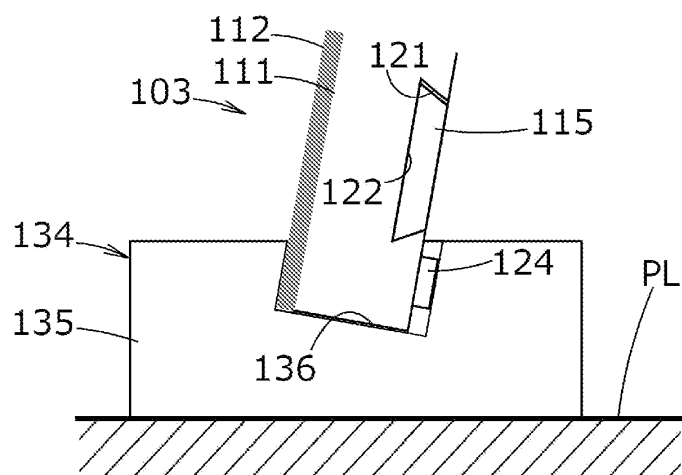
[図6]



[図7]



[図8]



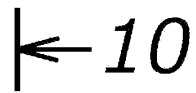
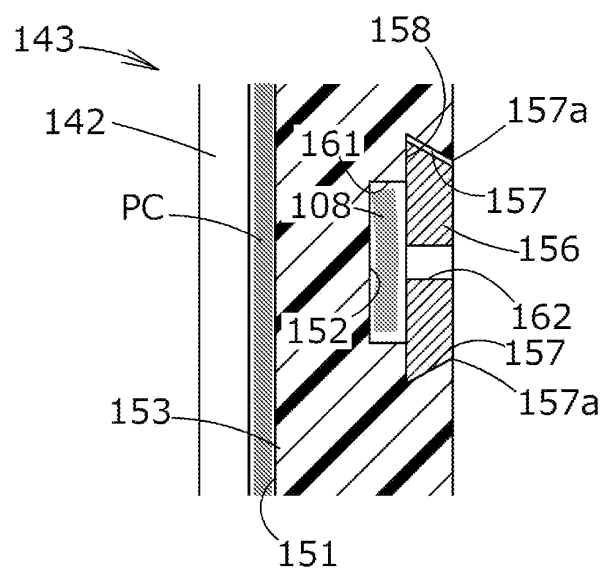
$\vdash 10$ 

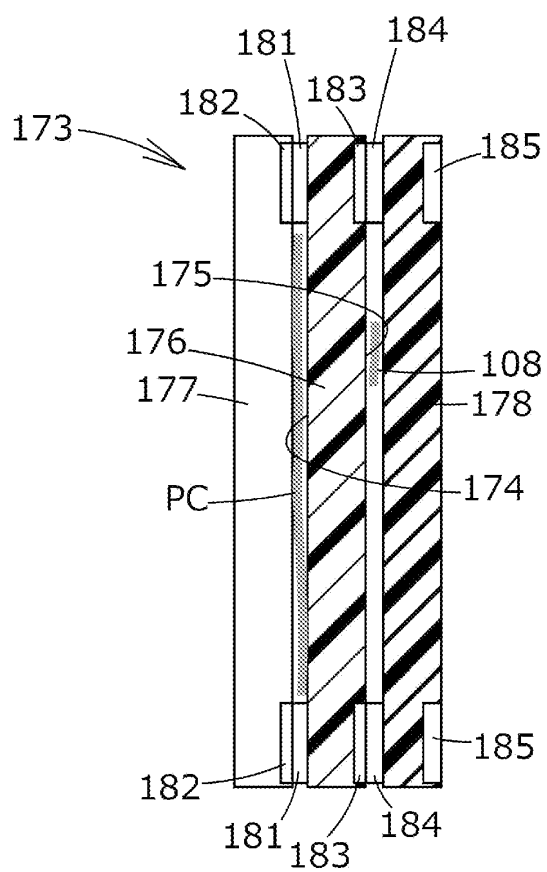
FIG. 10 is a schematic diagram of a second embodiment of a device. It shows a rectangular frame 141 containing a central panel 164. The panel has a top edge 164a and a bottom edge 164b. Various components are labeled: 146, 153, 143, 167a, 167, 154, 155, 166, 166a, 166b, 155, 154, 157, 162, 162, (157a), 158, 156, 159, 155, 163, 164, 144, 164b, and 164a.

(B)

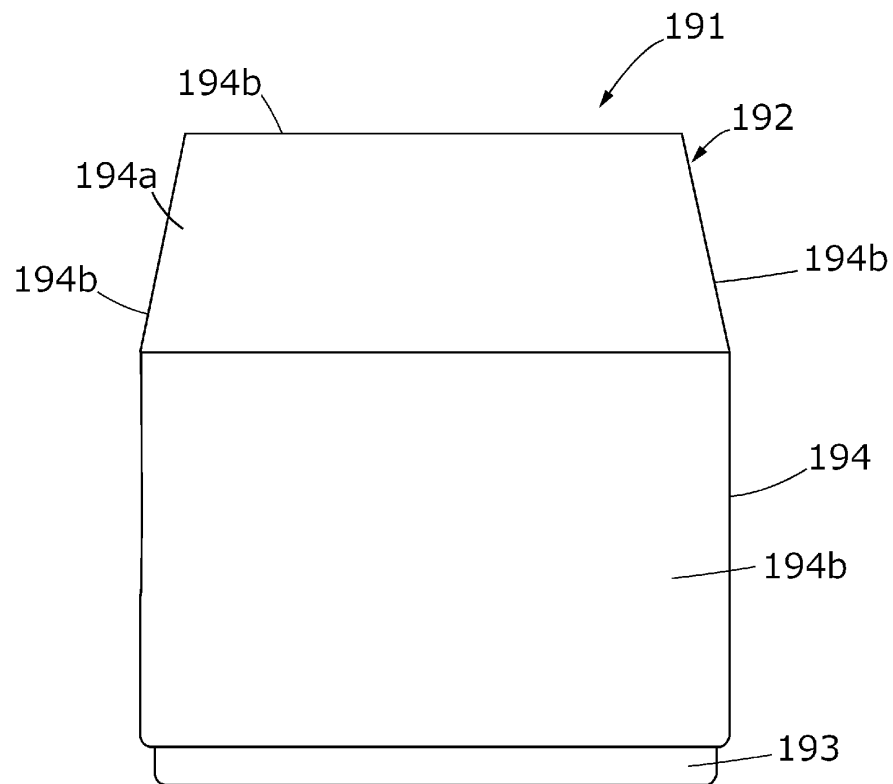
[図10]



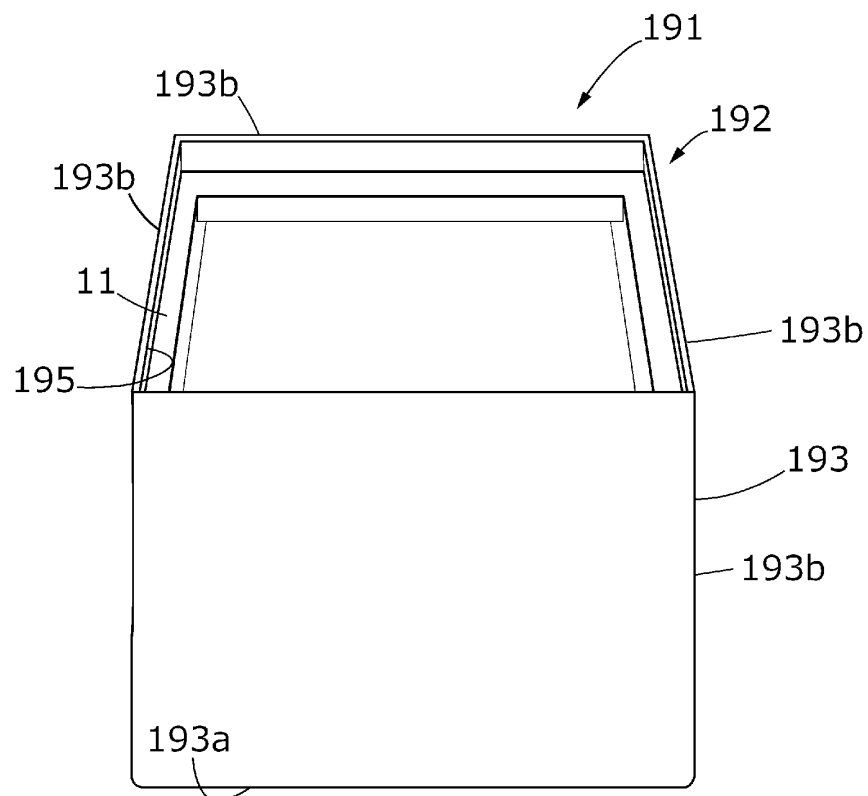
[図11]



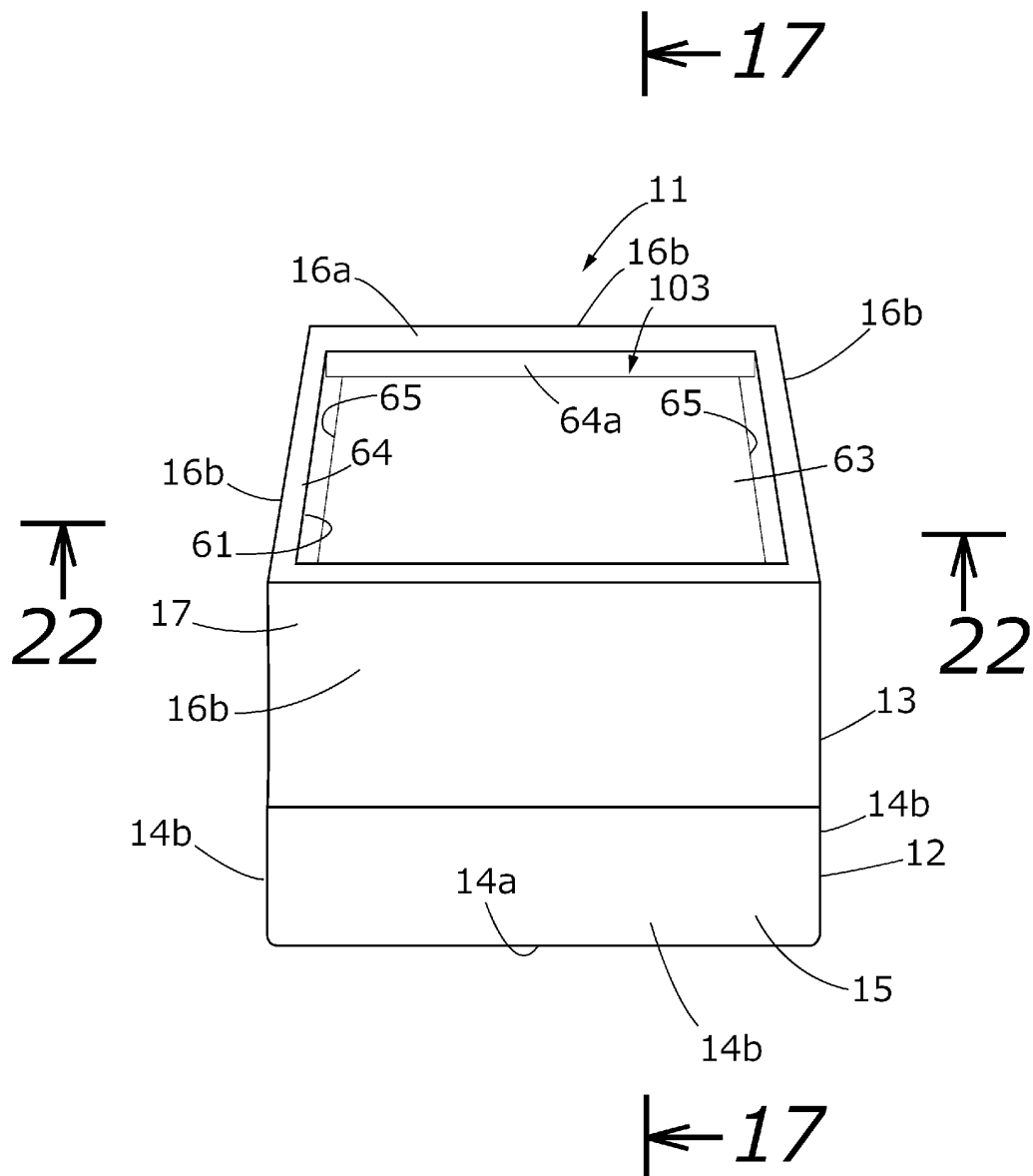
[図12]



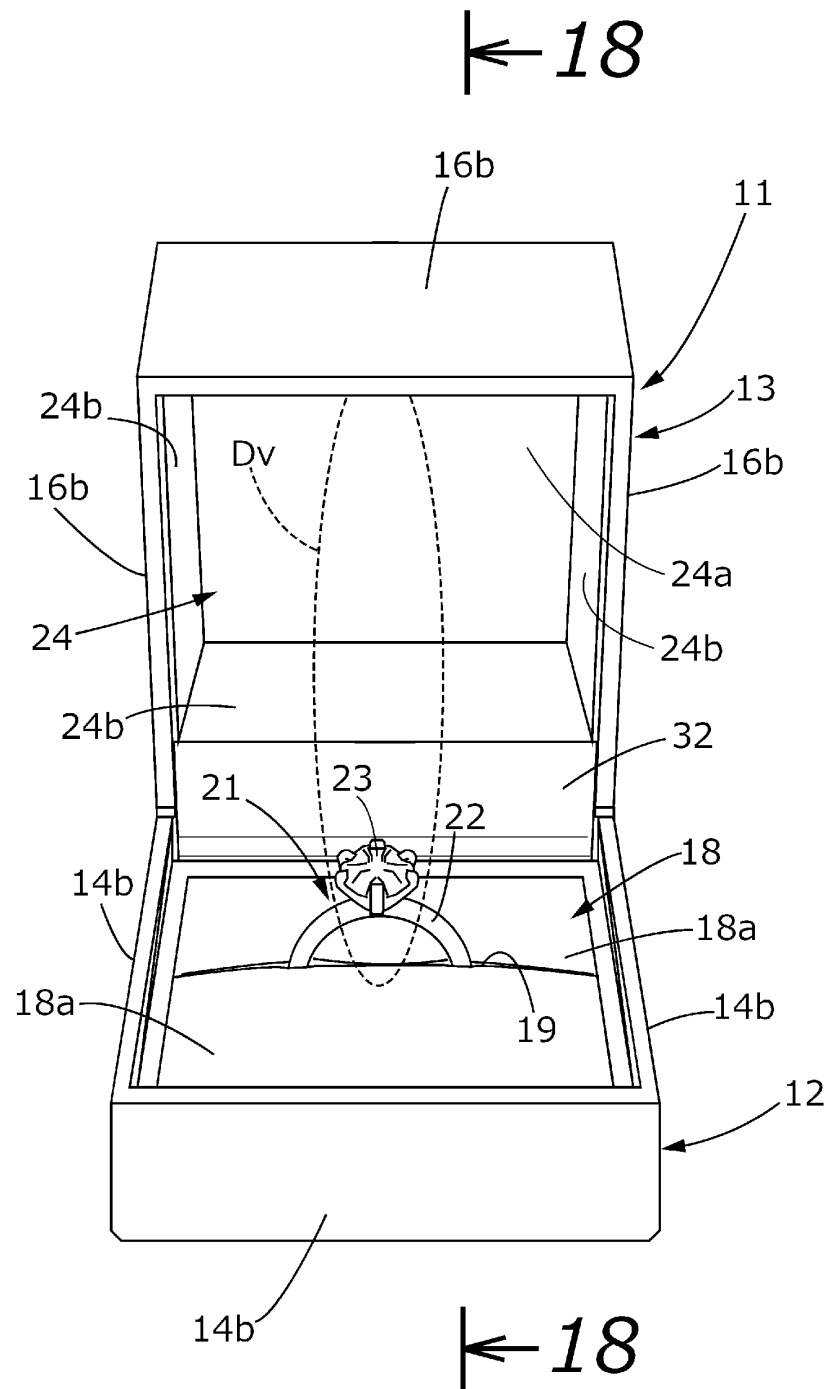
[図13]



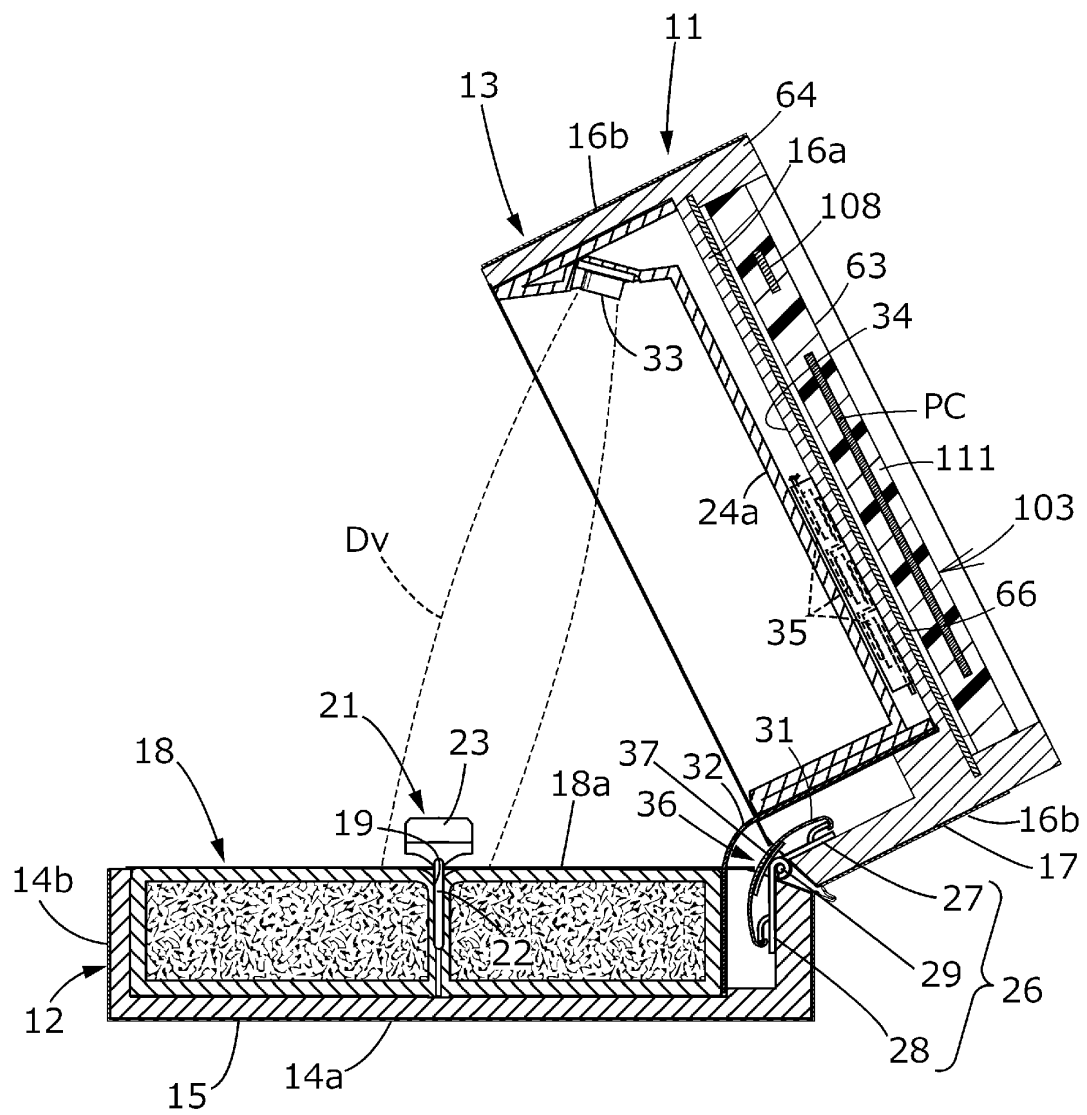
[図14]



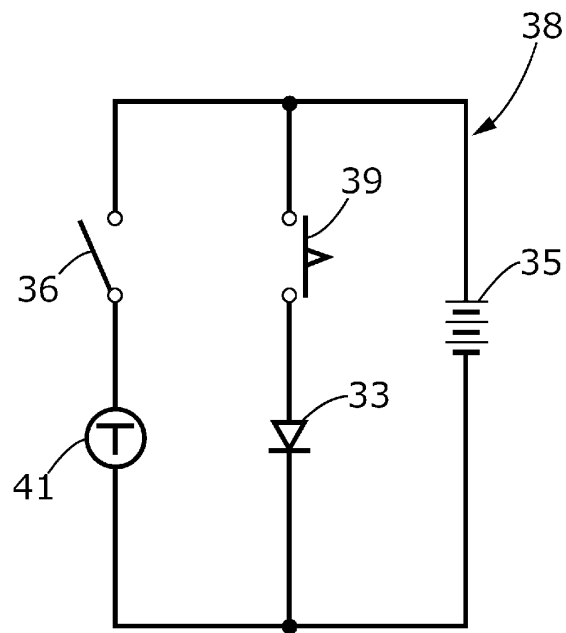
[図15]



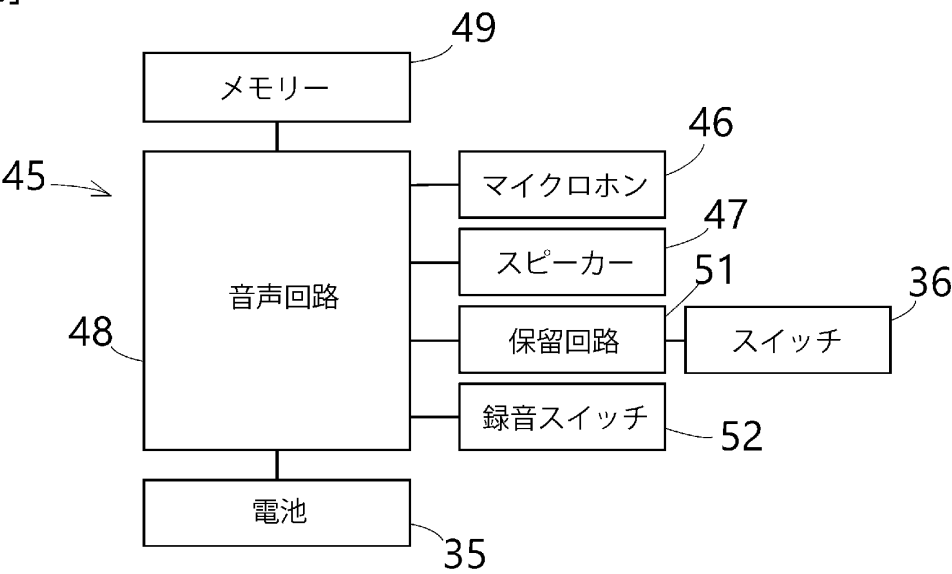
[図18]



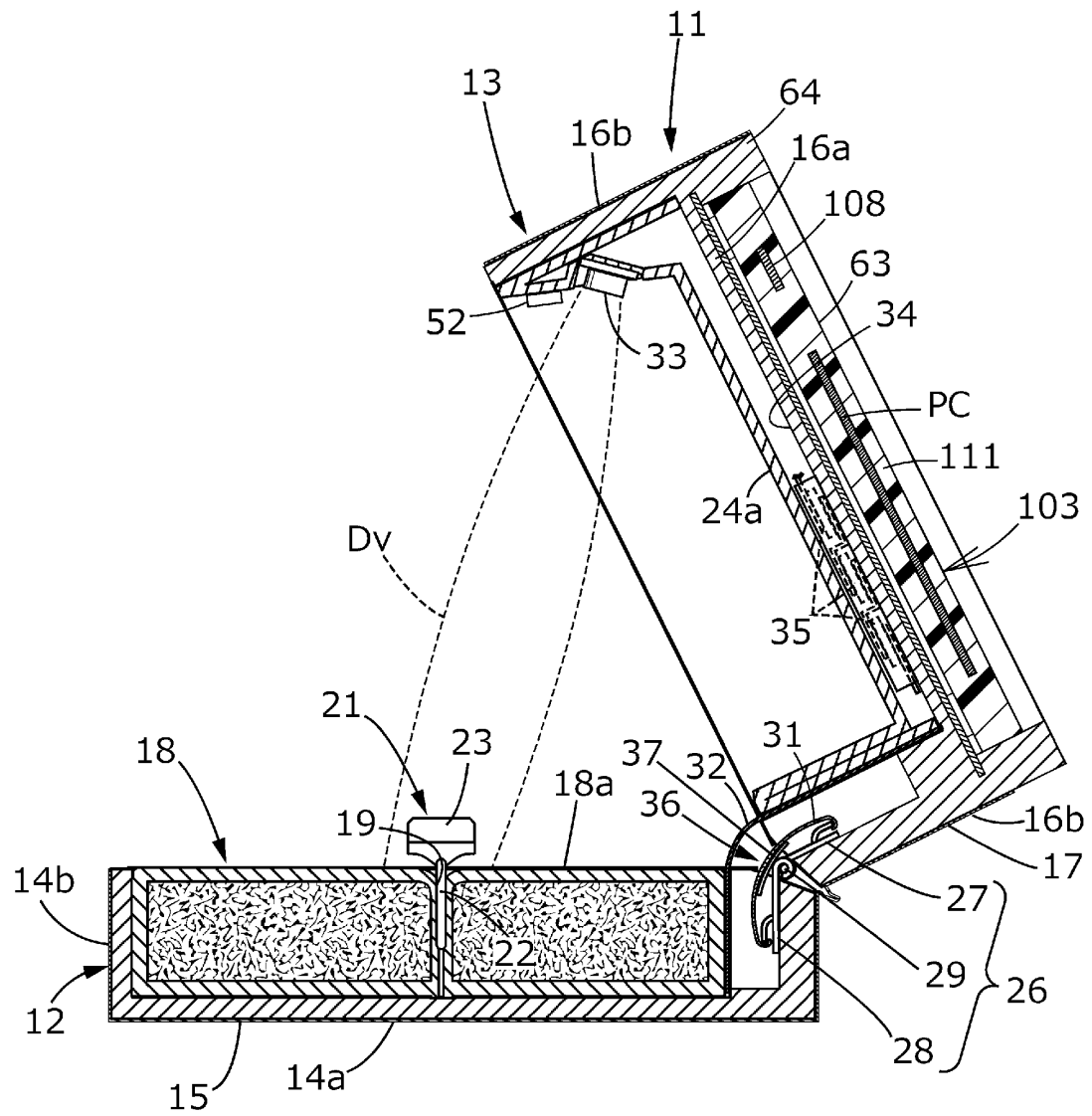
[図19]



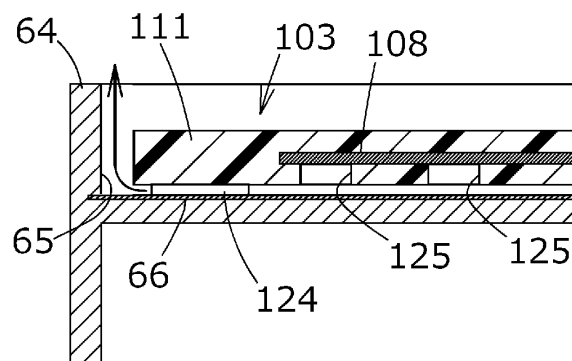
[図20]



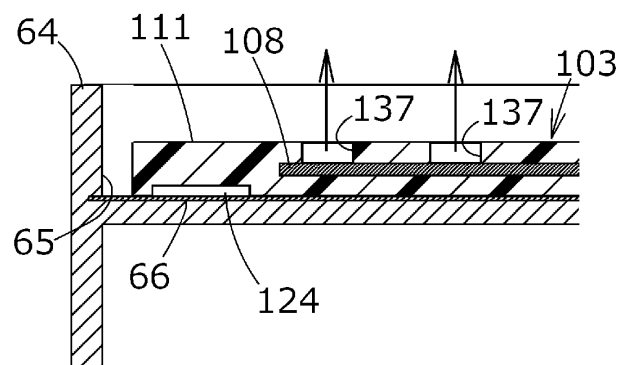
[図21]



[図22]



[図23]



[図24]

