A method for filtering Single Event Transients (SETs) comprising: providing an output buffer having a first pair of transistors wherein the first pair of transistors are a first PMOSFET and first NMOSFET and a second pair of transistors wherein the second pair of transistors are a second PMOSFET and a second NMOSFET, sending an input signal to the first pair of transistors, delaying the input signal by a predetermined amount of time to the second pair of transistors to form a delayed input signal, and driving an output buffer output signal when the input signal and the delayed input signal are at a same logic level.

According to an aspect of the present disclosure there is provided an interleaved filter circuit, comprising a delay element configured to receive an input signal, and an interleaved output buffer having a first input which receives the input signal, a second input which receives the output of the delay element, an output of the interleaved output buffer driven when the first input and the second input are at a same logic level, the interleaved output buffer comprising a plurality of interleaved transistors wherein the delay element is positioned between similar channel type transistors of the plurality of interleaved transistors.

Optionally, the interleaved filter interleaved output buffer comprises a first pair of transistors coupled to the input signal, and a second pair of transistors coupled to the output of the delay element wherein the first pair of transistors and the second pair of transistors are interleaved.

Optionally, the interleaved filter circuit interleaved output buffer comprises a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first P-type transistor and a first N-type transistor, and a second pair of transistors coupled to the output of the delay element, wherein the second pair of transistors are a second P-type transistor and a second N-type transistor, wherein the first N-type transistor and the second N-type transistor are interleaved and the first P-type transistor and the second P-type transistor are interleaved.

Optionally, the interleaved filter circuit interleaved output buffer comprises a first

the input signal and the output signal of the delay element are at a same logic level, wherein the interleaved output buffer comprises a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first PMOSFET and first NMOSFET, and a second pair of transistors coupled to the output of the interleaved output buffer, wherein the second pair of transistors are a second PMOSFET and a second NMOSFET wherein the first NMOSFET is interleaved with the second NMOSFET so that the delay element is positioned between the first NMOSFET and the second NMOSFET and the first PMOSFET is interleaved with the second PMOSFET so that the delay element is positioned between the first PMOSFET and the second PMOSFET.

Optionally, the interleaved filter circuit delay element provides a fixed time delay.

Optionally, the interleaved filter circuit delay element provides a programmable time delay.

Optionally, the interleaved filter circuit delay element provides a user selected time delay.

Optionally, the interleaved filter circuit delay element comprises a multiplexer, and a plurality of cascaded delay elements, wherein each of the plurality of cascaded delay elements has an output, and wherein the output of each of the plurality of cascaded delay elements is coupled to the multiplexer.

Optionally, the interleaved filter circuit delay element comprises a multiplexer, and a programmable delay element coupled to the multiplexer, the output of the delay element being determined by a programmable delay amount selected for the programmable delay element. Preferably the interleaved filter circuit programmable delay element comprises a plurality of transistor stacks, and a current mirror to control an amount of tail current flowing through the programmable delay element.

According to an aspect of the present disclosure there is provided a method for filtering Single Event Transients (SETs), the method comprising providing an output buffer having a first pair of transistors wherein the first pair of transistors are a first

PMOSFET and first NMOSFET and a second pair of transistors wherein the second pair of transistors are a second PMOSFET and a second NMOSFET, the first and second NMOSFETs being interleaved so that the delay element is positioned between the first NMOSFET and the second NMOSFET, the first and second PMOSFETs being interleaved so that the delay element is positioned between the first PMOSFET and the second PMOSFET, sending an input signal to the first pair of transistors, sending the input signal which is delayed by a predetermined amount of time to the second pair of transistors, and driving an output buffer output signal when the input signal and the delayed input signal are at a same logic level.

Optionally, sending the input signal which is delayed by a predetermined amount of time to the second pair of transistors comprises sending the input signal to a delay element. Preferably the delay element is programmable.

The features, functions, and advantages may be achieved independently in various embodiments of the disclosure or may be combined in yet other embodiments.

What is claimed is:

1. An interleaved filter circuit, comprising:

a delay element configured to receive an input signal; and

an interleaved output buffer having a first input which receives the input signal, a second input which receives the output of the delay element, an output of the interleaved output buffer driven when the first input and the second input are at a same logic level.

2. The interleaved filter circuit in accordance with Claim 1, wherein the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal; and

a second pair of transistors coupled to the output of the delay element;

wherein the first pair of transistors and the second pair of transistors are interleaved.

3. The interleaved filter circuit in accordance with Claim 1, wherein the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first P-type transistor and a first N-type transistor; and

a second pair of transistors coupled to the output of the delay element, wherein the second pair of transistors are a second P-type transistor and a second N-type transistor;

wherein the first N-type transistor and the second N-type transistor are interleaved and the first P-type transistor and the second P-type transistor are interleaved.

4. The interleaved filter circuit in accordance with Claim 1, wherein the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first PMOSFET and first NMOSFET; and

a second pair of transistors coupled to the output of the delay element, wherein the second pair of transistors are a second PMOSFET and a second NMOSFET;

wherein the first NMOSFET is interleaved with the second NMOSFET and the first PMOSFET is interleaved with the second PMOSFET.

5. The interleaved filter circuit in accordance with Claim 1, wherein the delay element provides a fixed time delay.

6. The interleaved filter circuit in accordance with Claim 1, wherein the delay element provides a programmable time delay.

7. The interleaved filter circuit in accordance with Claim 1, wherein the delay element provides a user selected time delay.

8. The interleaved filter circuit in accordance with Claim 1, wherein the delay element comprises:

a multiplexer; and

a plurality of cascaded delay elements, an output of each of the plurality of cascaded delay elements coupled to the multiplexer.

9. The interleaved filter circuit in accordance with Claim 1, wherein the delay element comprises:

a multiplexer; and

a programmable delay element coupled to the multiplexer, the output of the delay element being determined by a programmable delay amount selected for the programmable delay element.

10. The interleaved filter circuit in accordance with Claim 9, wherein the programmable delay element comprises:

a plurality of transistor stacks; and

a current mirror to control an amount of tail current flowing through the programmable delay element.

11. An interleaved filter circuit, comprising:

a delay element having an input signal and an output signal, the output signal of the delay element being at approximately a same level as the input signal after a predetermined amount of time determined by the delay element;

an interleaved output buffer having a first input coupled to the input signal, a second input coupled to the output signal of the delay element, an output buffer output signal being driven when the input signal and the output signal of the delay element are at a same logic level;

wherein the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first PMOSFET and first NMOSFET; and

a second pair of transistors coupled to the output of the interleaved output buffer, wherein the second pair of transistors are a second PMOSFET and a second NMOSFET;

wherein the first NMOSFET is interleaved with the second NMOSFET and the first PMOSFET is interleaved with the second PMOSFET.

12. The interleaved filter circuit in accordance with Claim 11, wherein the delay element provides a fixed time delay.

13. The interleaved filter circuit in accordance with Claim 11, wherein the delay element provides a programmable time delay.

14. The interleaved filter circuit in accordance with Claim 11, wherein the delay element provides a user selected time delay.

15. The interleaved filter circuit in accordance with Claim 11, wherein the delay element comprises:

a multiplexer; and

a plurality of cascaded delay elements, wherein each of the plurality of cascaded delay elements has an output, and wherein the output of each of the plurality of cascaded delay elements is coupled to the multiplexer.

16. The interleaved filter circuit in accordance with Claim 11, wherein the delay element comprises:

a multiplexer; and

a programmable delay element coupled to the multiplexer, the output of the delay element being determined by a programmable delay amount selected for the programmable delay element.

17. The interleaved filter circuit in accordance with Claim 16, wherein the programmable delay element comprises:

a plurality of transistor stacks; and

a current mirror to control an amount of tail current flowing through the

programmable delay element.

18. A method for filtering Single Event Transients (SETs), the method comprising:

providing an output buffer having a first pair of transistors wherein the first pair of transistors are a first PMOSFET and first NMOSFET and a second pair of transistors wherein the second pair of transistors are a second PMOSFET and a second NMOSFET, the first and second NMOSFETs being interleaved, the first and second PMOSFETs being interleaved;

sending an input signal to the first pair of transistors;

delaying the input signal by a predetermined amount of time to the second pair of transistors to form a delayed input signal; and

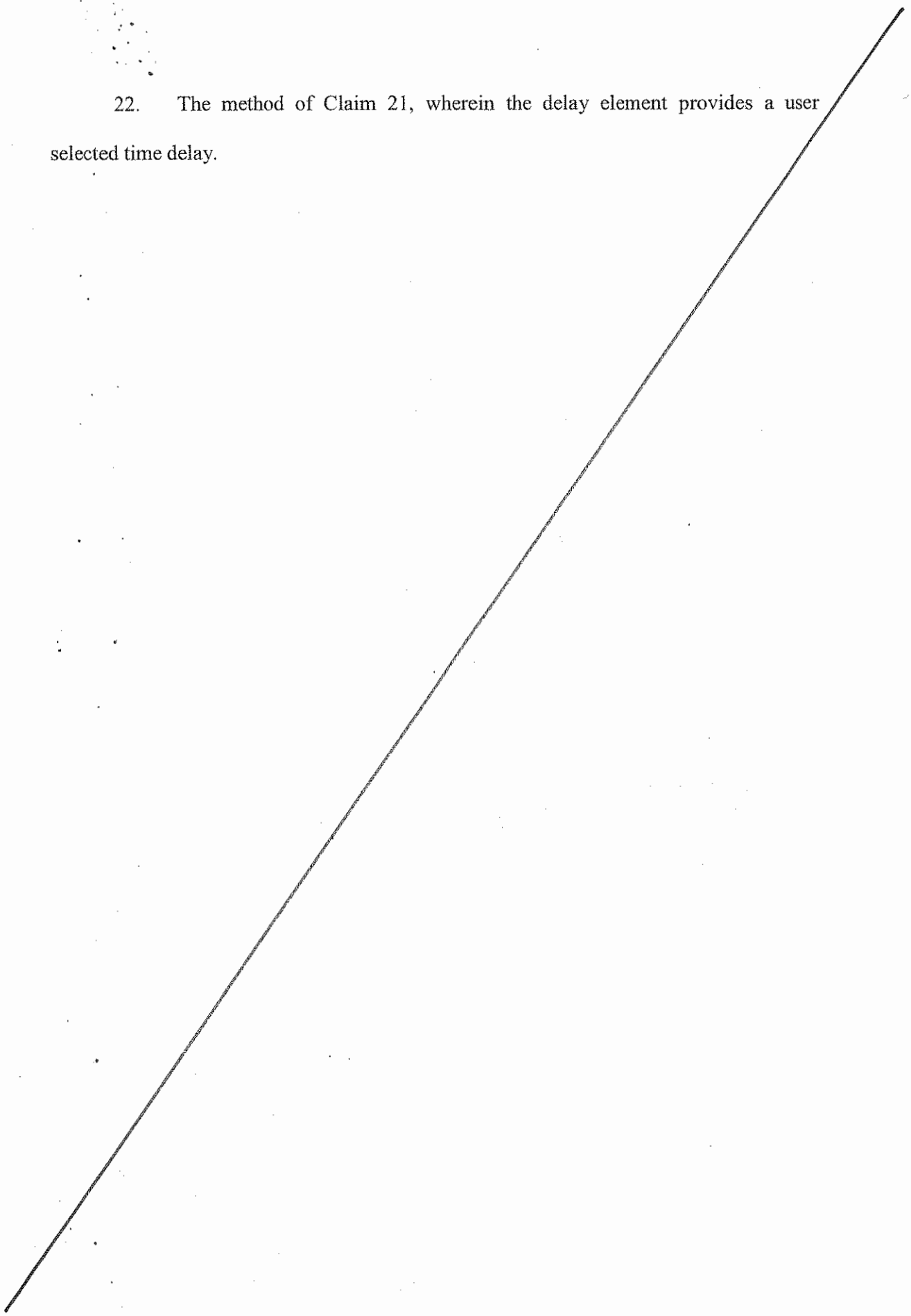
driving an output buffer output signal when the input signal and the delayed input signal are at a same logic level.

19. The method of Claim 18, wherein delaying the input signal comprises sending the input signal to a delay element.

20. The method of Claim 18, wherein the delay element provides a fixed time delay.

21. The method of Claim 18, wherein the delay element is programmable.

22. The method of Claim 21, wherein the delay element provides a user selected time delay.



What is claimed is:

1. An interleaved filter circuit, comprising:

a delay element configured to receive an input signal; and

an interleaved output buffer having a first input which receives the input signal, a second input which receives the output of the delay element, an output of the interleaved output buffer driven when the first input and the second input are at a same logic level, the interleaved output buffer comprising a plurality of interleaved transistors wherein the delay element is positioned between similar channel type transistors of the plurality of interleaved transistors.

2. The interleaved filter circuit in accordance with claim 1, wherein the plurality of interleaved transistors of the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first P-type transistor and a first N-type transistor; and

a second pair of transistors coupled to the output of the delay element, wherein the second pair of transistors are a second P-type transistor and a second N-type transistor;

wherein the first N-type transistor and the second N-type transistor are interleaved wherein the delay element is positioned between the first N-type transistor and the second N-type transistor and the first P-type transistor and the second P-type transistor are interleaved wherein the delay element is positioned between the first P-type transistor and the second P-type transistor.

3. The interleaved filter circuit in accordance with claim 1, wherein the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first PMOSFET and first NMOSFET; and

a second pair of transistors coupled to the output of the delay element, wherein the second pair of transistors are a second PMOSFET and a second NMOSFET;

wherein the first NMOSFET is interleaved with the second NMOSFET so that the delay element is positioned between the first NMOSFET and the second NMOSFET and the first PMOSFET is interleaved with the second PMOSFET so that the delay element is positioned between the first PMOSFET and the second PMOSFET transistor.

4. The interleaved filter circuit in accordance with claim 1, wherein the delay element provides a fixed time delay.

5. The interleaved filter circuit in accordance with claim 1, wherein the delay element provides a programmable time delay.

6. The interleaved filter circuit in accordance with claim 1, wherein the delay element provides a user selected time delay.

7. The interleaved filter circuit in accordance with claim 1, wherein the delay element comprises:

a multiplexer; and

a plurality of cascaded delay elements, an output of each of the plurality of cascaded delay elements coupled to the multiplexer.

8. The interleaved filter circuit in accordance with claim 1, wherein the delay element comprises:

a multiplexer; and

a programmable delay element coupled to the multiplexer, the output of the delay element being determined by a programmable delay amount selected for the programmable delay element.

9. The interleaved filter circuit in accordance with claim 8, wherein the programmable delay element comprises:

a plurality of transistor stacks; and

a current mirror to control an amount of tail current flowing through the programmable delay element.

10. An interleaved filter circuit, comprising:

a delay element having an input signal and an output signal, the output signal of the delay element being at approximately a same level as the input signal after a predetermined amount of time determined by the delay element;

an interleaved output buffer having a first input coupled to the input signal, a second input coupled to the output signal of the delay element, an output buffer output signal being

driven when the input signal and the output signal of the delay element are at a same logic level;

wherein the interleaved output buffer comprises:

a first pair of transistors coupled to the input signal, wherein the first pair of transistors are a first PMOSFET and first NMOSFET; and

a second pair of transistors coupled to the output of the interleaved output buffer, wherein the second pair of transistors are a second PMOSFET and a second NMOSFET;

wherein the first NMOSFET is interleaved with the second NMOSFET so that the delay element is positioned between the first NMOSFET and the second NMOSFET and the first PMOSFET is interleaved with the second PMOSFET so that the delay element is positioned between the first PMOSFET and the second PMOSFET.

11. The interleaved filter circuit in accordance with claim 10, wherein the delay element provides a fixed time delay.

12. The interleaved filter circuit in accordance with claim 10, wherein the delay element provides a programmable time delay.

13. The interleaved filter circuit in accordance with claim 10, wherein the delay element provides a user selected time delay.

14. The interleaved filter circuit in accordance with claim 10, wherein the delay element comprises:

a multiplexer; and

a plurality of cascaded delay elements, wherein each of the plurality of cascaded delay elements has an output, and wherein the output of each of the plurality of cascaded delay elements is coupled to the multiplexer.

15. The interleaved filter circuit in accordance with claim 10, wherein the delay element comprises:

a multiplexer; and

a programmable delay element coupled to the multiplexer, the output of the delay element being determined by a programmable delay amount selected for the programmable delay element.

16. The interleaved filter circuit in accordance with claim 15, wherein the programmable delay element comprises:

a plurality of transistor stacks; and

a current mirror to control an amount of tail current flowing through the programmable delay element.

17. A method for filtering Single Event Transients (SETs), the method comprising:

providing an output buffer having a first pair of transistors wherein the first pair of transistors are a first PMOSFET and first NMOSFET and a second pair of transistors wherein the second pair of transistors are a second PMOSFET and a second NMOSFET, the first and second NMOSFETs being interleaved so that the delay element is positioned between the first NMOSFET and the second NMOSFET, the first and second PMOSFETs being interleaved so that the delay element is positioned between the first PMOSFET and the second PMOSFET;

sending an input signal to the first pair of transistors;

sending the input signal which is delayed by a predetermined amount of time to the second pair of transistors; and

driving an output buffer output signal when the input signal and the delayed input signal are at a same logic level.

18. The method of claim 17, wherein sending the input signal which is delayed by a predetermined amount of time to the second pair of transistors comprises sending the input signal to a delay element.

19. The method of claim 18, wherein the delay element is programmable.