WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first pin configured to receive a first signal and a second signal having a smaller amplitude than the first signal;

a first receiving circuit connected to the first pin and configured to output a third signal and a fourth signal having a smaller amplitude than the third signal, the first receiving circuit outputting the third signal based on a comparison between the first signal and a first voltage, the first receiving circuit outputting the fourth signal based on a comparison between the second signal and a second voltage;

a first terminating circuit connected to the first pin and configured to be disabled if the first pin receives the first signal and enabled if the first pin receives the second signal;

a second pin configured to receive a fifth signal and a sixth signal having a smaller amplitude than the fifth signal;

a second receiving circuit connected to the second pin and configured to output a seventh signal and an eighth signal having a smaller amplitude than the seventh signal, the second receiving circuit outputting the seventh signal based on a comparison between the fifth signal and the first voltage, and the second receiving circuit outputting the eighth signal based on a comparison between the sixth

signal and the second voltage;

a second terminating circuit connected to the second pin and configured to be disabled if the second pin receives the fifth signal and enabled if the second pin receives the sixth signal;

a third pin configured to receive a ninth signal and a tenth signal having a smaller amplitude than the ninth signal;

a third receiving circuit connected to the third pin and configured to output an eleventh signal and a twelfth signal having a smaller amplitude than the eleventh signal, the third receiving circuit outputting the eleventh signal based on a comparison between the ninth signal and the first voltage, and the third receiving circuit outputting the twelfth signal based on a comparison between the tenth signal and the second voltage; and

a third terminating circuit connected to the third pin and configured to be disabled if the third pin receives the ninth signal and enabled if the third pin receives the tenth signal.

2. The semiconductor memory device according to claim 1, wherein

the second voltage is smaller than the first voltage.

3. The semiconductor memory device according to claim 1, wherein

the first terminating circuit includes a first resistor and a first switch connected in series between the

first pin and a node for supplying a ground voltage.

4. The semiconductor memory device according to claim 1, wherein

the first signal includes a command or an address, and

the second signal includes a parameter value or write data.

5. The semiconductor memory device according to claim 1, further comprising

a first transmitting circuit configured to output the fifth signal and the sixth signal, wherein

the fifth signal includes data indicative of a status, and

the sixth signal includes read data.

6. The semiconductor memory device according to claim 1, further comprising

a first transmitting circuit configured to output the fifth signal to the first pin, wherein

the fifth signal includes status or read data.

7. The semiconductor memory device according to claim 6, wherein

an output node of the first transmitting circuit is connected, via an NMOS transistor, to a node for supplying a supply voltage.

8. The semiconductor memory device according to claim 1, further comprising:

a fourth pin configured to receive a thirteenth signal and a fourteenth signal having a smaller amplitude than the

thirteenth signal;

a fourth receiving circuit connected to the fourth pin and configured to output a fifteenth signal and a sixteenth signal having a smaller amplitude than the fifteenth signal, the fourth receiving circuit outputting the fifteenth signal based on a comparison between the thirteenth signal and the first voltage, the fourth receiving circuit outputting the sixteenth signal based on a comparison between the fourteenth signal and the second voltage;

a fourth terminating circuit connected to the fourth pin and configured to be disabled if the fourth pin receives the thirteenth signal and enabled if the fourth pin receives the fourteenth signal;

a fifth pin configured to receive a seventeenth signal and an eighteenth signal having a smaller amplitude than the seventeenth signal;

a fifth receiving circuit connected to the fifth pin and configured to output a nineteenth signal and a twentieth signal having a smaller amplitude than the nineteenth signal, the fifth receiving circuit outputting the nineteenth signal based on a comparison between the seventeenth signal and the first voltage, the fifth receiving circuit outputting the twentieth signal based on a comparison between the eighteenth signal and the second voltage; and

a fifth terminating circuit connected to the fifth pin

and configured to be disabled if the fifth pin receives the seventeenth signal and enabled if the fifth pin receives the eighteenth signal.

9. The semiconductor memory device according to claim 8, further comprising:

a first circuit connected to the second receiving circuit and the third receiving circuit and configured to output a twenty-first signal and a twenty-second signal, the first circuit outputting the twenty-first signal and the twenty-second signal based on the seventh signal and the eleventh signal or based on the eighth signal and the twelfth signal; and

a latch circuit configured to store, based on the twenty-first signal and the twenty-second signal, data included in the third signal or the fourth signal.

10. The semiconductor memory device according to claim 1, further comprising

a first chip including the first pin, the first receiving circuit, and the first terminating circuit.

11. The semiconductor memory device according to claim 1, further comprising:

a first chip including the first pin and the first receiving circuit; and

a second chip including the first terminating circuit.

12. The semiconductor memory device according to claim 11, wherein

after receipt of a first command which is the first

signal and up to receipt of a second command, the first terminating circuit is in an enabled state for a period where the second chip is receiving a signal for enabling the second chip.

13. A memory system comprising:

a first transmitting circuit configured to receive a first signal and output a second signal having a smaller amplitude than the first signal;

a first pin configured to receive the second signal;

a first receiving circuit connected to the first pin and configured to output a third signal based on a comparison between the second signal and a first voltage; and

a first terminating circuit connected to the first pin and configured to be in an enabled state for a period where the first pin is receiving the second signal,

wherein an output node of the first transmitting circuit is connected, via an NMOS transistor, to a node for supplying a supply voltage.

14. The memory system according to claim 13, wherein

the first terminating circuit includes a first resistor and a first switch connected in series between the first pin and a node for supplying a ground voltage.

15. The memory system according to claim 13, wherein

the first signal includes a command or an address.

16. The memory system according to claim 15, wherein

the first signal further includes a parameter value or

write data.

17. The memory system according to claim 13, further comprising

a second transmitting circuit configured to receive a fourth signal and output a fifth signal to the first pin, the fifth signal having a smaller amplitude than the fourth signal, wherein

the fifth signal includes data indicative of a status, or write data, and

an output node of the second transmitting circuit is connected, via an NMOS transistor, to a node for supplying the supply voltage.

18. The memory system according to claim 13, further comprising:

a second transmitting circuit configured to receive a fourth signal and output a fifth signal having a smaller amplitude than the fourth signal;

a second pin configured to receive the fifth signal;

a second receiving circuit connected to the second pin and configured to output a sixth signal based on a comparison between the fifth signal and the first voltage;

a second terminating circuit connected to the second pin and configured to be in an enabled state for a period where the second pin is receiving the fifth signal;

a third transmitting circuit configured to receive a seventh signal and output an eighth signal having a smaller amplitude than the seventh signal;

a third pin configured to receive the eighth signal;

a third receiving circuit connected to the third pin and configured to output a ninth signal based on a comparison between the eighth signal and the first voltage; and

a third terminating circuit connected to the third pin and configured to be in an enabled state for a period where the third pin is receiving the eighth signal.

19. The memory system according to claim 18, further comprising:

a fourth transmitting circuit configured to receive a tenth signal and output an eleventh signal having a smaller amplitude than the tenth signal;

a fourth pin configured to receive the eleventh signal;

a fourth receiving circuit connected to the fourth pin and configured to output a twelfth signal based on a comparison between the eleventh signal and the first voltage;

a fourth terminating circuit connected to the fourth pin and configured to be in an enabled state for a period where the fourth pin is receiving the eleventh signal;

a fifth transmitting circuit configured to receive a thirteenth signal and output a fourteenth signal having a smaller amplitude than the thirteenth signal;

a fifth pin configured to receive the fourteenth signal;

a fifth receiving circuit connected to the fifth pin and configured to output a fifteenth signal based on a comparison between the fourteenth signal and the first voltage; and

a fifth terminating circuit connected to the fifth pin and configured to be in an enabled state for a period where the fifth pin is receiving the fourteenth signal.

20. The memory system according to claim 19, further comprising:

a first circuit connected to the second receiving circuit and the third receiving circuit and configured to output a sixteenth signal and a seventeenth signal based on the sixth signal and the ninth signal; and

a latch circuit configured to store, based on the sixteenth signal and the seventeenth signal, data included in the third signal.

21. The memory system according to claim 13, further comprising

a first chip including the first pin, the first receiving circuit, and the first terminating circuit.

22. The memory system according to claim 13, further comprising:

a first chip including the first pin and the first receiving circuit; and

a second chip including the first terminating circuit.

23. The memory system according to claim 22, wherein

after receipt of a first command which is the first

signal and up to receipt of a second command, the first terminating circuit is in an enabled state for a period where the second chip is receiving a signal for enabling the second chip.

24. The memory system according to claim 13, further comprising:

a memory controller including the first transmitting circuit; and

a semiconductor memory device including the first pin and the first terminating circuit.