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Description

Electronic component with an integrated passive electronic component and method for production thereof

The invention relates to an electronic component having an integrated electronic component and a method for producing this electronic component.

Most analogue circuit sections of hybrid digital/analogue circuits require passive components, for example capacitors with a high capacitance, a high degree of linearity and high quality. In order to minimize the costs of producing the component, it is necessary that the production of the passive components, in particular capacitance or inductance structures, require as few process steps as possible. Furthermore, the advancing miniaturization of the components and integrated circuits is also accompanied by the demand for the least possible area requirement for the said integrated passive components.

The patent specification US 5,583,359 discloses a capacitance structure for an integrated circuit. In that case, a plurality of metal plates which form the electrodes of a stacked capacitor are arranged one above the other, separated by dielectric layers. Arranged in each plane of a metal plate is a metal line insulated from the respective plate. The metal lines are in each case contact-connected on both sides by via connections, as a result of which, on the one hand, all the plates positioned in odd-numbered fashion in the stack and, on the other hand, all the plates positioned in even-numbered fashion in the stack are electrically connected to one another. By connecting the plates positioned in even-numbered fashion to a first connection line and the plates positioned in odd-numbered fashion to a second connection line, adjacent

plates are at a different potential and form pairwise in each case electrodes of a plate capacitor. The capacitance surface area is thus formed by the plate surfaces. An alternative embodiment of the electrodes is provided by forming the plates as strip-type lines arranged parallel to one another.

Further possible configurations of capacitance structures are disclosed in Aparicio, R. and Hajimiri, A.: Capacity Limits and Matching Properties of Integrated Capacitors; IEEE Journal of Solid-State Circuits, Vol. 37, No. 3, 2002, pp. 384-393, which are shown in perspective illustration there in Figures 5 to 10.

Furthermore, in novel chips in which dielectric regions are formed whose materials have low dielectric constants (for example SiLK (organic material having a dielectric constant of 2.65), black diamond, coral (both carbon-doped oxides having a dielectric constant of less than 3) or porous formations of these dielectrics), it is necessary to form mechanical reinforcements in order to avoid damage on account of the low hardness of these dielectric materials under the action of mechanical force on the component.

Components in which both passive components and mechanical supporting structures are necessary therefore require a relatively large amount of space. What is more, the mechanical supporting structure is no longer required after the completion of the component, in particular after bonding and mounting of the component in the housing.

Therefore, it is an object of the invention to provide an electronic component having an integrated passive electronic component and a method for producing it which can be produced with a relatively low outlay and

in a space-saving manner and is robust towards any action of mechanical force.

This object is achieved by means of an electronic component having the features of Patent Claim 1 and by means of a method having the steps according to Patent Claim 18.

An electronic component according to the invention has a first insulation layer, on which an upper metal layer is formed. The upper metal layer is formed as an electrically conductive bonding pad layer, in particular, to which are bonded, by way of example, aluminium or gold wires for electrically connecting the contact regions of the electronic component or the chip to the contact tracks of a housing in which the electronic component is mounted. An electrically conductive structure is integrated in the first insulation layer and mechanically stabilizes the first insulation layer under the action of mechanical force, in particular during the bonding of the upper metal layer and/or the mounting of the electronic component. The electrically conductive structure is additionally formed as a passive electronic component.

As a result, it is possible to produce an electronic component which needs a relatively low space requirement and can be realized with a relatively low outlay. The electrically conductive structure in the electronic component serves, on the one hand, as a mechanical supporting structure under the action of mechanical force on the component, in particular as a mechanical supporting structure for the first insulation layer, and, on the other hand, as a passive component of the electronic component. This individual structure with a dual function reduces the process steps during production and thus the manufacturing costs since mechanical supporting or stability

structure and passive component structures do not have to be produced separately.

In a preferred exemplary embodiment, the first insulation layer is formed as a dielectric layer made of a material whose dielectric constant has a value of less than 4. By way of example, the dielectric constant of SiLK, an organic material, has the value 2.65. Other materials may be, for example, coral or black diamond, which are carbon-doped oxides and have a dielectric constant of less than 3. The small modulus and the low hardness of these materials mean that even relatively low mechanical forces can lead to damage, as a result of which, therefore, in this case the integrated electrically conductive structure as mechanical stabilization proves to be particularly advantageous. The first insulation layer may also be formed as a multilayer system in which the individual layers in some instances also have dielectric constants higher than 4. What is essential in this case is that the multilayer system has an average dielectric constant whose value is less than 4, in particular less than 3.

In an advantageous exemplary embodiment, the electrically conductive structure is essentially arranged vertically below a bonding region of the upper metal layer. The bonding region, which essentially denotes that region of the upper metal layer in which the electrical connections, in particular the contact wires, for producing the electrical contact with the contact tracks of the housing are arranged, can be realized in diverse ways. Directly arranging the electrically conductive structure below the said bonding region enables an optimized mechanical stability. It is particularly preferred if the dimensions of the electrically conductive structure in a plane parallel to the upper metal layer has at least the dimensions of the bonding region. Irrespective of where a bonding or an action of mechanical force acts

on the bonding region, the first insulation layer or the entire electronic component can therefore be protected from mechanical damage or destruction.

It is particularly advantageous to arrange the electrically conductive structure in the first insulation layer in such a way that the electrically conductive structure is essentially flush with the horizontal planes of the first insulation layer. Consequently, the electrically conductive structure is formed in the first insulation layer in such a way that partial regions of the horizontal surfaces of the first insulation layer are formed by surface regions of the electrically conductive structure. In this case, the electrically conductive structure is formed with maximal extent in the first insulation layer in the vertical direction (first insulation layer and electrically conductive structure have essentially identical dimensions in the vertical direction). The mechanical stability can be improved again as a result of this since there is no mechanically less stable or "softer" region of the first insulation layer below the bonding region which is not supported by the electrically conductive structure.

A further advantageous embodiment is characterized in that the electrically conductive structure is connected to a supply voltage potential by means of via connections by means of a metal strip, in particular contact metal strip, formed in a further metallization plane and is connected to earth potential by means of via connections by means of a further metal strip formed in a metallization plane. It may be provided that both contact strips are formed in a second insulation layer which is produced from a material having a high mechanical stability in comparison with the mechanical stability of the material of the first insulation layer. The elastic modulus of the material of the second insulation layer preferably has a value

of greater than 15 gigapascals, in particular a value of greater than 20 gigapascals, and a hardness of greater than 4. However, it may also be provided that only one or none of the contact strips is formed in the second insulation layer. This is missing on the geometry of the electrically conductive structure and the associated arrangement of the contact metal strips. Forming at least one metal strip - which enables the electrically conductive structure to be electrically contact-connected to voltage potentials - in a second insulation layer made of a material having high mechanical stability achieves additional stabilization of the electronic component under the action of mechanical force, in particular on the bonding region of the upper metal layer. An oxide layer or a layer made of FSG (fluorosilicate glass) dielectric may be formed as the second insulation layer.

It is particularly advantageous if an electrically conductive screening layer is formed between the upper metal layer and the electrically conductive structure. The electrically conductive screening layer is insulated both from the upper metal layer and from the electrically conductive structure. The screening layer may advantageously be formed as a metal layer which is preferably connected to earth potential. What can be achieved as a result of this is that the signals applied to the upper metal layer cannot couple into the underlying electrically conductive structure and the signals applied to the electrically conductive structure or to the passive component cannot couple into the upper metal layer.

It is advantageous to form the screening layer in a third insulation layer, the third insulation layer being arranged between the upper metal layer and the first insulation layer. Forming the third insulation layer preferably as an oxide layer makes it possible to obtain a further mechanical reinforcement of the first

insulation layer. The screening layer may be formed as a contiguous plate or as a grid structure.

A particularly effective electrical screening can be obtained when the screening layer is advantageously formed in such a way that that area of the screening layer which faces the electrically conductive structure is at least equal in magnitude to that area of the electrically conductive structure which faces the screening layer. The screening layer is preferably formed on the electrically conductive structure in such a way that, in the case of a plan view of the screening layer, the contour of the area of the screening layer covers the contour of the area of the electrically conductive structure.

It is particularly advantageous if the electrically conductive structure is formed as a capacitance structure and/or as an inductance structure. In this case, it may be provided that the electrically conductive structure is produced completely as a capacitance or completely as an inductance. However, the electrically conductive structure may also comprise a plurality of partial structures, one partial structure being arranged as a capacitance and a further partial structure being arranged as an inductance in the first insulation layer.

A preferred exemplary embodiment of the electrically conductive structure is characterized in that at least one partial structure is formed as a capacitance structure, which extends over at least two metallization planes, and metal strips arranged parallel to one another and in a manner electrically insulated from one another are formed in each metallization plane. The metal strips of the first metallization plane are arranged essentially congruently with respect to the metal strips of the second metallization plane and are electrically

connected to one another by via connections in the vertical direction.

A further advantageous exemplary embodiment is provided by the fact that at least one partial structure of the electrically conductive structure is formed as an inductance structure and has at least one metallization plane in which a spiral metal track is formed.

The upper metal layer may be contact-connected by means of a contact hole in the second insulation layer to an electrically conductive region formed underneath, in particular in the third insulation layer. The contact hole is preferably arranged in the region outside the bonding region of the upper metal layer and, in the same way as the electrically conductive region, may be arranged horizontally offset with respect to the electrically conductive structure.

In a preferred exemplary embodiment, the electronic component according to the invention is arranged on a substrate in an integrated circuit.

In a method according to the invention for producing an electronic component, in a first insulation layer, an electrically conductive structure is formed as at least one passive electronic component and as a mechanical stabilization structure for supporting the first insulation layer under the action of mechanical force. There is produced on the first insulation layer an upper metal layer, which is formed as an electrically conductive bonding pad layer, in particular, on which actions of mechanical force are exerted in particular during bonding or during mounting of the electronic component.

A structure having a dual function for the electronic component is thus produced in a simple manner exhibiting a low outlay. As a result, the electronic

component can be realized in a space-saving manner and cost-effectively.

In an advantageous exemplary embodiment, the first insulation layer is formed from a material having a dielectric constant of less than 4, in particular less than 3. A considerable improvement of the mechanical stability can thereby be achieved particularly in the case of such mechanically unstable and relatively sensitive materials with respect to the action of mechanical force.

It is particularly advantageous to form the electrically conductive structure below a bonding region of the upper metal layer since, as a result of the mounting or the bonding of the electronic component particularly in the region below the bonding region, large mechanical forces take effect and may lead to damage and destruction.

Further advantageous refinements of the invention are specified in the subclaims.

An exemplary embodiment is explained in more detail below with reference to the diagrammatic drawings, in which:

Figure 1 shows a sectional illustration of an electronic component according to the invention;

Figure 2 shows a perspective illustration of a first exemplary embodiment of an electrically conductive structure of the electronic component according to the invention;

Figure 3 shows a plan view of a second exemplary embodiment of an electrically conductive

structure of the electronic component according to the invention;

Figure 4 shows a perspective illustration of a detail from the electrically conductive structure in accordance with Figure 3.

In the figures, identical or functionally identical elements are provided with the same reference symbols.

An electronic component EB (Figure 1) has a first insulation layer 1, which is formed from a material having a low dielectric constant in the exemplary embodiment. An electrically conductive structure 2 is integrated in this first insulation layer 1. The electrically conductive structure 2 is formed as a capacitance structure and is constructed from the metal strips M11 to M33. The metal strips M11 to M33 extend in the z direction parallel to one another, the metal strips M11 to M13, the metal strips M21 to M23 and the metal strips M31 to M33 in each case being formed in a metallization plane. The metal strips M11, M21 and M31 are arranged congruently with respect to one another and are electrically connected to one another by means of via connections v. This also applies analogously to the metal strips M12, M22 and M32 and also M13, M23 and M33. The metal strips M11, M21 and M31 and also M13, M23 and M33 are connected to a supply voltage potential - DC or AC voltage. The metal strips M12, M22 and M32 are connected to earth potential. The capacitance structure is arranged in the first insulation layer 1 in such a way that the metal strips M11, M12 and M13 terminate in a planar manner with the lower horizontal surface of the first insulation layer 1. Equally, the metal strips M31, M32 and M33 are embedded in the first insulation layer 1 with their surfaces in such a way that they form a planar surface with the upper horizontal plane of the first insulation layer 1 in the x-z plane and essentially have the same height level. A

further insulation layer 4b is arranged in a manner adjoining the first insulation layer 1 and is formed from a material having a high mechanical stability in comparison with the mechanical stability of the material of the first insulation layer 1. Components, for example transistors, are formed in this insulation layer 4b. This layer 4b is formed on a substrate (not illustrated).

The structure 2 formed as a capacitance structure may also be formed in diverse ways in addition to the form illustrated in the exemplary embodiment. As further configuration possibilities, mention may be made of the structures in Aparicio, R. and Hajimiri, A.: Capacity Limits and Matching Properties of Integrated Capacitors; IEEE Journal of Solid-State Circuits, Vol. 37, No. 3, 2002, pp. 384-393, which are shown in perspective illustration there in Figures 5 to 10. The capacitance structure 2 may also be realized as a grid structure or as a MOS structure in a semiconductor component.

There is formed on this structure 2 an electrically conductive screening layer 3 as a metal layer which is arranged in a third insulation layer 4a. The screening layer 3, formed as a plate, is arranged in the third insulation layer 4a in such a way that the structure 2 is arranged completely below the screening layer 3. The third insulation layer 4a is embodied as an oxide layer in the exemplary embodiment. An upper metal layer 5 is formed as a bonding pad layer on the third insulation layer 4a. The bonding pad layer 5 is connected to an electrically conductive region 7 by means of a contact hole 6 formed in the third insulation layer 4a. Both the contact hole 6 and the electrically conductive region 7 are arranged outside a bonding region BB of the bonding pad layer 5. In order to obtain an optimum mechanical reinforcement or stabilization of the first insulation layer 1 with regard to the actions of force

that occur during bonding and/or during mounting of the electronic component EB in a housing, the structure 2 is essentially arranged below the bonding region BB. The bonding region BB is produced by removal, for example by exposure or etching, of the layer 10 formed on the bonding pad layer 5, and/or of the oxide and nitride layers 8 and 9. The layer 10 is formed as a PSPI layer (Photo-Sensitive Polyemide layer) in the exemplary embodiment.

The screening layer 3 is connected to earth potential, so that it is possible to prevent a coupling of a signal present at the bonding pad layer 5 into the structure 2 or a coupling of a signal present at the structure 2 into the bonding pad layer 5.

If no screening layer 3 is formed in the exemplary embodiment illustrated (Figure 1), provision may also be made for forming the electrically conductive region 7 in that metallization plane in which the metal strips M31 to M33 are also arranged.

Figure 2 shows a perspective illustration of the capacitance structure 2, the metal strips M11, M21 and M31, the metal strips M12, M22 and M32 and also the metal strips M13, M23 and M33 being contact-connected by means of only one via connection V in each case, viewed in the y direction. The electrical connection of the metal strips M12, M22 and M32 to earth potential and the electrical connection of the metal strips M11, M21, M31, M13, M23 and M33 to supply voltage potential are effected by means of via connections (not illustrated) and metal strips KM (not illustrated). At least the metal strips KM may both be formed in a second insulation layer (not illustrated) which has a higher mechanical stability than the first insulation layer 1 (Figure 1). The second insulation layer may be identical to the third insulation layer 4 illustrated in Figure 1. The material of the second insulation

layer has a higher mechanical stability than the material of the first insulation layer 1. The second insulation layer may be produced for example as an oxide layer or as a layer made of an FSG dielectric. However, it may also be the case that only one of the contact strips KM is formed in the second insulation layer. It is also possible to form the contact metal strips KM in the first insulation layer 1.

Figure 3 illustrates a plan view (viewed in the negative y direction) of a further exemplary embodiment of an electrically conductive structure 2 of an electronic component according to the invention. The electrically conductive structure 2 is formed as an inductance structure in this exemplary embodiment. A spiral metal track MB4 having a rectangular form is formed in a single metallization plane. The metal track MB4 is integrated in the first insulation layer 1, which is not illustrated in this Figure 3. The inductance structure in the form of the spiral metal track MB4 may also be formed in a plurality of metallization planes, in which case, as also in the exemplary embodiment of the capacitance structure in accordance with Figures 1 and 2, an essential point of the invention is to be seen, here as well, inter alia in the fact that the entire metal track MB4 extends in the first insulation layer 1. At its inner end of the spiral, the metal track MB4 is contact-connected by means of via connections V to a contact metal strip KM connected to a supply voltage potential. The contact metal strip KM is produced in a higher metallization plane (viewed in the y direction corresponding to Figures 1, 2 and 4) than the metallization plane in which the metal track MB4 is formed, and is formed in the second insulation layer. In this case, a metallization plane arranged higher is to be understood as a metallization plane which is such that it is further away, viewed in the same direction, from a substrate of an integrated circuit - on which the

electronic component EB according to the invention is arranged - than the metallization plane in which the electrically conductive structure 2 in the form of the capacitance structure and/or the inductance structure is formed. In this exemplary embodiment, too, the second insulation layer may be identical to the third insulation layer 4a illustrated in Figure 1.

The outer second end of the spiral metal track MB4 is likewise electrically connected to earth potential by a via connection (not illustrated) and a further contact metal strip KM (not illustrated). This further metal strip KM may be arranged in the first insulation layer 1 (Figure 1) or the second insulation layer or a higher (viewed in the positive y direction) insulation layer that is possibly present.

The geometrical area configuration of the electrically conductive structure 2 in the plan view (Figure 3) is of secondary importance for the invention. Thus, the spiral metal track in accordance with Figure 3 may also be made square, for example. Equally, the capacitance structure in accordance with Figure 2, in the case of a plan view in the negative y direction, may have a rectangular or square contour, for example. In a particularly advantageous manner, the geometrical area configuration, in particular the contour and thus the dimensions of the electrically conductive structure, are chosen in such a way that the area of the bonding region BB of the first metal layer 5, when projected onto the contour area of the electrically conductive structure, is completely contained in the said contour area of the electrically conductive structure.

Figure 4 shows a perspective sectional illustration of the region I depicted in Figure 3. In Figure 4, an electrically conductive structure 2 formed as an inductance structure is integrated in the first insulation layer 1 and is formed in four metallization

planes. One of the metal tracks MB1 to MB4 is in each case formed in the metallization planes, which metal tracks are electrically contact-connected to one another in each case by means of via connections V. The via connections may be formed as vertical pillars or as elongated strands running parallel to the metal tracks MB1 to MB4. On account of the so-called hierarchical interconnect technology, the metal tracks MB1 to MB4, with increasing distance (positive y direction) from the substrate S, may be formed with a larger cross section (x-y plane) and with an increasing distance (positive y direction) from one another. The second insulation layer (not illustrated), in which the contact metal strip KM is arranged, may be formed on the first insulation layer 1 in a directly adjoining manner. Layers 3 to 10 according to Figure 1 may be arranged above that. As can be seen in Figure 4, the inductance structure 2 in the form of the metal coils MB1 to MB4 is also formed in such a way that the surface regions of the metal track MB4 and the surface regions of the metal track MB1 are formed in a planar manner (viewed in the x-z plane) with the surface of the first insulation layer 1. The course of the metal track MB4 within the first insulation layer 1 is illustrated by broken lines and by way of example for the course of the metal tracks MB1 to MB3. The first insulation layer 1 directly adjoins the insulation layer 4b, the insulation layer 4b being formed on the substrate S.

Provision may also be made for forming the electrically conductive structure 2 in such a way that it has a first partial structure corresponding to a capacitance structure in accordance with the exemplary embodiment in Figures 1 or 2 and a second partial structure corresponding to an inductance structure in accordance with the exemplary embodiment in Figures 3 or 4. In this case, a mechanical stabilization structure and two passive electronic components can be realized with the

electrically conductive structure. The partial structures may be arranged one beside the other or one above the other.

The electrically conductive structure may be realized in diverse ways and is not restricted to the exemplary embodiments shown. Thus, the electrically conductive structure may also be formed in two or more than four metallization planes. Equally, the insulation layers may be constructed from a plurality of layers in each case. Provision may also be made for forming the capacitance structure in accordance with Figures 1 and 2 only in one metallization plane and, for example, for producing only the metal strips M11, M12 and M13.

By means of the electronic component according to the invention and the method for producing the electronic component, it is possible, by means of the suitable formation (shaping) and arrangement of a single electrically conductive structure formed in an insulation layer, in particular a dielectric layer made of a material having a low dielectric constant, to produce both a passive component and a mechanical supporting or stabilization structure for the electronic component EB, in particular for the insulation layer in which the electrically conductive structure is formed, against damage under the action of mechanical force, for example during bonding or mounting of the component in a housing. As a result, optimum utilization is made of the region under the bonding pad layer, which region is otherwise essentially not required in the electronic component EB, thus resulting in a component topology with minimized dimensions and optimized functional utilization.

What is essential to the invention, then, is that the electrically conductive structure has a dual function on the one hand in the form of at least one passive

electronic component and on the other hand as a mechanical stabilization structure for the electronic component EB and in particular for the first insulation layer.

Patent claims

1. Electronic component having
- a first insulation layer (1),
- an upper metal layer (5), in particular an electrically conductive bonding pad layer, which is formed on the first insulation layer (1), and
- an electrically conductive structure (2), which is integrated into the first insulation layer (1), mechanically stabilizes the insulation layer (1) under the action of mechanical force, in particular during the bonding of the upper metal layer (5) and/or the mounting of the electronic component (EB), and is formed as a passive electronic component.

2. Electronic component according to Claim 1, characterized in that
the first insulation layer (1) is formed from a material having a dielectric constant of less than 4, in particular less than 3.

3. Electronic component according to Claim 1 or 2, characterized in that
the upper metal layer (1) has a bonding region (BB) and the electrically conductive structure (2) is essentially arranged vertically below this bonding region (BB).

4. Electronic component according to Claim 3, characterized in that
in that the dimensions of the electrically conductive structure (2) in a plane parallel to the upper metal layer (5) are at least identical in magnitude to the bonding region (BB).

5. Electronic component according to one of the preceding claims,
characterized in that

the electrically conductive structure (2) is electrically connected to supply voltage potential and earth potential, respectively, by means of via connections (V) and electrical contact strips (KM), in particular contact metal strips.

6. Electronic component according to one of the preceding claims,
characterized in that
at least one electrically conductive screening layer (3) is formed between and in a manner electrically insulated from the upper metal layer (5) and the electrically conductive structure (2).

7. Electronic component according to Claim 6,
characterized in that
the screening layer (3) is a second metal layer and is connected to earth potential.

8. Electronic component according to Claim 6 or 7,
characterized in that
the screening layer (3) is formed in a third insulation layer (4a), the third insulation layer (4a) being arranged between the first insulation layer (1) and the upper metal layer (5).

9. Electronic component according to one of Claims 6 to 8,
characterized in that
the screening layer (3) is formed as a contiguous plate or as a grid structure.

10. Electronic component according to one of Claims 6 to 9,
characterized in that
that area of the screening layer (3) which faces the electrically conductive structure (2) is at least identical in magnitude to that area of the conductive structure (2) which faces the screening layer (3), and

is arranged in such a way that when the areas are projected on one another, the said area of the screening layer (3) completely covers the said area of the conductive structure (2).

11. Electronic component according to one of the preceding claims,
characterized in that
the electrically conductive structure (2) is formed as a capacitance structure and/or as an inductance structure.

12. Electronic component according to Claim 11,
characterized in that
at least one partial region of the electrically conductive structure (2) is formed as a capacitance structure and has at least two metallization planes, strips (M11, M12, M13) arranged parallel to one another and insulated from one another being formed in the first metallization plane, which strips are arranged congruently with respect to the strips (M21, M22, M23) arranged parallel to one another and insulated from one another in the second metallization plane and the strips (M11, M21; M12, M22; M13, M23) arranged one above the other in the vertical direction in the two metallization planes being electrically connected by via connections (V).

13. Electronic component according to Claim 11 or 12,
characterized in that
at least one partial region of the electrically conductive structure (2) is formed as an inductance structure and has at least one metallization plane in which a spiral metal track is formed.

14. Electronic component according to Claim 8,
characterized in that
the upper metal layer (5) is electrically connected to an electrically conductive region (7) by means of a

contact region (6) in the third insulation layer (4a), the electrically conductive region (7) being arranged, in particular, in the second or third insulation layer (4).

15. Electronic component according to Claim 14, characterized in that
the contact region (6) and the second electrically conductive region (7) are arranged horizontally offset with respect to the electrically conductive structure (2) and with respect to the bonding region (BB) of the upper metal layer (5).

16. Electronic component according to one of the preceding claims,
characterized in that
the electrically conductive structure (2) is formed in a planar manner with the horizontal surfaces of the first insulation layer (1) and surface regions of the first conductive structure (2) form partial regions of the horizontal surfaces of the first insulation layer (1).

17. Integrated circuit having a substrate and an electronic component (EB) according to one or more of Claims 1 to 16, which electronic component is formed on the substrate.

18. Method for producing an electronic component in which
- a first insulation layer is produced,
- an upper metal layer (5), in particular an electrically conductive bonding pad layer, is produced on the first insulation layer (1), and
- in the first insulation layer (1), an electrically conductive structure (2) is formed as a passive electronic component and as a mechanical stabilization structure in a manner electrically insulated from the upper metal layer (5).

19. Method according to Claim 18,
characterized in that
the first insulation layer (1) is formed from a material having a dielectric constant of less than 4, in particular less than 3.

20. Method according to Claim 18 or 19,
characterized in that
the electrically conductive structure (2) is essentially formed below a bonding region of the upper metal layer (5) and the dimensions of the electrically conductive structure (2) in a plane parallel to the upper metal layer (5) are produced at least identical in magnitude to the bonding region (BB).

21. Method according to one of Claims 18 to 20,
characterized in that
the electrically conductive structure (2) is electrically contact-connected to supply voltage potential and earth potential, respectively, by means of via connections (V) and contact strips (KM), in particular contact metal strips.

22. Method according to one of Claims 18 to 21,
characterized in that
between the upper metal layer (5) and the electrically conductive structure (2), an electrically conductive screening layer (3) is formed in a manner electrically insulated from the upper metal layer (5) and the electrically conductive structure (2), in particular in a third insulation layer (4a) produced on the first insulation layer (1).

23. Method according to Claim 22,
characterized in that
the electrically conductive screening layer (3) is formed as a plate or as a grid structure and is connected to earth potential.

24. Method according to Claim 22 or 23, characterized in that the electrically conductive screening layer (3) is formed in such a way that its horizontal areal extent is at least identical in magnitude to the horizontal areal extent of the electrically conductive structure (2) and the areal extent of the electrically conductive structure (2) is completely covered by the areal extent of the electrically conductive screening layer (3).

25. Method according to one of Claims 18 to 24, characterized in that the electrically conductive structure (2) is formed as a capacitance structure and/or as an inductance structure.

26. Method according to Claim 25, characterized in that at least one partial region of the electrically conductive structure (2) is formed as a capacitance structure, electrically conductive strips (M11, M12, M13; M21, M22, M23) formed in each case parallel to one another and in a manner electrically insulated from one another being produced in a first and a second metallization plane, the strips (M11, M12, M13; M21, M22, M23) of the first and second metallization planes essentially being arranged congruently and being electrically connected by means of via connections (V) and the horizontally adjacent strips (M11, M12, M13; M21, M22, M23) alternately being connected to a first and to a second electrical potential, respectively.

27. Method according to Claim 25 or 26, characterized in that at least one partial region of the electrically conductive structure (2) is formed as an inductance structure, a spiral metal track being produced at least in one metallization plane.

28. Method for producing an integrated circuit, in which a substrate is provided and an electronic component (EB) according to one or more of Claims 18 to 27 is formed on the substrate.