CLAIMS

1. A data error correction circuit, provided in a memory, the data error correction circuit comprising:

a data error correction module, configured to receive first data and a first check code corresponding to the first data, perform error correction on the first data according to the first check code to generate second data, and output the second data; and

a check code generation module, configured to receive the first data and the first check code, generate a second check code according to the first data and the first check code, and output the second check code.

2. The data error correction circuit of claim 1, wherein the data error correction module comprises:

an error correction code generation unit, configured to receive the first data and the first check code and generate a data error correction code and a check error correction code according to the first data and the first check code; and

a data error correction unit, connected to the error correction code generation unit, and configured to receive the first data and the data error correction code, and perform error correction on the first data according to the data error correction code to generate and output the second data.

3. The data error correction circuit of claim 1 or 2, wherein the check code generation module is connected to the error correction code generation unit and configured to receive the data error correction code and the check error correction code, and the check

code generation module is configured to correct the second check code according to the data error correction code or the check error correction code.

4. The data error correction circuit of claim 1 or 2, wherein the check code generation module comprises:

a full check value generation unit, connected to the error correction code generation unit, and configured to receive the first data and the first check code, and generate a full check value according to the first data, the first check code and the data error correction code, or generate the full check value according to the first data, the first check code and the check error correction code, wherein the second check code comprises the full check value.

5. The data error correction circuit of claim 4, wherein the full check value generation unit comprises:

a full check value calculation unit, configured to receive the first data and the first check code, and generate an initial full check value according to the first data and the first check code; and

a full check value error correction unit, connected to the full check value calculation unit and the error correction code generation unit, and configured to perform error correction on the initial full check value according to the data error correction code or the check code error correction code, and output the full check value.

6. The data error correction circuit of claim 5, wherein the full check value error correction unit is configured to, after receiving the data error correction code or the

check error correction code, invert the initial full check value to generate the full check value.

7. The data error correction circuit of claim 5 or 6, wherein the initial full check value is obtained by performing XOR operation on each bit of the first data and each bit of the first check code.

8. The data error correction circuit of any one of claims 4 to 6, wherein the check code generation module comprises:

a check code error correction unit, connected to the error correction code generation unit, and configured to receive the first check code, and perform error correction on the first check code according to the check error correction code, wherein the second check code comprises an error-corrected first check code.

9. The data error correction circuit of claim 8, wherein a highest bit of the second check code is the full check value, and the error-corrected first check code forms remaining bits of the second check code.

10. The data error correction circuit of any one of claims 1 to 9, wherein the first check code comprises 8-bit data.

11. A memory, comprising:

the data error correction circuit of any one of claims 1 to 10;

a first output terminal, configured to output second data; and

a second output terminal, configured to output a second check code corresponding to the second data.

12. An integrated memory apparatus, comprising:

the memory according to claim 11; and

a controller, connected to the memory, and configured to receive second data and a second check code, and perform check and error correction on the second data according to the second check code.

13. The integrated memory apparatus of claim 12, wherein the controller determines, according to the second check code, whether there is a multi-bit error in the second data.

14. A data transmission method, executed by the memory of claim 11, comprising:

acquiring first data to be transmitted and a first check code corresponding to the first data;

performing error correction on the first data according to the first check code and the first data to generate second data;

generating a second check code according to the first data and the first check code; and

simultaneously outputting the second data and the second check code to a controller, to enable the controller to perform check and error correction on the second data according to the second check code.

15. The data transmission method of claim 14, wherein generating the second check code according to the first data and the first check code comprises:

performing XOR operation on each bit of the first data and each bit of the first check code to generate an initial full check value;

acquiring check results of the first data and the first check code; and

generating the second check code according to the check results, the first check code and the full check value.

16. The data transmission method of claim 15, wherein generating the second check code according to the check results, the first check code and the full check value comprises:

when it is determined, according to the check results, that the first check code has an error and the first data does not have an error, performing error correction on the initial full check value to generate a full check value, and performing error correction on the first check code; and

generating the second check code according to an error-corrected first check code and the full check value.

17. The data transmission method of claim 15, wherein generating the second check code according to the check results, the first check code and the full check value comprises:

when it is determined, according to the check results, that the first check code does not have an error and the first data has an error, performing error correction on the initial full check value to generate a full check value; and

generating the second check code according to the first check code and the full check value.

18. The data transmission method of claim 15, wherein generating the second check code according to the check results, the first check code and the full check value comprises:

when it is determined, according to the check results, that the first data and the first check code both do not have an error, generating the second check code according to the first check code and the initial full check value.

19. The data transmission method of claim 16 or 17, wherein performing error correction on the initial full check value to generate the full check value comprises:

inverting the initial full check value to generate the full check value.

20. The data transmission method of claim 14, wherein generating the second check code according to the first data and the first check code comprises:

acquiring check results of the first data and the first check code; and

when it is determined, according to the check results, that the first data and the first check code both do not have an error, performing XOR operation on each bit of the first data and each bit of the first check code to determine a full check value, and

generating the second check code according to the full check value and the first check code;

when it is determined, according to the check results, that only the first data has an error, performing XOR operation on each bit of the second data and each bit of the first check code to determine a full check value, and generating the second check code according to the full check value and the first check code; and

when it is determined, according to the check results, that only the first check code has an error, performing XOR operation on each bit of the first data and each bit of an error-corrected first check code to determine a full check value, and generating the second check code according to the full check value and the error-corrected first check code.