SYSTEM AND METHOD FOR INTEGRATION OF HfO_2 AND RTCVD POLY-SILICON

BACKGROUND

The present disclosure relates generally to the field of semiconductor processing and, more particularly, to a method and system for improving electrical characteristics of dielectrics having a high dielectric constant.

An integrated circuit (IC) is formed by creating one or more devices (e.g., circuit components) on a semiconductor substrate using a fabrication process. As fabrication processes and materials improve, semiconductor device geometries have continued to decrease in size since such devices were first introduced several decades ago. For example, current fabrication processes are producing devices having geometry sizes (e.g., the smallest component (or line) that may be created using the process) of less than 0.1 μm. However, the reduction in size of device geometries frequently introduces new challenges that need to be overcome.

As semiconductor devices, such as metal oxide semiconductor field effect transistors (MOSFETs), are scaled below 0.1 μm, ultra thin SiO_2 gate oxide dielectric films that form portions of the devices may exhibit undesirable leakage current. In order to minimize leakage current while maintaining high drive current, high equivalent oxide thickness (EOT) may be achieved by using thinner films with higher dielectric constants (k). EOT is a thickness value used to compare the performance of MOS gate dielectrics having a dielectric constant that is different than SiO_2 with the performance of SiO_2 MOS gates. For example, EOT may be used to represent the SiO_2 gate oxide thickness required to obtain the same gate capacitance as would be obtained with the alternate dielectric featuring the different dielectric constant k. One method of reducing the EOT is by placing a high-k dielectric film (a film having a dielectric constant k greater than that of SiO_2) immediately over the gate of a MOSFET or over the area where the high-k dielectric becomes the gate of a MOSFET. However, high-k dielectric films may not have the desired electrical properties needed for a particular device design, and therefore, post processing may be necessary. Such post processing adds complexity to the fabrication process and increases production time and costs.

Accordingly, what is needed is a system and method for integrating high-k dielectric layers with other materials utilized in a semiconductor fabrication process.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A illustrates a method for integrating transistor gate deposition processes to produce a semiconductor device having improved electrical characteristics.

Fig. 1B illustrates a schematic view of one embodiment of a process reactor for providing a loading treatment constructed according to aspects of the present disclosure.

Figs. 2A-2D are cross-sectional views of an exemplary integrated circuit produced by a fabrication process that utilizes the method of Fig. 1.

DETAILED DESCRIPTION

The present disclosure relates generally to the field of semiconductor processing and, more particularly, to a system and method for integrating high-k dielectric layers with other materials utilized in a semiconductor fabrication process. It is understood, however, that the following disclosure provides many different embodiments or examples. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Referring to Fig. 1A and with additional reference to Figs. 2A-2D, in one embodiment, a method 100 illustrates a portion of a fabrication process that may be used to produce a semiconductor device, such as a metal oxide semiconductor (MOS) device. It is understood that the MOS device may be a positive-channel MOS (PMOS) structure or a negative-channel MOS (NMOS) structure, and may have a single finger design or a multiple finger design. In the present example, the method 100 is used in the fabrication of a gate on the MOS device. As will be described in greater detail with

respect to Figs. 3A-3D, the method 100 may be used to provide improved electrical characteristics to the MOS device, including the suppression of flatband voltage shifts.

The method 100 may begin after other fabrication steps have been completed. For example, referring specifically to Fig. 2A, prior to the start of the method 100, a device 200 may be formed on a substrate 202. The substrate 202 may be comprised of silicon, silicon-on-insulator (SOI), and diamond. The substrate 202 may be N doped or P doped, and is N doped in the present example for purposes of illustration. The substrate 202 may be provided with one or more isolation layers (not shown). The isolation layers may be local oxidation of silicon (LOCOS) structures or shallow trench isolation (STI) structures that are formed in the substrate 202 to electrically isolate device areas.

A well region 204 may be formed in the substrate 202 by ion implantation (although use of a P doped substrate may negate the need for a well region). For example, the well region 204 may be formed by growing a sacrificial oxide on the substrate 202, opening a pattern for the location of the well, and then using a chained-implantation procedure, as is known in the art. It is understood that the substrate 202 may have a P doped well or a combination of P and N wells.

While not limited to any particular dopant types or schemes, in one embodiment, the well region 204 may employ boron as a p-type dopant and deuterium-boron complexes for an n-type dopant. The deuterium-boron complexes may be formed by plasma treatment of boron-doped diamond layers with a deuterium plasma.

In one embodiment, the well region 204 may be formed using a high density plasma source with a carbon-to-deuterium ratio ranging between about 0.1 percent and about 5 percent in a vacuum process ambient. Boron doping may be provided by the mixing of a boron containing gas with a carbon/hydrogen gas. The boron containing gas may include B_2H_6, B_2D_6 and/or other boron containing gases. The concentration of boron doping may depend upon the amount of boron containing gas that may be leaked or added into the process. The process ambient pressure may range between 0.1 mTorr and about 500 Torr. The substrate 202 may be held at a temperature ranging between 150°C and about 1100°C. High density plasma may be produced by a microwave electron cyclotron resonance (ECR) plasma, a helicon plasma, a

inductively coupled plasma and/or other high density plasma sources. For example, the ECR plasma may utilize microwave powers ranging between about 800 Watts and about 2500 Watts.

As described above, the well region 204 may also comprise n-type deuterium-boron complex regions of the substrate 202, which may be formed by treating the above-described boron-doped regions employing a deuterium plasma. For example, selected areas of the substrate 202 may be covered by photoresist or another type of mask such that exposed boron-doped regions may be treated with the deuterium containing plasma. The deuterium ions may provide termination of dangling bonds, thereby transmuting the p-type boron-doped regions into n-type deuterium-boron complex regions. Alternatively, deuterium may be replaced with tritium, hydrogen and/or other hydrogen containing gases. The concentration of the n-type regions may generally be controlled by a direct current (DC) or a radio frequency (RF) bias of the substrate 202. The above-described processes may also be employed to form lightly-doped source/drain regions in the substrate 202. Of course, other conventional and/or future-developed processes may also or alternatively be employed to form the source/drain regions.

Referring again to Fig. 1A, the method 100 begins in step 102 by cleaning the substrate 202 (Fig. 2A). The substrate 202 may be cleaned using one or more of a variety of chemical cleaners and cleaning methods. For example, the chemical cleaner may be a mixture of H_2SO_4 and H_2O_2 (commonly known as sulfuric peroxide mix (SPM)) that is used for removing native oxides. Other exemplary chemical cleaners and cleaning methods include a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized (DI) water, commonly referred to as an "SC1 clean," as well as a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2), and deionized (DI) water, commonly referred to as an "SC2 clean." The chemical cleaning may be carried out in an high vacuum environment to prevent that formation of an ultra thin oxide that may occur if the substrate 202 is cleaned in an ambient environment.

In step 103 of Fig. 1A and with additional reference to Fig. 2A, a thin insulate 205 may be deposited or formed upon the cleaned substrate 202. The thin insulate 205 may be formed by a plurality of different methods. For example, the thin insulate 205 may be formed upon exposure to air wherein 3 to 15 Angstroms of native oxide may readily form on a semiconductor substrate 202. Alternatively, the cleaned substrate 202 may subsequently proceed to a process where the thin insulate 205 of

SiO_2 may be formed by a low temperature RTP or thermal process. The subsequent transfer to the process for forming the thin insulate 205 may be under an inert gas or vacuum environment. Formation of the thin insulate 205 may be performed wherein an Ar plasma clean may occur prior to the growth of the thin insulate 205. Native oxide may be cleaned from the substrate 202 by the plasma clean and the thin insulate 205 may be deposited insitu of the plasma clean. The thin insulate 205 may be comprised of a variety of different materials including SiO_2, SiC, CN, and SiOC.

In step 104 of Fig. 1A and with additional reference to Fig. 2B, a high-k dielectric film layer 206 is deposited upon the thin insulate 205 and the cleaned substrate 202. The thin insulate 205 may be used as a MOS gate oxide, and may be a thermal oxide, carbon nitride, or any other appropriate gate film. In some examples, the thin insulate 205 may be too thin to be of any appreciable significance, and in other examples, it may be formed so as to have a thickness suitable for the MOS gate.

The high-k layer 206 may be formed from a variety of different materials, such as TaN, TiN, Ta_2O_5, HfO_2, ZrO_2, HfSiON, $HfSi_x$, $HfSi_xN_y$, $HfAlO_2$, $NiSi_x$, or other suitable materials using atomic layer deposition (ALD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), evaporation, or other methods. Generally, the high-k layer may have a thickness between approximately 3 and 50 Angstroms. With some materials, such as HfO_2, the high-k layer 206 may be blanket deposited on the surface of the substrate 202, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfO_2, in some fabrication processes, while selectively depositing the same materials in other processes. Since the gate oxide thickness continues to decrease along with device geometries, incorporating such high-k materials may yield the higher capacitance needed to reduce the gate leakage associated with smaller device geometries.

In the present example, HfO_2 is to be deposited as the high-k layer 206 using ALD, which is frequently used to deposit high-k materials for MOSFET gate fabrication. ALD provides good step coverage, even on large areas, and a dense and pinhole free structure. ALD may be particularly useful for the deposition of metals and metal oxides in high packing density, high aspect ratio applications which have

relatively demanding thin film requirements. In ALD, films grow with a relatively constant growth rate, and each deposition cycle ideally produces one molecular layer of the deposited material on the substrate surface. Usually, the growth rate is below one molecular layer per cycle because the absorbed source chemical molecules may be bulky or the substrate temperature may affect the number of active sites (e.g., –OH groups) on the substrate surface. Metal oxide thin films produced by ALD are generally uniform and have desirable adhesion properties that allow them to become firmly bonded to the substrate surface.

The ALD of a high-k material, such as HfO_2, may be achieved by co-reacting a precursor in the presence of a gas, and then purging the precursor using the same gas. For HfO_2, ALD may utilize a precursor of Hf, such as $HfCl_4$, or other organometallic Hf sources having a variety of ligands attached to the Hf atom may be utilized. For example, appropriate precursors may include $HfCl_4$ or $Hf(OR)_4$, where R is an alkyl such as $CH(CH_3)_2$; $Hf(tmdh)_4$, where tmdh = 2,2,6,6-tetramethyl-3,5-heptanedionato; $Hf(tfac)_4$, where tfac = trifluoroacetylacetonate; or $Hf(NO_3)_4$. Similar precursors may be used for the ALD of other high-k materials, such as ZrO_2. Because carbon containing hafnium precursors may result in excess carbon and fluorine incorporation in the metal oxide film, $HfCl_4$ may be desirable because it may result in limited residual chlorine incorporation. $HfCl_4$ may also be a preferred metal oxide precursor because it may be sublimated by injection and vaporization into the process reactor.

H_2O vapor may be selected as an oxygen source for the HfO_2. In the present example, an HfO_2 deposition process may be carried out at a temperature of 200° C to 400° C, preferably 300° C, with a deposited film thickness of approximately 3 to 50 Angstroms, preferably 35 Angstroms. The ALD process may be performed in cycles with a series of HfO_2 monolayers formed during each cycle until the desired film thickness is achieved for the high-k layer 206.

In step 106 of Fig. 1A and with continued reference to Fig. 2B, a first anneal may be performed on the substrate 202 after the deposition of the high-k material 206. Although the first anneal may be selected from a variety of anneals, in the present example the first anneal is a hydrogen-based anneal treatment. The hydrogen-based anneal treatment may cause hydrogen (H_2) to attach to any residual Cl that may be in

the upper monolayers of the high-k layer 206 (which comprises HfO_2 in the present example). The resulting effluent HCl may then be driven out of the substrate 202. Accordingly, the hydrogen-based anneal may aid in reducing interface traps on the surface of the HfO_2 layer 206. In the present example, the hydrogen-based anneal is performed using H_2, but other gases containing hydrogen, such as NH_3 and SiH_4, may also be used in the first anneal.

For purposes of illustration, the hydrogen-based anneal may be performed at a temperature between approximately 500° C and 1000° C, and at a pressure between approximately 0.1 Torr and 760 Torr (e.g., 1 atmosphere), preferably between 10 Torr and 70 Torr. The processing time for the hydrogen anneal may be between approximately 10 seconds and 10 minutes. In the present example, the hydrogen-based anneal is performed for one minute at a temperature of 800° C and a pressure of 40 Torr. The hydrogen-based anneal may be performed in a rapid thermal process (RTP), in which a single semiconductor substrate may be quickly treated, or the hydrogen-based anneal may be carried out in a conventional furnace where multiple semiconductor substrates are treated in a batch.

In step 108 of Fig. 1A and with continued reference to Fig. 2B, a second anneal may be performed on the high-k layer 206. Although the second anneal may be selected from a variety of anneals, in the present example the second anneal is an oxygen-based anneal treatment. The second anneal may be a diluted oxygen anneal (DOA) performed in the presence of oxygen (O_2) or other oxygen sources, such as N_2O, NO, or D_2O. The oxygen-based anneal may be used following the hydrogen-based anneal of step 106 to improve the electrical characteristics of the high-k layer 206 (and the resulting MOS gate). If the second anneal is a DOA, then the DOA may be performed at a temperature between approximately 700° C and 900° C, and at a pressure between approximately 1 milliTorr and 10 Torr. The processing time for the oxygen-based anneal may be between approximately 1 second to 60 minutes, and may be performed in an RTP. In the present example, the oxygen-based anneal is performed for 1 to 300 seconds at a temperature of 700° C to 900° C and a pressure of 0.1 Torr to 10 Torr

Typically, the use of high-k materials, such as HfO_2, in a MOS gate formation process increases the density of interface traps which causes a flatband voltage shift and a more "stretched out" capacitance-gate voltage (CV) curve. Interface traps may form at sites of imperfect interfaces between the semiconductor substrate and the high-k material. For example, dangling bonds may trap electrons and interfere with the operations performed by electrons that travel through the gate structure.

A related problem associated with the deposition of HfO_2 is that the chlorine contamination of the HfO_2 film may reduce the insulating characteristics of the film and increase leakage. Secondary ion mass spectrometry (SIMS) depth profile analysis of hydrogen treated HfO_2 surfaces has shown that the hydrogen-based anneal treatment may drive a significant amount of Cl out of the HfO_2 film from a depth of up to 3 nm. The Cl content reduction in the HfO_2 film may reduce the flatband voltage and improve electron and hole mobility in the gate structure.

In step 110 of Fig. 1A and with reference to Fig. 2C, a loading treatment may be applied to the high-k layer 206 and the substrate 202. Prior to steps that may follow step 106, the surface of the high-k layer 206 and the substrate 202 may have a plurality of dangling (-OH) bonds. The dangling bonds may have a negative impact upon any proceeding process after any of the preceding steps 102-108. Step 110 applies a loading treatment that may be applied prior to the commencement of the deposition of a polysilicon layer 208. The loading treatment may be performed insitu (within the same process environment) or exsitu (within an individual process) of the polysilicon layer 208 deposition process. The loading treatment may consist of a H_2 gas treatment, wherein the gas may be passed across the substrate 102. The substrate 202 may be heated by a rapid thermal chemical vapor deposition (RTCVD) reactor.

Referring to Fig. 1B and with continued reference to Fig. 2C, in another embodiment the loading treatment may comprise the periodic H_2 gas treatment of a pseudo-substrate 122 in a process chamber 120. The process chamber 120 may provide single substrate processing of the substrate 202 and a pseudo-substrate 122. The process chamber 120 may provide for CVD, PECVD, ALD, and/or other processes. The process chamber 120 may comprise a single or multiple substrate 202 and/or pseudo-substrate 122. The pseudo-substrate 122 may comprise Si, SiGe, ceramic, SiC, and/or

other materials. The pseudo-substrate 122 may be periodically placed into the process chamber 120, and the loading treatment may be applied to the pseudo-substrate 122. The H_2 gas treatment of the pseudo-substrate 122 may be carried out at a temperature ranging between about 550 C and about 750 C. The H_2 gas loading treatment of the pseudo-substrate 122 may have a process time ranging between about 1 second and about 5 minutes.

The process chamber 120 may have a process environment pressure ranging between about 0.1 Torr and about 80 Torr. Following the loading treatment, the pseudo-substrate 122 may be removed from the process chamber 120 and the substrate 202 may be placed into the process chamber 120. The pseudo-substrate 122 may be placed into the process chamber 120 and treated with the H_2 gas loading treatment at periodic intervals. For example, the pseudo-substrate 122 may be processed by the loading treatment sequentially after the processing of the substrate 202. Alternatively, the pseudo-substrate 122 may be processed by the loading treatment at greater intervals between processing of the substrate 202. The interval may, for example, comprise five, twelve, or twenty-four substrates 202.

Alternatively, the H_2 gas may be excited by a plasma source. The H_2 loading treatment of the high-k layer 206 and the substrate 202 prior to the deposition may remove any dangling (-OH) bonds at the surface. The dangling bonds may cause high leakage of the gate structure if there is no loading treatment to remove the dangling bonds prior to the deposition of the polysilicon layer 208. The introduction of H_2 gas for loading treating the surface immediately prior to ALD of polysilicon layer 208 may provide a uniform and dense polysilicon layer 208 at the interface with the high-k layer 206. In the polysilicon ALD or CVD, H_2 may be used to control the deposition zone and may help to reduce or eliminate any gas phase reactions. The loading treatment of step 110 may employ H_2 gas in an initial process recipe step of the polysilicon layer 208 deposition at a lower temperature wherein dangling bonds may be eliminated and the surface may have molecular H_2 proximate to the surface of the high-k layer 206. The substrate 202 may be treated in the same process chamber used by later step 112. The substrate 202 may be heated at a loading temperature of 450° C to 650° C, preferably 500° C. The loading treatment step 208 process time may range from 1

second to 5 minutes, preferably 120 seconds. The H_2 gas may be controlled up to a partial pressure of 80 Torr during step 110 of the loading treatment, preferably 40 Torr.

At step 112 of Fig. 1A and with reference to Fig. 2C, a polysilicon layer 208 may be deposited upon the treated high-k layer 206 and the substrate 202 to form a polysilicon gate structure using a process such as low pressure chemical vapor deposition (LPCVD), or ALD. The polysilicon layer 208 may be deposited upon the high-k layer 206 and the substrate 202 in a single or batch substrate 202 reactor and may be heated by infra-red (IR) lamps, resistive elements, or any other heating method known by one skilled in the art.

It is understood that some processing steps may occur between step 102 and step 112. For example, the semiconductor substrate may be moved to a different location, or a chamber in which the first anneal is performed may be evacuated to prepare the chamber for another anneal or treatment.

While an annealing process is used for purposes of example at steps 106 and 108, it is understood that other treatments may be used instead. Accordingly, treatments may be performed on the high-k layer, and such treatments include, but are not limited to, annealing processes. For example, a treatment may be performed at a lower temperature that that needed for an annealing process.

Referring now to Fig. 2D, in another embodiment, a silicide layer 210 may be deposited onto the polysilicon layer 208. The silicide layer 210 may be a metal silicide using one or more metals such as titanium, tungsten, cobalt, or nickel. Source and drain extensions (SDEs) 212, 214 (e.g., lightly P- doped areas for a source and drain) in the substrate 202 may be formed by low energy implantation. A spacer 216 may be formed by LPCVD by, for example, depositing an insulating material such as silicon nitride or silicon oxide. The deposited silicon nitride or silicon oxide may then be anisotropically etched back to form the spacer. Heavily P+ doped source and drain regions 218, 220, respectively, may be formed by ion implantation to function as source and drain contact areas. A rapid thermal annealing (RTA) step may be used to activate the implanted dopants. In some examples, the source 218 may be connected to an N+ guard ring 222 and grounded.

While the disclosure has been particularly shown and described with reference to exemplary embodiments, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the disclosure. For example, various parameters may be altered with respect to the chemical(s) selected for a treatment, as well as processing conditions (e.g., temperature, pressure, time, etc.). In addition, while the present disclosure uses a MOS device for purposes of illustration, it is understood that the present disclosure is equally applicable to dynamic random access memory (DRAM), magnetoresistive RAM (MRAM), capacitors, and other devices that may be fabricated on a semiconductor substrate using a high-k dielectric layer. Therefore, the claims should be interpreted in a broad manner, consistent with the present disclosure.

WHAT IS CLAIMED IS:

1. A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material;

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially

2. The method of claim 1 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal; and

selecting a second temperature, a second pressure, and a second time for the oxygen-based anneal.

3. The method of claim 2 wherein the first temperature is selected from a range between 500° C and 1000° C, the first pressure is selected from a range between 0.1 torr and 760 torr, and the first time is selected from a range between 10 seconds and 10 minutes.

4. The method of claim 3 wherein the first temperature is 800° C, the first pressure is 40 torr, and the first time is 1 minute.

5. The method of claim 2 wherein the second temperature is selected from a range between 700° C and 900° C, the second pressure is selected from a range between 1 millitorr and 10 torr, and the second time is selected from a range between 1 second and 300 seconds.

6. The method of claim 1 further comprising selecting a first chemical for the hydrogen-based anneal and a second chemical for the oxygen-based anneal, wherein the first and second chemicals are selected based on a chemical composition of the high-k material.

7. The method of claim 6 wherein the first chemical is H_2.

8. The method of claim 6 wherein the first chemical is NH_3.

9. The method of claim 6 wherein the first chemical is SiH_4.

10. The method of claim 6 wherein the second chemical is O_2.

11. The method of claim 6 wherein the second chemical is N_2O.

12. The method of claim 6 wherein the second chemical is NO.

13. The method of claim 6 wherein the second chemical is D_2O.

14. The method of claim 1 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

15. The method of claim 14 wherein the high-k material is HfO_2, and wherein the method further comprises selecting a deposition temperature from a range between 200° C and 400° C, and selecting a deposition depth from a range between 3 and 75 Angstroms.

16. The method of claim 15 wherein a plurality of cycles of the ALD process are performed until the selected deposition depth is attained

17. The method of claim 1 wherein the substrate is diamond.

18. A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

placing a pseudo-substrate in a process reactor;

applying a loading treatment to the pseudo-substrate;

removing the pseudo-substrate from the process reactor;

placing a device substrate into the process reactor; and

forming a poly-silicon layer upon the device substrate.

19. The method of claim 18 wherein the pseudo-substrate comprises silicon.

20. The method of claim 18 wherein the pseudo-substrate comprises diamond.

21. The method of claim 18 further comprising:

selecting a first temperature, a first pressure, and a first time for the loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

22. The method of claim 21 wherein the first temperature is selected from a range between about 550° C and about 750° C, the first pressure is selected from a range between about 0.1 torr and about 80 torr, and the first time is selected from a range between about 1 seconds and about 5 minutes.

23. The method of claim 22 wherein the first temperature is 625° C, the first pressure is 40 torr, and the first time is 1 minute.

24. The method of claim 21 wherein the second temperature is selected from a range between about 700° C and about 900° C, the second pressure is selected from a range between about 1 millitorr and about 760 torr, and the second time is selected from a range between about 1 second and about 20 minutes.

25. The method of claim 18 further comprising selecting a chemical for the loading treatment.

26. The method of claim 25 wherein the chemical is H_2.

27. The method of claim 25 wherein the chemical is NH_3.

28. The method of claim 25 wherein the chemical is SiH_4.

29. The method of claim 18 wherein the loading treatment is performed within the same process environment as the poly-silicon formation.

30. The method of claim 18 wherein the loading treatment is performed within an individual process environment.

31. The method of claim 18 wherein the loading treatment is proximate to a plasma.

32. A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material;

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially;

applying a loading treatment to the high-k material; and

forming a poly-silicon layer on the treated high-k material, wherein the loading treatment and poly-silicon deposition occur sequentially.

33. The method of claim 32 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal;

selecting a second temperature, a second pressure, and a second time for the oxygen-based anneal.

selecting a third temperature, a third pressure, and a third time for the loading treatment; and

selecting a fourth temperature, a fourth pressure, and a fourth time for the poly-silicon layer formation.

34. The method of claim 33 wherein the first temperature is selected from a range between 500° C and 1000° C, the first pressure is selected from a range between 0.1 torr and 760 torr, and the first time is selected from a range between 10 seconds and 10 minutes.

35. The method of claim 34 wherein the first temperature is 800° C, the first pressure is 40 torr, and the first time is 1 minute.

36. The method of claim 33 wherein the second temperature is selected from a range between 700° C and 900° C, the second pressure is selected from a range between 1 millitorr and 10 torr, and the second time is selected from a range between 1 second and 300 seconds.

37. The method of claim 33 wherein the third temperature is selected from a range between 450° C and 650° C, the first pressure is selected from a range between 0.1 torr and 80 torr, and the third time is selected from a range between 1 seconds and 5 minutes.

38. The method of claim 37 wherein the third temperature is 500° C, the first pressure is 40 torr, and the third time is 2 minutes.

39. The method of claim 33 wherein the fourth temperature is selected from a range between 700° C and 900° C, the fourth pressure is selected from a range between 1 millitorr and 760 torr, and the fourth time is selected from a range between 1 second and 20 minutes.

40. The method of claim 32 further comprising selecting a first chemical for the hydrogen-based anneal, a second chemical for the oxygen-based anneal, and a third chemical for the loading treatment, wherein the first, second, and third chemicals are selected based on a chemical composition of the high-k material.

41. The method of claim 40 wherein the first chemical is H_2.

42. The method of claim 40 wherein the first chemical is NH_3.

43. The method of claim 40 wherein the first chemical is SiH_4.

44. The method of claim 40 wherein the second chemical is O_2.

45. The method of claim 40 wherein the second chemical is N_2O.

46. The method of claim 40 wherein the second chemical is NO.

47. The method of claim 40 wherein the second chemical is D_2O.

48. The method of claim 32 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

49. The method of claim 48 wherein the high-k material is HfO_2, and wherein the method further comprises selecting a deposition temperature from a range between 200° C and 400° C, and selecting a deposition depth from a range between 3 and 75 Angstroms.

50. The method of claim 48 wherein a plurality of cycles of the ALD process are performed until the selected deposition depth is attained.

51. The method of claim 32 wherein the loading treatment is performed within the same process environment of the poly-silicon formation.

52. The method of claim 32 wherein the loading treatment is performed within an individual process environment.

53. The method of claim 32 wherein the loading treatment is proximate to a plasma.

54. The method of claim 32 wherein the substrate is diamond.

55. A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate on the substrate;

depositing a high dielectric constant (high-k) material upon the thin insulate;

performing an anneal on the high-k material;

applying a loading treatment upon the high-k material; and

forming a poly-silicon layer on the treated high-k material, wherein the anneal and poly-silicon deposition occur sequentially.

56. The method of claim 55 further comprising:

selecting a first temperature, a first pressure, and a first time for the loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

57. The method of claim 55 wherein the first temperature is selected from a range between 450° C and 650° C, the first pressure is selected from a range between 0.1 torr and 80 torr, and the first time is selected from a range between 1 seconds and 5 minutes.

58. The method of claim 57 wherein the first temperature is 500° C, the first pressure is 40 torr, and the first time is 2 minutes.

59. The method of claim 55 wherein the second temperature is selected from a range between 700° C and 900° C, the second pressure is selected from a range between 1 millitorr and 760 torr, and the second time is selected from a range between 1 second and 20 minutes.

60. The method of claim 55 further comprising selecting a chemical for the loading treatment.

61. The method of claim 60 wherein the chemical is H_2.

62. The method of claim 60 wherein the chemical is NH_3.

63. The method of claim 60 wherein the chemical is SiH_4.

64. The method of claim 55 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

65. The method of claim 55 wherein the loading treatment is performed within the same process environment of the poly-silicon formation.

66. The method of claim 55 wherein the loading treatment is performed within an individual process environment.

67. The method of claim 55 wherein the loading treatment is proximate to a plasma.

68. The method of claim 55 wherein the high-k material is deposited using atomic layer deposition (ALD) process.

69. The method of claim 68 wherein the high-k material is HfO_2, and wherein the method further comprises selecting a deposition temperature from a range between 200° C and 400° C, and selecting a deposition depth from a range between 3 and 75 Angstroms.

70. The method of claim 68 wherein a plurality of cycles of the ALD process are performed until the selected deposition depth is attained.

71. The method of claim 55 wherein the substrate comprises diamond.

72. A metal oxide semiconductor device formed on a substrate using a sequential hydrogen-based anneal and an oxygen-based anneal, the device comprising:

first and second electrodes;

a thin insulate material separating the first and second electrodes;

a high-k dielectric material separating the first and second electrodes, wherein a flatband response of the dielectric material is altered due to the hydrogen-based and oxygen-based anneals;

a poly-silicon material separating the first and second electrodes, wherein a leakage current of the poly-silicon material is altered due to a loading treatment;

a source positioned proximate to the first electrode; and

a drain positioned proximate to the first electrode and separated from the source by the first electrode.

73. The metal oxide semiconductor device of claim 72 wherein the substrate is diamond.

74. The metal oxide semiconductor device of claim 72 further comprising a silicide layer deposited onto the poly-silicon layer.

75. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises TaN.

76. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises TiN.

77. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises HfSiON.

78. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises nickel silicide.

79. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises hafnium silicate.

80. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises nitrided hafnium silicate.

81. The metal oxide semiconductor device of claim 72 wherein the high-k dielectric comprises hafnium aluminum oxide.