CLAIMS

1. A computer implemented method for balancing currents in a first circuit comprising an array of resistive elements, the method comprising:

receiving, by one or more computer processors, an array of values and an associated vector of array inputs, the array comprising rows and columns;

determining, by the one or more computer processors, a score for each row of the array according to at least one of array row values and an associated array input;

determining, by the one or more computer processors, a ranking of the rows according to the score of each row; and

mapping, by the one or more computer processors, the rows to the first circuit according to the ranking.

2. The method according to claim 1, wherein the resistive elements comprise non-volatile memory elements.

3. The method according to claim 1, wherein the array of values comprises the synaptic weights of a layer within a neural network.

4. The method according to claim 1, further comprising mapping, by the one or more computer processors, columns of a second circuit according to the mapping of rows.

5. The method according to claim 1, further comprising assigning, by the one or more computer processors, each row to an identical segment of multiple identical circuits.

6. The method as claimed in any preceding claim, wherein the mapping the rows comprises: mapping, by the one or more computer processors, the rows to the first circuit comprising the array of resistive elements according to the ranking and a columnar segment current.

7. A computer program product comprising one or more computer readable storage devices and collectively stored program instructions on the one or more computer readable storage devices, the stored program instructions, when executed by one or more computer processors, causing the one or more processors to perform the steps of the computer implemented method of any preceding claim.

8. A computer system for balancing current within a device, the computer system comprising one or more computer readable storage devices and collectively stored program instructions on the one or more computer readable storage devices, the stored program instructions, when executed by one or more computer processors, causing the one or more processors to perform the steps of the computer implemented method of any of preceding claims 1 to 6.