

SPECIFICATION **Improvements in or relating to electronic timepieces**

This invention relates to electronic timepieces of the kind in which time display means are driven by time signals supplied from a frequency divider which is driven by a time standard oscillator — in modern practice, usually a crystal controlled oscillator. The invention is applicable both to timepieces providing an analog display of time and those providing a digital display of time.

It is of great advantage, from the viewpoint of ease of manufacture and of operation, to provide, in an electronic timepiece of the kind referred to, for adjustment of the frequency of the signals actually driving the time display to a value which will result in a very high degree of time-keeping accuracy but to achieve such adjustment without having to adjust the frequency of the time standard oscillator itself. In other words it is of great advantage to effect adjustment of the frequency of the signals driving the time display at some point in the signal channel between the output side of the time standard oscillator and the input side of the time display. In practice, however, this is very difficult to achieve and, although there are known proposals for achieving this, the known proposals have one or more of the serious defects that they provide an undesirably limited range of frequency adjustment, involve the use of complex and expensive circuitry which is difficult to manufacture by mass production methods and difficult to be embodied in structures which are small enough to be satisfactory for use in physically small timepieces such as wrist watches, and tend to be unstable and unreliable in operation. The object of the present invention is to avoid these defects.

According to this invention there is provided in an electronic timepiece having a time standard oscillator, a multi-stage divider dividing down the output frequency from said oscillator, and time display means driven by signals of the divided down frequency, presetting means in at least two stages of the divider; means providing data-input signals to be written into the pre-settable stages; and control means controlling data to be written in, said control means including detecting means which, under the control of signals from the divider, await input signals to be written in, detect their timing, and provide instructing signals for causing the writing in to the pre-settable stages the data input signals provided therefor.

The detecting means may comprise a single detecting circuit or they may include two detecting circuits, one detecting one pre-determined digital condition of the divider stages and the other detecting another pre-determined digital condition thereof. Preferably, in the latter case, the divider includes two sets of pre-settable stages each set consisting of at least two stages and there is provided means providing data input signals for effecting relatively coarse adjustment of frequency and to be written into the stages of

one set, means providing data input signals for effecting relatively fine adjustment of frequency and to be written into the stages of another set; and means responsive to the outputs of the respective detecting circuits for writing into the stages of the respective sets, the data input signals respectively provided therefor.

The timepiece may comprise at least one detecting circuit constituted by a re-set flip-flop consisting of a pair of cross-connected NOR gates.

The invention is illustrated in and explained in connection with the accompanying drawings, in which:—

Figure 1 shows in simplified diagrammatic manner a typical known crystal controlled oscillator as commonly used as a time standard in a conventional electronic timepiece;

Figure 2 is a block diagram of one embodiment of this invention;

Figure 3 is an explanatory table of logic states in the divider stages 7 and 8 of Figure 2;

Figure 4 is a diagram of another embodiment in which provision is made for both rough and precise adjustment of frequency independently;

Figure 5a illustrates, so far as is necessary to an understanding thereof, the nature of a modification which may be adopted in the embodiments of Figures 2 and 4 and in which the logic state on a data input signal terminal is changed into a coded form;

Figure 5b is a truth table of code conversion and relates to the modification illustrated by Figure 5a;

Figure 6 shows, by way of example, a rotary switch which may be employed to determine the logic states at data signal input terminals;

Figure 7a shows one form of circuitry which may be used for any of the divide-by-two divider stages 7 employed in the embodiments of Figures 2 and 4; and

Figure 7b is a pulse timing chart relating to the operation of Figure 7a.

Referring to Figure 1 which shows a crystal controlled oscillator as most usually employed at the time standard oscillator of a conventional so-called quartz timepiece the known oscillator circuit therein shown comprises a piezo-electric crystal 1 across which is connected an inverting amplifier in series with a resistance R_1 and across which is also connected a second resistance R_2 .

The terminals of the crystal are connected to earth through two condensers 1 and 4 the former of which is variable in value and is adjusted in order to adjust the frequency of oscillation. Such a timepiece has the defects that the range of frequency adjustment is undesirably limited; the oscillator becomes increasingly unstable as the frequency is adjusted to values further and further from the natural frequency of the crystal; and owing to the cost and difficulty of manufacturing crystals to a specified natural frequency—as is necessary if errors due to differences between individual crystals intended to be made to the same specification are to be avoided—cost of manufacture becomes undesirably high if a high

degree of timekeeping accuracy is required.

The present invention seeks to avoid these defects.

Referring to Figure 2 the block 5 represents a crystal controlled oscillator which is not itself adjustable in frequency once manufactured; 6 is a divide-by-two divider stage; 7 are divide-by-two divider stages each with a set input terminal S; 8 are divide-by-two divider stages each with a reset input terminal R; 9 is a further divider with a plurality (N) of stages and driving the time display (not shown) of a timepiece; 10 is a detector circuit for detecting a specified logic state; 11, 12 and 13 are terminals to which are applied signals for pre-setting data in the divider stages 7 and 8; 14 is a latching circuit; and 15, 16, 17 and 18 are AND gates.

Figure 7 shows the circuitry of one of the stages 7 of Figure 2, the other being similar. Referring to Figure 7, the set terminal S is connected to one input of a NOR gate 36 the output of which constitutes the $\bar{Q}$ output of the stage. The set terminal S is also connected to one input of another NOR gate 41. 35 etc. are clocked inverters which drive only when clocking signals are applied thereto. The clocking signals are indicated by arrow heads conventionally referenced CL and $\bar{CL}$ and are taken from opposite sides of an inverter. When the logic state at S is "1", the $\bar{Q}$ output from the divider stage is "0" and the Q output thereof is "1". Circuitry of each of the stages 8 is the same as that shown in Figure 7 except for the insertion of an additional gate to ensure that, when the reset terminal (R in Figure 2) is in the "1" state, the $\bar{Q}$ output of the stage is "1" and the Q output is "0".

Referring again to Figure 2 the latching circuit 14 and the AND gates 15, 16, 17 and 18 constitute a control circuit for controlling write-in signals to the divider stages. Assume that there is a little difference between the frequency of the output signal from the oscillator 5 and the frequency actually required. The write-in signal control circuit just mentioned serves to correct for this difference by writing data signals at the terminals 11, 12 and 13 into the divider circuits 7 and 8 to advance or delay the oscillation frequency fed into the divider 9 and thus adjust it to the desired value.

The theory underlying this adjustment of frequency will now be explained with reference to Figure 3 which is a table showing the logic states of the signals at the output terminals Q_2 , Q_3 , Q_4 and Q_5 of the divider stages 7 and 8 of Figure 2 for different frequency adjustments (such as the adjustments indicated in Figure 3 by the values of -4 to +3) determined by data input signals applied at terminals 11, 12 and 13.

Suppose the logic states of the Q_2 , Q_3 , Q_4 and Q_5 outputs of the divider stages 7 and 8 are "0", "0", "1" and "0", respectively. If such data signals are written in at the terminals 11, 12 and 13 as to make these logic states "1", "1", "0" and "0" respectively, the overall logic state is put back by one step, thus delaying the output to divider 9.

If, however, the data written in is such as to make the respective logic states "1", "0", "1" and "0", the overall logic state is advanced by one step, thus advancing the output to the divider 9. As will be seen from Figure 2 output from the divider 9 is fed to one input of a logic state detector 10 constituted by two cross-connected NOR gates 10, the other input of which is fed from the Q_4 output terminal of the first of the two divider stages 8.

When the output signal from the divider 9 is logic "1", the detecting circuit 10 is in the initial state and when the output signal from the divider circuit 9 becomes logic "0", the detecting circuit is awaiting a signal for its operation. In this case, when the Q_4 output of the first of the divider stages 8 is made logic "1", the detecting circuit 10 detects a "1", and produces a differential signal output, that is to say an output signal representative of the difference between the "0" signal on one of its inputs and the "1" signal on the other, and supplies it to the write-in terminal W of the latching circuit 14 and to one input of the AND gate 15. This differential signal acts as a command signal for writing data into the divider stages 7 and 8. When this differential signal is logic "1", the output from the AND gate 15, the other input of which is connected to the Q_M output terminal of the latching circuit, opens the AND gates 16, 17 and 18 and data from the terminals 11, 12 and 13 is written into the divider stages 7 and 8. For example a "1" signal on each of the terminals 11, 12 and 13 produces a "1" at the outputs of the AND gates 16, 17 and 18. In this condition, the Q_2 and Q_3 outputs of the two divider stage 7 become "1" and "1", respectively, and the Q_4 and Q_5 outputs of the divider stage 8 are made "0" and "0" respectively because the output signal from the AND gate 18 is applied to the reset terminal of the divider stage 8. In this way, the logic of the Q_2 , Q_3 , Q_4 and Q_5 outputs of divider stages 7 and 8 is changed from "0", "0", "1" and "0" respectively into "1", "1", "0" and "0". In other words the overall logic state is put back by one step, thereby delaying the input into the divider 9.

A Q_M output from the first of the two stages 7 is taken as a clocking input directly to the clock input terminal CL of the latching circuit 14 and also, through an inverter as shown, to the $\bar{CL}$ clock input terminal of said circuit 14.

The detector 10 is an R—S (reset-set) flip-flop comprising two cross-connected NOR gates. Once the state of the Q_4 output of the first of the two stages 8 is detected, the detector 10 will not return to its initial state until the output from the N stage divider 9 becomes "1". Accordingly, the write-in command signal generated and which appears at the output of the AND gate 15 comes into operation when the Q_4 output of the first of the divider stages 8 first becomes "0" after the output of the divider 9 changes from "1" to "0". In the particular embodiment shown in Figure 2, the logic states "0", "0", "1" and "0" at the Q_2 , Q_3 , Q_4 and Q_5 outputs of the stages 7 and 8 can be

detected by detecting only the output Q_4 . However, not only the specified logic state just mentioned but also any other desired logic state in the general gamut of logic states which can occur can be detected by applying the divider stage outputs corresponding to the desired logic state to an AND gate, the output of which is fed as an input to the detector 10.

In the embodiment shown in Figure 2, if the output from the N stage divider 9 is a signal of 10 seconds period and the output from the divide-by-two divider stage 6 is 16384 Hz, the minimum value of frequency adjustment possible is $1/16384 \times 86400 \times 1/10 \div 0.53$ sec/day. Since this embodiment has three data signals input terminals (11, 12 and 13), frequency adjustment is possible over a range extending from a delay of 2.11 sec/day to an advance of 1.58 sec/day.

Figure 4 shows an embodiment which has, in addition to three data input signal terminals 11, 12 and 13 providing relatively coarse adjustment of frequency as already described with reference to Figure 2, five additional data input signals 19 to 23 for providing relatively fine adjustment of frequency. Since the principles of operation of the circuits for relatively coarse adjustment and for relatively fine adjustment are the same, no further description of these principles is required and little further description of the circuitry is necessary. However it will be seen that there are provided three divide-by-two divider stages 7 with set terminals S; two divide-by-two divider stages 8 the first of which has a set terminal S and the second of which has a re-set terminal R; and two divide-by-two divider stages 24 each having a set terminal S and reset terminal R; and, for fine adjustment, a second latching circuit 26, an additional AND gate 27 and a second logic state detector 25, performing, in fine adjustment, functions similar to those performed, in coarse adjustment, by the circuit parts 14, 15 and 10 respectively. 28 and 29 are AND/or gates to which write-in data (from the gates 15 and 27) for both coarse and fine adjustment are fed. The circuit connections are as shown in Figure 4 and, need no further description. 31 and 32 are AND gates.

In Figure 4 an output signal from the N stage divider 9 is applied to the detector circuit 25 for precise adjustment. This signal is a signal of 120 seconds period, and the logic "0", "0", "0", "0", "0" and "1" on the Q_2 , Q_3 , Q_4 , Q_5 , Q_6 and Q_7 outputs respectively so referenced, is detected. The minimum value of fine adjustment available is $1/16384 \times 86400 \times 1/120 \div 0.044$ sec/day. In Figure 4, a signal 10 seconds period is applied to the detector 10 and a signal of 120 seconds period is applied to the detector 25, and relatively coarse adjustment and relatively fine adjustment are independently performed. The amount of relatively coarse adjustment available and which is effected every 10 seconds is 0.53 sec/day, and the amount of relatively fine adjustment available and which is effected every 120 seconds is 0.044 sec/day. Relatively coarse adjustments and relatively fine adjustment are

effected alternately in accordance with the respective periods of operation of the detectors provided therefor.

The terminals by means of which data input signals for frequency adjustment are supplied to the appropriate divider stages need not be separate individual terminals as shown in Figures 2 and 4. Instead they may be constituted by contacts on a rotary switch or by other switching arrangements. For example, a rotary switch as shown in Figure 6 could be used. In Figure 6, the position of the rotor determines whether a "1" or a "0" appears on one of the leads 11, 12 and 13 (corresponding respectively with the terminals 11, 12 and 13 of Figure 2). If the rotor contacts with two diametrically opposite contacts (shown black) a "1" appears. When it does not a "0" appears. Thus different data input signals can be obtained by moving the rotor to different positions.

The rotary switch shown in Figure 6 may be replaced by a data determining counter with the outputs of the respective digits thereof (corresponding to terminals 11, 12 and 13) connected to the data determining terminals. The logic level of each counter digit can be optionally determined in response to the input pulses thereto. In this way various different outputs can be provided by a counter instead of by the rotary switch of Figure 6.

Figure 5a shows a code converter for connection between terminals 11, 12 and 13 (Figure 5a) and data determining terminals (also referenced 11, 12, 13 in Figure 2) and 19 to 23 in Figure 4, as the case may be. As shown in Figure 5b such a code converter will cause output to appear at one of the terminals 34 to 41 in response to three-bit code signals fed into the terminals 11, 12 and 13 of Figure 5a. The table in Figure 5b shows, in the columns headed 41 to 43, the logic states of the leads similarly referenced and, in columns headed 13, 12, 11 the corresponding logic states on the terminals so referenced.

The divider stage illustrated in Figure 7a has a master portion consisting of the clocked gates 35 and 36 and the NOR gate 38 and a slave portion consisting of the clocked gates 39 and 40 and the NOR gate 41. Clocking inputs are applied as conventionally indicated at CL and $\overline{CL}$. When the clock signal is HIGH the gates 35 and 40 are set in operation and the Q output of the slave portion is written into the master portion, the state of the slave portion remaining unchanged at this time. When the clock signal is LOW only the gates 36 and 39 are set in operation, the master portion is changed into the holding state and the slave portion into the writing state. By a repetition of the foregoing actions, the clocking signal is, in effect, divided by 2 as shown by the waveforms in Figure 7b in which the top line CL represents the clocking signal inputs, the middle line MO represents the master portion output (available as indicated by a broken line connection in Figure 7a) and the bottom line Q represents the slave portion output. By means of a set input applied at S, the NOR

gates 38 and 41 are used to determine the states of the master and slave portions. When this set input is HIGH the outputs of NOR gates 38 and 41 become LOW and the master and slave portion outputs become HIGH.

The amount of frequency regulation obtainable can be chosen as desired over a wide range of amounts since the timing for writing data into the divider stages may be chosen as desired by changing the logic state of the divider stage detecting circuit which determines the timing.

As will now be appreciated, the use of an adjustable frequency arrangement in accordance with this invention to provide time signals in an electronic timepiece enables such a timepiece to be made of very high accuracy without being complex, expensive, or difficult to manufacture. The circuitry necessary is relatively simple and such that pre-setting is required only in those divider stages which must be previously set, frequency adjustment being obtained merely by applying data signals at added connection terminals.

CLAIMS

1. An electronic timepiece having a time standard oscillator, a multi-stage divider dividing down the output frequency from said oscillator, and time display means driven by signals of the divided down frequency; wherein there is provided pre-setting means in at least two stages of the divider; means providing data input signals to be written into the pre-settable stage; and control means controlling data to be written in, said control means including detecting means which, under the control of signals from the divider, await

input signals to be written in, detect their timing, and provide instructing signals for causing the writing in to the pre-settable stages the data input signals provided therefor.

2. A timepiece as claimed in claim 1 wherein the detecting means comprise a single detecting circuit.

3. A timepiece as claimed in claim 1 wherein the detecting means include two detecting circuits, one detecting one predetermined digital condition of the divider stages and the other detecting another pre-determined digital condition thereof.

4. A timepiece as claimed in claim 3 wherein the divider includes two sets of pre-settable stages each set consisting of at least two stages and there is provided means providing data input signals for effecting relatively coarse adjustment of frequency and to be written into the stages of one set, means providing data input signals for effecting relatively fine adjustment of frequency and to be written into the stages of another set; and means responsive to the outputs of the respective detecting circuits for writing into the stages of the respective sets, the data input signals respectively provided therefor.

5. A timepiece as claimed in any of the preceding claims and comprising at least one detecting circuit constituted by a re-set flip-flop consisting of a pair of cross-connected NOR gates.

6. Electronic timepieces having time signal frequency adjusting means substantially as herein described with reference to Figures 2 to 7 inclusive of the accompanying drawings.



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- 15 divider stages which must be previously set, frequency adjustment being obtained merely by applying data signals at added connection terminals.

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- 30 pre-setting means in at least two stages of the divider; means providing data input signals to be written into the pre-settable stage; and control means controlling data to be written in, said control means including detecting means which,
- 35 under the control of signals from the divider, await

input signals to be written in, detect their timing, and provide instructing signals for causing the writing in to the pre-settable stages the data input signals provided therefor.

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- 45 circuits, one detecting one predetermined digital condition of the divider stages and the other detecting another pre-determined digital condition thereof.

4. A timepiece as claimed in claim 3 wherein
- 50 the divider includes two sets of pre-settable stages each set consisting of at least two stages and there is provided means providing data input signals for effecting relatively coarse adjustment of frequency and to be written into the stages of one set, means providing data input signals for effecting relatively fine adjustment of frequency and to be written into the stages of another set; and means responsive to the outputs of the
- 55 respective detecting circuits for writing into the stages of the respective sets, the data input signals respectively provided therefor.

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- 60 consisting of a pair of cross-connected NOR gates.

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