

SPECIFICATION

High voltage integrated circuit switch

- 5 This invention relates to the field of integrated circuits and especially to a high voltage switch and capacitively-coupled drive circuit for providing a high voltage relay with a controlled input, which is suitable for fabrication on a
10 single silicon chip. It also relates to solid state telephone line circuits in which integrated circuit DC relays and capacitively-coupled drive circuitry is required to couple DC input voltages to high voltage switches while main-
15 taining isolation between the high voltage switch and the controlled DC input to the switch.

- Prior art high voltage switches for deriving a high voltage output signal from a DC input
20 in which the switch portion of the circuit has to be made on an integrated circuit silicon chip MOS configuration, for example, must maintain electrical isolation between the solid state relay contacts of the high voltage switch and the control input by which a DC or pulsed
25 direct voltage is coupled to the circuit. This electrical isolation has been achieved by optical couplers or transformers, neither of which can be combined with the high voltage switch on a single integrated circuit chip using currently known integrated circuit fabrication techniques for MOS integrated circuit design. Isolation between the solid state relay output of the high voltage switch and its control
35 input is essential in an integrated circuit configuration since the high voltage at the relay output would destroy the input logic portion of the circuit, causing undesired switching of the relay. Additionally, the isolation of the
40 output terminals of the high voltage switch and its control input is particularly suitable in applications such as telephone line circuit configurations in which a floating ground at the switch is required.

- 45 As mentioned, optical couplers must be made separately and put together as an assembly rather than being fabricated on a single chip for the transmission of signals between two circuits to be electrically isolated
50 from each other. Such couplers typically include a light emitting diode and photosensitive transistors configured so that an input voltage is applied to the LED terminals. The resulting LED light output then turns on the photosensitive transistors to produce an electrically isolated output voltage at the photo-
55 transistor output. Such optical couplers are well known and are further described in Modern Microelectronics by Research and Education Association, Second Printing 1974, at
60 pages 312 and 313 thereof.

- An object of the invention is to provide a circuit which minimizes or even obviates the disadvantages of the known circuits.
65 According to the invention there is provided

a solid state switching circuit with direct current isolation between its input to which an activating input signal may be applied and its output, which circuit includes:

- 70 (a) first gating means having two inputs to one of which is connected the said input to the circuit, a pulse train being applied to the other input of the gating means, the arrangement being such that when a said activating
75 input signal is applied to said one input the gating means passes the pulse train to its output;
(b) second gating means formed by a NAND gate having first and second inputs
80 with the output of the first gating means capacitively coupled to one input of the second gating means and with the output of the first gating means coupled also to the second input of the second gating means via an
85 inverter and further capacitive coupling means, so that when a pulse train output issues from the first gating means to the two inputs of the second gating means receive the said pulse train in anti-phase;
90 (c) a rectification circuit connected to the output of the second gating means and arranged to derive a controlling output from that output when the second gating means delivers an output in response to its two inputs
95 receiving said pulse trains in anti-phase; and
(d) normally conductive semiconductor switching means connected between a pair of output terminals, with control connections from the output of the rectification circuit to the normally non-conductive switching means, the arrangement being such that when said rectification gives a direct current output that output so alters the condition of the switching means that they assume a conductive condition so that current can flow in a circuit to
100 which said two output terminals are connected.
- Such an arrangement may be advantageously used in MOS circuitry made by well-
110 known dielectric isolation processes such as described, for example, in the aforementioned Modern Microelectronics, Second Printing 1974, at pages 425 through 434. One known fabrication technique in which V
115 shaped curves are etched into the surface of the metal oxide semiconductor dice (VMOS) is a well known technique in which the vertical difference between two diffusion layers (the channel length) is maintained short, ie, a few
120 microns, is suitable for fabricating such a circuit. Since these techniques are well known, they will not be described in detail herein, but reference is made to the aforementioned Modern Microelectronics for a description of VMOS fabrication.

- The disclosed circuit without prior art optical couplers or transformers can also be made in large scale integrated circuits (LSI) together with other devices and is particularly suitable
130 and cost effective for use in such LSI circuits

which are designed to be manufactured in large quantity.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which

Figure 1 is a schematic of a high voltage switch and capacitively-coupled drive circuit embodying the invention, and, Fig. 2 is a simplified circuit diagram of a signal generator of the floating isolated bridge type for use in a telephone line circuit in which a circuit such as Fig. 1 may be used.

Referring to Fig. 1, the combined high voltage switch and capacitively-coupled drive circuit is illustrated generally at 10. A 5MHz clock or other suitable signal is coupled through a NAND gate in input logic 12 and drives a pair of matched capacitors in the capacitively-coupled drive circuit 14 to couple an applied direct voltage at the applied clock rate to the high voltage switch 16. Matched capacitors 28 and 30 are typically about ten picofarads with time constants of about 10-4. Input logic 12, capacitively-coupled drive 14 and high voltage switch 16 may be configured on a single silicon chip to which the 5MHz clock is applied by a switch 18 being in the ON position or to which a pulsed DC signal at the control signal input of switch 18 may be applied, which for example, may be at frequency of 100 Hz or less. NAND gate 20 has coupled to one of its logical inputs the 5MHz clock and has coupled at its other logical input 24 a signal which is either low (zero volts) or high (15 volts) to turn the switch 16 OFF or ON respectively. A 15 volt DC source 22 is coupled to NAND gate 20 at the appropriate voltage input for the device used. A pulsed switching operation at a control signal frequency is obtained at the pulse control signal input to switch 18.

When switch 18 is ON, the 15 volts DC applied at 22 is coupled internally in the NAND gate to logical input 24 of NAND gate 20. With the 15 volts coupled to NAND gate 20 on line 26, the 5MHz clock rate appears at the output of NAND gate 20 and is coupled to the capacitors 28 and 30, with the drive voltage coupled directly to capacitor 28 (in-phase) and inverted by inverter 32 before being coupled (out of phase) to the other capacitor 30. The matched capacitors 28 and 30 with values of the 10 pf range capacitively couple the applied input to logic 12 at a voltage level determined by DC source 22 to a diode bridge circuit 34 including four diodes. This effectively decouples the input DC from the voltage on the diode bridge side of capacitors 28 and 30, thereby performing the function previously performed by an optical coupler, *ie*, electrical isolation. The 15 volts DC applied to NAND gate 20 and inverter 32, which is coupled to the diode bridge 34, is also coupled to an EXCLUSIVE OR gate 36 powered by the output of the diode bridge

34. Capacitor 38 filters the input applied to the gate 36 by the diode bridge 34, providing a full wave rectifier fed by an input square wave at 5MHz clock rate.

A direct voltage is provided at the gate electrodes of the high voltage switch 16 as follows: the output of EXCLUSIVE OR 36 is high (ON) only when the two logical inputs 40 and 42 thereto from the diode bridge 34 are out of phase *ie*, when one input is high (logic 1) and the other input is low (logic 0). When the output of gate 36 is high (logic 1), this output is coupled through diode 44, to charge capacitor 46 and turn ON high voltage transistors 48 and 50. This provides a low resistance path between output terminals 52 and 54 at the drains of transistors 48 and 50 respectively. Transistors 48 and 50 may for example, be VMOS transistors, having gate source and drain connections as illustrated, or their equivalent, manufactured by Siliconex Corp., which have a 90 volt capability. This capability can be increased to a 400 to 500 volt output by variation of transistor parameters and the 90 volt example is by way of illustration only.

The operation of the high voltage switch and capacitive drive circuit 10 will now be explained for the case in which the input on line 24 to NAND gate 20 is low (0 volts) *ie*, when switch 18 is OFF. For this condition, the output of NAND gate 20 is an unlocked 15 volts DC, blocked by capacitors 28 and 30. The residual charge of capacitors 28 and 30 is dissipated in resistors 56 and 58 respectively as leakage current. Capacitor 46 is discharged through resistor 60, resulting in a gate-to-source voltage applied to transistors 48 and 50 of 0 volts, which turns transistors 48 and 50 OFF, and provides a high resistance path between terminals 52 and 54 at the drains of transistors 48 and 50 respectively.

Any current which may be coupled to capacitors 28 and 30 from the output terminals 52 and 54 of transistors 48 and 50 gives the same voltage shift across capacitors 28 and 30, which provides in-phase signals at the input terminals 40 and 42 of EXCLUSIVE OR gate 36. Since as aforementioned, EXCLUSIVE OR gate 36 only has an output in response to out-of-phase inputs, the gate 36 is insensitive to the in-phase signal applied at inputs 40 and 42 thereto. Thus the output voltage on terminals 52 and 54 of the high voltage switch has no effect on the operation of the switch, which is turned ON only by the out-of-phase drive. Thus the operation of the gate 36 maintains electrical isolation of the output voltage of switch 16 for all voltages below the break-down limit of transistors 48 and 50 and of capacitors 28 and 30, which as aforementioned may be within the range of 400 to 500 volts. Since all the active components may comprise MOS transistors which are fab-

ricable by well known fabrication techniques, using conventional dielectric isolation processes, the entire circuit is implementable on a single silicon chip. An isolated (from ground) floating switched direct voltage is thus obtained at terminals 52 and 54.

Referring now to Fig. 2, a floating isolated bridge circuit for switching the output on the secondary of a telephone line circuit is illustrated at 100. This circuit is useful as a programmable signal generator in a telephone subscriber line circuit for interfacing analog telephone lines or trunks to a digital switching system of the type described in our Application No. 6797/78. (R. Treiber 1) and to which reference may be made for details of the operation of the line circuit and programmable signal generator. For present purposes the incorporation of switches such as shown in Fig. 1 into the illustrated signal generator is sufficient. In such an arrangement, incoming analog signals such as appear on the tip and ring lines 102 and 104 are sensed, digitized, and processed by a microprocessor to derive a modulated signal from the digitized sensed voltage, which is then coupled back to the programmable signal generator to generate various signals, such as telephone ringing voltage. The details of the operation of such a line circuit are described in the above-mentioned application but it is sufficient for the present purpose that the programmable signal generator 100 must be isolated from the rest of the line circuit (not shown) by a transformer such as ferrite transformer 106. Since the magnitude of the signal generated by such a generator is determined by input control signals derived from a microprocessor, the generator 100 is referred to as a programmable signal generator.

For a given value of voltage coupled to the primary 108 of transformer 106 a drive transistor 110 of a drive circuit has a base drive derived from a microprocessor such that the base drive has a variable pulse duration of the order of 50 to 100 KHz to generate a fixed direct voltage on the tip and ring lines 102 and 104. The pulse duration of the base drive applied to transistor 110 is varied by the microprocessor according to sensed load changes on tip and ring lines 102 and 104, which are sensed in the line circuit and used by the microprocessor to vary the pulse duration of the pulse drive on the base of transistor 110 to enable, for example, the detection of changes in hook status of a telephone subscriber.

A number of switches S1, S2, S3, S4, S5 and S6 are utilised in such a signal generator. Each of the switches S1 to S6 may be a high voltage switch and capacitively-coupled drive circuit such as that of Fig. 1, with the control signal input illustrated by switch 18 of Fig. 1 being provided for switches S3 to S6 by switching control signals from the micropro-

cessor at the control inputs of the switches. Switches S1 and S2 may be used to ground either side of the line for test purposes and inductance 112 serves to isolate the relatively low impedance signal generator from the line.

Operationally, primary 108 stores energy in accordance with the relationship $E = 1/2 L i^2$. When transistor 110 is ON (the indicated positive polarity dots become negative polarity) diode 114 does not conduct. When transistor 110 is OFF diode 114 conducts, charging shunt capacitor 116 and transferring the energy stored in primary 108 to the secondary 118 i.e., to capacitor 116. Energy transfer from the primary to the secondary of the transformer 106 is controlled by the switching of transistor 110 while the amount of energy transferred (the effective output voltage) is controlled by the duty cycle of the switching of transistor 110, which in turn is controlled by the pulse duration modulated signal applied to the base thereof.

Switches S3, S4, S5 and S6, which may comprise VMOS switches of the type described with reference to Fig. 1 are driven by isolated transformer coupled microprocessor controlled switching pulses at their control inputs. An ac signal is generated by a half-wave rectified signal and the switches S3 to S6. When switches S3 and S4 are ON, switches S5 and S6 are OFF, and vice versa. Illustratively, when switches S3 and S4 are ON the negative polarity from capacitor 116 is coupled to the tip line 102 and the positive polarity to the ring line 104. It is important to maintain the floating bridge configuration so that isolation of the outputs of switches S3 to S6 from the control inputs thereto is maintained.

CLAIMS

1. A solid state switching circuit with direct current isolation between its input to which an activating input signal may be applied and its output, which circuit includes:

(a) first gating means having two inputs to one of which is connected the said input to the circuit, a pulse train being applied to the other input of the gating means, the arrangement being such that when a said activating input signal is applied to said one input the gating means passes the pulse train to its output;

(b) second gating means formed by a NAND gate having first and second inputs with the output of the first gating means capacitively coupled to one input of the second gating means and with the output of the first gating means coupled also to the second input of the second gating means via an inverter and further capacitive coupling means, so that when a pulse train output issues from the first gating means the two inputs of the second gating means receive the said pulse train in anti-phase;



ricable by well known fabrication techniques, using conventional dielectric isolation processes, the entire circuit is implementable on a single silicon chip. An isolated (from ground) floating switched direct voltage is thus obtained at terminals 52 and 54.

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For a given value of voltage coupled to the primary 108 of transformer 106 a drive transistor 110 of a drive circuit has a base drive derived from a microprocessor such that the base drive has a variable pulse duration of the order of 50 to 100 KHz to generate a fixed direct voltage on the tip and ring lines 102 and 104. The pulse duration of the base drive applied to transistor 110 is varied by the microprocessor according to sensed load changes on tip and ring lines 102 and 104, which are sensed in the line circuit and used by the microprocessor to vary the pulse duration of the pulse drive on the base of transistor 110 to enable, for example, the detection of changes in hook status of a telephone subscriber.

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cessor at the control inputs of the switches. Switches S1 and S2 may be used to ground either side of the line for test purposes and inductance 112 serves to isolate the relatively low impedance signal generator from the line.

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Switches S3, S4, S5 and S6, which may comprise VMOS switches of the type described with reference to Fig. 1 are driven by isolated transformer coupled microprocessor controlled switching pulses at their control inputs. An ac signal is generated by a half-wave rectified signal and the switches S3 to S6. When switches S3 and S4 are ON, switches S5 and S6 are OFF, and vice versa. Illustratively, when switches S3 and S4 are ON the negative polarity from capacitor 116 is coupled to the tip line 102 and the positive polarity to the ring line 104. It is important to maintain the floating bridge configuration so that isolation of the outputs of switches S3 to S6 from the control inputs thereto is maintained.

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(b) second gating means formed by a NAND gate having first and second inputs with the output of the first gating means capacitively coupled to one input of the second gating means and with the output of the first gating means coupled also to the second input of the second gating means via an inverter and further capacitive coupling means, so that when a pulse train output issues from the first gating means the two inputs of the second gating means receive the said pulse train in anti-phase;



(c) a rectification circuit connected to the output of the second gating means and arranged to derive a controlling output from that output when the second gating means delivers an output in response to its two inputs receiving said pulse trains in anti-phase; and

5 (d) normally non-conductive semiconductor switching means connected between a pair of output terminals, with control connections
10 from the output of the rectification circuit to the normally non-conductive switching means, the arrangement being such that when said rectification gives a direct current output that output so alters the condition of the switching
15 means that they assume a conductive condition so that current can flow in a circuit to which said two output terminals are connected.

2. A switching circuit as claimed in claim 20 1, and which includes a diode bridge connected to the two inputs of the second gating means and arranged to derive from the pulsed inputs to the second gating means a direct current supply for the second gating means.

25 3. A switching means circuit in accordance with claim 3, wherein said first gating means includes an EXCLUSIVE OR gate.

4. A switching circuit in accordance with claim 3, wherein said switching means includes a pair of switching transistors switched
30 ON by the presence of the output of said gate means and OFF by the absence of the output of said gate means.

5. A switching circuit in accordance with claim 4, wherein said transistors are MOS transistors whose gates are coupled to the output of said first gating means and which transistors provide either a high or low resistance path between the drains thereof in response to the presence of an output from said
40 first gating means.

6. A switching circuit in accordance with claim 5, wherein said transistors are VMOS transistors.

45 7. A switching circuit in accordance with claim 3, 4, 5, or 6, wherein said first gating means, said capacitively coupling means, said second gating means and said switching means are comprised on a single silicon chip.

50 8. In a telephone subscriber circuit, a signal generator for generating an electrically isolated output voltage, including signal isolation means having a plurality of switching circuits, each as claimed in any preceding
55 claim.

9. A solid state switching circuit, substantially as described with reference to Fig. 1 of the accompanying drawings.

60 10. A telephone subscriber circuit, substantially as described with reference to Fig. 2 of the accompanying drawings.