formed over active surface 130 and conductive layer 132 using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer 134 contains one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), benzocyclobutene (BCB), polyimide (PI), polybenzoxazoles (PBO), suitable dielectric material, or other material having similar insulating and structural properties. A portion of insulating layer 134 is removed by an etching process through a photoresist layer (not shown) to expose conductive layer 132.

In FIG. 4d, an insulating or passivation layer 136 is formed over insulating layer 134 and the exposed conductive layer 132 using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer 136 contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, BCB, PI, PBO, suitable dielectric material, or other material having similar insulating and structural properties. A portion of insulating layer 136 is removed by an etching process through a photoresist layer to form openings 138 and fully expose conductive layer 132 with respect to insulating layer 136, as shown in FIG. 4e. That is, no portion of insulating layer 136 overlies conductive layer 132.

In one embodiment, a portion of insulating layer 136 is removed by subjecting irradiated DFR material to a developer which selectively dissolves non-irradiated portions of the DFR material to create patterned openings 138 in insulating layer 136 disposed over conductive layer 132, while leaving the irradiated portions of the photoresist material intact.

Alternatively, circular openings 138 can be formed by laser direct ablation (LDA) using laser 140 to remove portions

evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 142 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form bumps 146. In some applications, bumps 146 are reflowed a second time to improve electrical contact to conductive layer 142. Bumps 146 can also be compression bonded to conductive layer 142. An under bump metallization (UBM) layer can be formed between bumps 146 and conductive layer 142. Bumps 146 represent one type of interconnect structure that can be formed over conductive layer 142. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect.

Semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 148 into individual semiconductor die 124. FIG. 5a shows semiconductor die 124 after singulation. Semiconductor die 124 is electrically connected through conductive layers 132 and 142 to bumps 146. The opening 138 fully exposes conductive layer 132 with respect to insulating layer 136, so that no portion of insulating layer 136 overlies conductive layer 132. Conductive layer 142 is formed over portions of insulating layers 134 and 136 and the exposed conductive layer 132. Since insulating layer 136 does not overlap conductive layer 132, a greater separation between adjacent conductive layers 142 can be realized, without losing contact area between conductive layer 132 and conductive layer 142. The greater separation between

adjacent conductive layers 142 increases alignment tolerance.

FIG. 5b shows a plan view of conductive layers 132 and 142 and insulating layer 134, taken along line 5b-5b of FIG. 5a. Conductive layer 142 extends over conductive layer 132 up to one side of insulating layer 134. In one embodiment, the width of conductive layer 132 is 45 μm, and the width between adjacent conductive layers 132 is 5 μm, providing a pitch for conductive layer 132 of 50 μm. The width of contact interface $W_{132-142}$ between conductive layer 132 and conductive layer 142 is at least 20 μm for good contact characteristics, e.g. low contact resistance. The width between adjacent conductive layers 142 $W_{142-142}$ is 30 μm. By increasing the size of opening 138 to fully expose conductive layer 132 with respect to insulating layer 136, a high alignment tolerance is achieved for conductive layer 142 without sacrificing the contact interface $W_{132-142}$.

FIGs. 6a-6c illustrate, in relation to FIGs. 2 and 3a-3c, a process of forming an RDL over a contact pad with reduced interconnect pitch. Continuing from FIG. 4g, an electrically conductive layer 152 is formed over the exposed conductive layer 132 and insulating layers 134 and 136 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating, as shown in FIG. 6a. Conductive layer 152 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 152 can be conformally applied to follow the contour of insulation layers 134 and 136 and conductive layer 132 and, in this embodiment, extends completely across conductive layer 132 up to insulating layer 134 on opposite sides of conductive layer 132. Conductive layer 152 operates as an RDL electrically connected to conductive layer 132. Conductive layer 152 extends in a direction parallel to

Semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 158 into individual semiconductor die 124. FIG. 7a shows semiconductor die 124 after singulation. Semiconductor die 124 is electrically connected through conductive layers 132 and 152 to bumps 156. The opening 138 fully exposes conductive layer 132 with respect to insulating layer 136, so that no portion of insulating layer 136 overlies conductive layer 132. Conductive layer 152 is formed over portions of insulating layers 134 and 136 and the exposed conductive layer 132. Since insulating layer 136 does not overlap conductive layer 132, the contact area between conductive layer 132 and conductive layer 152 is maintained while the width of conductive layer 132 is reduced to decrease the interconnect pitch.

FIG. 7b shows a plan view of conductive layers 132 and 152 and insulating layer 134, taken along line 7b–7b of FIG. 7a. Conductive layer 152 extends over conductive layer 132 between opposing sides of insulating layer 134. In one embodiment, the width of conductive layer 132 is 25 μm, and the width between adjacent conductive layers 132 is 5 μm, providing a pitch for conductive layer 132 of 30 μm. The pitch of conductive layer 132 can range from 30–50 μm. The width of contact interface $W_{132-152}$ between conductive layer 132 and conductive layer 152 is at least 20 μm for good contact characteristics, e.g. low contact resistance. The smaller width of conductive layer 132 reduces interconnect pitch. By increasing the size of opening 138 to fully expose conductive layer 132 with respect to insulating layer 136 and extending conductive layer 152 completely over conductive layer 132 up to insulating layer 134 on opposite sides of conductive layer 132, the width and pitch of conductive layer 132 are reduced without sacrificing the

insulating and structural properties.

Semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 168 into individual semiconductor die 124. FIG. 10a shows semiconductor die 124 after singulation. Semiconductor die 124 is electrically connected to conductive layers 132 and 162. The opening 138 fully exposes conductive layer 132 with respect to insulating layer 136, so that no portion of insulating layer 136 overlies conductive layer 132. Conductive layer 162 is formed over insulating layers 134 and 136 and the exposed conductive layer 132. Since insulating layer 136 does not overlap conductive layer 132 and conductive layer 162 extends in a direction perpendicular to the adjacent conductive layer 132, a greater separation is realized between adjacent conductive layers 162, without losing contact area between conductive layer 132 and conductive layer 162. The greater separation between adjacent conductive layers 162 provides a high alignment tolerance. In addition, the width of conductive layer 132 can be reduced for a smaller interconnect pitch.

FIG. 10b shows a plan view of conductive layers 132 and 162 and insulating layer 134. Conductive layer 162 extends over conductive layer 132 up to one side of insulating layer 134. In one embodiment, the width of conductive layer 132 is 25 μm, and the width between adjacent conductive layers 132 is 5 μm, providing a pitch for conductive layer 132 of 30 μm. The pitch of conductive layer 132 can range from 30-50 μm. The width of contact interface $W_{132-162}$ between conductive layer 132 and conductive layer 162 is at least 20 μm for good contact characteristics, e.g. low contact resistance. The smaller width of conductive layer 132 reduces the interconnect pitch. By increasing the size of opening 138 to fully expose conductive

layer 132 with respect to insulating layer 136 and by extending conductive layer 162 in a direction perpendicular to the adjacent conductive layer 132, the width and pitch of conductive layer 132 is reduced without sacrificing the contact interface $W_{132-162}$. A high alignment tolerance of conductive layer 162 is achieved with the spacing between conductive layers 162.

FIG. 10c shows a cross sectional view of conductive layers 132, conformally applied conductive layer 162, and insulating layers 134, 136, and 164, taken along line 10c-10c of FIG. 10b.

FIGs. 11a-11b illustrate, in relation to FIGs. 2 and 3a-3c, another process of forming an RDL over a contact pad with a high alignment tolerance and reduced interconnect pitch. Continuing from FIG. 4g, an electrically conductive layer 172 is formed over the exposed conductive layer 132 and insulating layers 134 and 136 using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating, as shown in FIG. 11a. Conductive layer 172 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 172 can be conformally applied to follow the contour of insulation layers 134 and 136 and conductive layer 132 and, in this embodiment, extends completely across conductive layer 132 up to insulating layer 134 on opposite sides of conductive layer 132. Conductive layer 172 operates as an RDL electrically connected to conductive layer 132. Conductive layer 172 extends in a direction parallel to active surface 130 and perpendicular to the adjacent conductive layer 132, beyond opening 138 in insulating layer 136, to laterally redistribute the electrical interconnect to conductive layer 132.

In FIG. 11b, an insulating or passivation layer 174 is formed over insulating layer 136 and conductive layer 172 using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer 174 contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, BCB, PI, PBO, suitable dielectric material, or other material having similar insulating and structural properties.

Semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 178 into individual semiconductor die 124. FIG. 12a shows semiconductor die 124 after singulation. Semiconductor die 124 is electrically connected to conductive layers 132 and 172. The opening 138 fully exposes conductive layer 132 with respect to insulating layer 136, so that no portion of insulating layer 136 overlies conductive layer 132. Conductive layer 172 is formed over insulating layers 134 and 136 and the exposed conductive layer 132. Since insulating layer 136 does not overlap conductive layer 132 and conductive layer 172 extends in a direction perpendicular to the adjacent conductive layer 132, a greater separation is realized between adjacent conductive layers 172, without losing contact area between conductive layer 132 and conductive layer 172. The greater separation between adjacent conductive layers 172 provides a high alignment tolerance. In addition, the width of conductive layer 132 can be reduced for a smaller interconnect pitch.

FIG. 12b shows a plan view of conductive layers 132 and 172 and insulating layer 134. Conductive layer 172 extends over conductive layer 132 between opposing sides of insulating layer 134. In one embodiment, the width of conductive layer 132 is 25 µm, and the width between adjacent conductive layers 132 is 5 µm, providing a pitch for conductive layer 132 of 30 µm.

The pitch of conductive layer 132 can range from 30-50 μm. The width of contact interface $W_{132-172}$ between conductive layer 132 and conductive layer 172 is at least 20 μm for good contact characteristics, e.g. low contact resistance. The smaller width of conductive layer 132 reduces the interconnect pitch. By increasing the size of opening 138 to fully expose conductive layer 132 with respect to insulating layer 136 and extending conductive layer 172 completely over conductive layer 132 up to insulating layer 134 on opposite sides of conductive layer 132 in a direction perpendicular to the adjacent conductive layer 132, the width and pitch of conductive layer 132 is reduced without sacrificing the contact interface $W_{132-172}$. A high alignment tolerance of conductive layer 172 is achieved with the spacing between conductive layers 172.

FIG. 12c shows a cross sectional view of conductive layers 132, conformally applied conductive layer 172, and insulating layers 134, 136, and 174, taken along line 12c-12c of FIG. 12b.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor die ~~having~~ including an active surface;

forming a first conductive layer over the active surface of the semiconductor die;

forming a first insulating layer over the active surface of the semiconductor die;

forming a second insulating layer over the first insulating layer and first conductive layer;

removing a portion of the second insulating layer over the first conductive layer so that no portion of the second insulating layer overlies the first conductive layer;

forming a second conductive layer over a portion of the first conductive layer and over the first and second insulating layers and including a width over the first conductive layer that is less than a width of the first conductive layer; and

forming a third insulating layer over the second conductive layer and first and second insulating layers.

2. The method of claim 1, wherein the second conductive layer extends over the first conductive layer up to the first insulating layer.

3. The method of claim 1, wherein the second conductive layer extends across the first conductive layer up to the first insulating layer on opposite sides of the first conductive layer.

4. The method of claim 1, wherein the second conductive layer extends across the first conductive layer up to the first insulating layer on opposite sides of the first conductive layer

in a direction perpendicular to an adjacent first conductive layer.

5. The method of claim 1, wherein a contact interface between the first conductive layer and second conductive layer is at least 20 micrometers.

6. The method of claim 1, wherein a pitch of the first conductive layer ranges from 30-50 micrometers.

7. A method of making a semiconductor device, comprising:

providing a semiconductor die;

forming a first conductive layer over a surface of the semiconductor die;

forming a first insulating layer over the first conductive layer and ~~surface of~~ over the semiconductor die;

~~removing a portion of the first insulating layer over the first conductive layer so that no portion of the first insulating layer overlies the first conductive layer;~~

forming a second ~~conductive~~ insulating layer over the first conductive layer and first insulating layer~~s~~; ~~and~~

~~forming a second insulating layer over the second conductive layer and first insulating layer~~

removing a portion of the second insulating layer over the first conductive layer so that no portion of the second insulating layer overlies the first conductive layer; and

forming a second conductive layer over the first insulating layer and a portion of the first conductive layer.

8. The method of claim 7, further including forming a third insulating layer over the ~~surface of the semiconductor die prior to forming the first~~ second ~~insulating~~conductive layer.

9. The method of claim ~~8~~7, wherein the second conductive layer extends over the first conductive layer up to the ~~third~~first insulating layer.

10. The method of claim ~~8~~7, wherein the second conductive layer extends across the first conductive layer up to the ~~third~~first insulating layer on opposite sides of the first conductive layer.

11. The method of claim 7, wherein the second conductive layer extends across the first conductive layer up to the ~~first~~ second insulating layer on opposite sides of the first conductive layer in a direction perpendicular to an adjacent first conductive layer.

12. The method of claim 7, wherein a contact interface between the first conductive layer and second conductive layer is at least 20 micrometers.

13. The method of claim 7, wherein a pitch of the first conductive layer ranges from 30-50 micrometers.

14. A method of making a semiconductor device, comprising:

providing a semiconductor die;

forming a first conductive layer over ~~a surface of~~ the semiconductor die;

forming a first insulating layer over the ~~surface of the~~ semiconductor die;

forming~~ a second conductive layer that extends across the first conductive layer up to the first insulating layer on opposite sides of the first conductive layer~~ an opening in the first insulating layer over the first conductive layer such that no portion of the first insulating layer overlies the first conductive layer; and

forming a second ~~insulating~~ conductive layer over the ~~second~~ first conductive layer, ~~and first insulating layer~~ the second conductive layer including a width over the first conductive layer that is less than a width of the first conductive layer.

15. The method of claim 14, further including:

forming a ~~third~~ second insulating layer over the ~~first insulating layer~~ semiconductor die and the first conductive layer~~; and~~

~~removing a portion of the third insulating layer over the first conductive layer so that no portion of the third insulating layer overlies the first conductive layer~~.

16. The method of claim 1~~4~~5, wherein the second conductive layer extends over the first conductive layer up to the ~~first~~second insulating layer.

17. The method of claim 1~~4~~5, wherein the second conductive layer extends across the first conductive layer up to the ~~first~~second insulating layer on opposite sides of the first conductive layer in a direction perpendicular to an adjacent first conductive layer.

18. The method of claim 14, wherein a contact interface between the first conductive layer and second conductive layer is at least 20 micrometers.

19. The method of claim 14, wherein a pitch of the first conductive layer ranges from 30-50 micrometers.

20. A semiconductor device, comprising:

a semiconductor die;

a first conductive layer formed over a surface of the semiconductor die;

a first insulating layer formed over the first conductive layer and over the surface of the semiconductor die; and

a second conductive layer~~ extending across the first conductive layer up to the first insulating layer on opposite sides of the first conductive layer; and~~

~~a second insulating layer formed over the second conductive layer and first insulating layer~~ electrically connected to and extending across the first conductive layer up to a first side of the first insulating layer without extending past the first side of the first insulating layer.

21. The semiconductor device of claim 20, further including a ~~third~~second insulating layer formed over the first insulating layer~~ and first conductive layer~~, wherein no portion of the ~~third~~second insulating layer overlies the first conductive layer.

~~22. The semiconductor device of claim 20, wherein the second conductive layer extends over the first conductive layer up to the first insulating layer.~~

2~~3~~2. The semiconductor device of claim 20, wherein the second conductive layer extends across the first conductive layer up to the first insulating layer on opposite sides of the first conductive layer in a direction perpendicular to an adjacent first conductive layer.

2~~4~~3. The semiconductor device of claim 20, wherein a contact interface between the first conductive layer and second conductive layer is at least 20 micrometers.

2~~5~~4. The semiconductor device of claim 20, wherein a pitch of the first conductive layer ranges from 30-50 micrometers.

25. A semiconductor device, comprising:

a semiconductor die;

a first conductive layer formed over the semiconductor die;

a first insulating layer formed over the semiconductor die such that no portion of the first insulating layer overlies the first conductive layer; and

a second conductive layer formed over the first conductive layer and in an opening in the first insulating layer.

26. The semiconductor device of claim 25, further including a second insulating layer formed over the first conductive layer.

27. The semiconductor device of claim 25, further including a second insulating layer formed over the second conductive layer.

28. The semiconductor device of claim 25, wherein the second conductive layer includes a width over the first conductive layer that is less than a width of the first conductive layer.

29. The semiconductor device of claim 25, further including a second insulating layer formed over the semiconductor die and first conductive layer.

30. The semiconductor device of claim 25, wherein a pitch of the first conductive layer ranges from 30-50 micrometers.